CMOS Digital IC Design(R22D6806)

QUESTION BANK

M.TECH
(I YEAR – I SEM)
(2023-24)

Department of Electronics and Communication Engineering

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)

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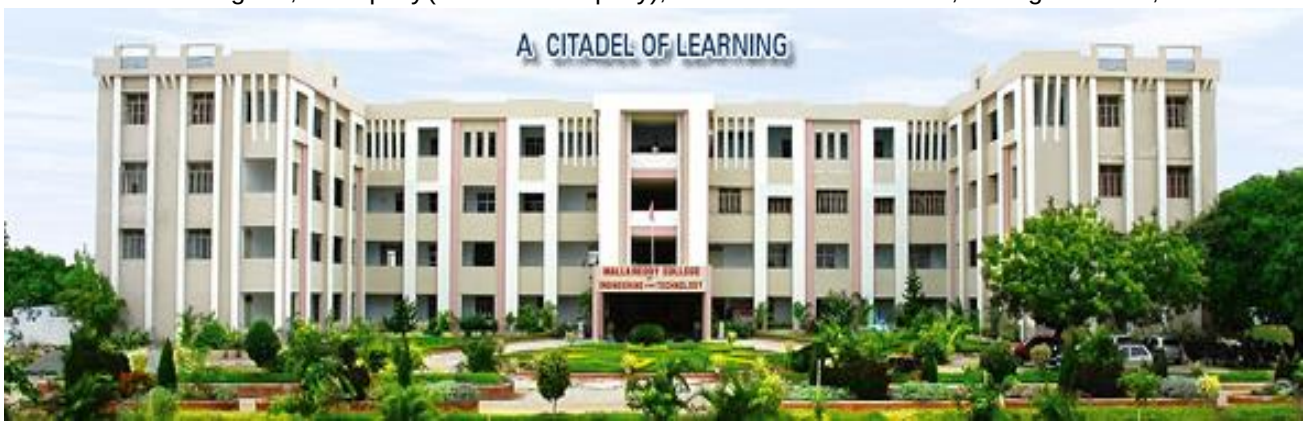
Maisammaguda, Dhulapally (Post Via. Kompally), Secunderabad – 500100, Telangana State, India



Code No: R22D6806 **R22**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, August 2023

CMOS Digital IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 60**

Note: This question paper contains two parts A and B
Part A is compulsory which carries 10 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART-A(10MARKS)

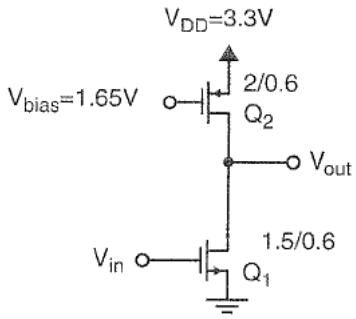
(Write all answers of this PART at one place)

1	A	What would be the approximate threshold voltage of a perfectly designed MOS Inverter if the Power supply voltage is 3.3V?	**[1M]**
	B	Draw the logic diagram of a CMOS Inverter.	**[1M]**
	C	Draw the inverter equivalent of CMOS NOR2 gate.	**[1M]**
	D	Draw the symbol of CMOS transmission gate.	**[1M]**
	E	Give the truth table of NAND-based SR latch circuit.	**[1M]**
	F	What is the advantage of JK latch over SR latch?	**[1M]**
	G	What is the advantage of dynamic logic circuit over a static logic circuit?	**[1M]**
	H	What is 'worst-case-holding time'?	**[1M]**
	I	What is the basic difference between SRAM and DRAM?	**[1M]**
	J	How many memory cells will be there in 32-kbit ROM array?	**[1M]**

PART-B(50 MARKS)

SECTION-I

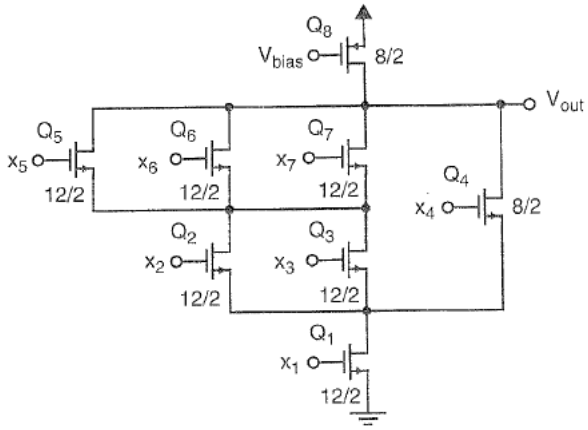
2	A	Estimate the rise time for the pseudo-NMOS inverter shown below. Assume C_L = 75fF. Given W/L values are in µm. Assume $\mu_p C_{ox}$ = 44.5 µA/V^2 and V_{tp} = -0.9V.	**[5M]**



B Derive the equation for the threshold voltage of a pseudo NMOS inverter. **[5M]**

OR

3 Explain the procedure to implement the logic function of a circuit. Also obtain the equivalent logic diagram for the circuit shown below: **[10M]**



SECTION-II

4 Draw the logic diagram of 2-input depletion-load NAND gate and derive the expression for I_D for the same. **[10M]**

OR

5 Design a complex-CMOS logic gate realizing the Boolean function **[10M]**

$F = \overline{A[D+E]+BC}$

SECTION-III

6 Draw the logic diagram of CMOS SR latch circuit based on NAND2 gates and explain its operation. Give the function table along with sample input and output waveforms. **[10M]**

OR

7 Draw a two-stage master-slave flip-flop using D-latch circuits and explain its operation. Also explain with waveforms that what will happen when the 'D' input switches from '0' to '1' immediately before the clock transition occurs? **[10M]**

SECTION-IV

8 What is voltage bootstrapping? Why is a dummy MOS device required to increase the bootstrap capacitance? Explain the reasons with necessary equations. **[10M]**

OR

9 Draw the circuit diagram of dynamic D latch and discuss its operation. **[10M]**

SECTION-V

10	A	Draw the logic diagram of CMOS SRAM cell and explain its various modes of operation.	**[5M]**
	B	Write short notes on fast Sense Amplifiers.	**[5M]**
		OR	
11		Draw the diagram of a Three-transistor DRAM cell and explain various operations with the typical voltage waveforms.	**[10M]**

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Code No: R20D6806 **R20**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, August 2023

CMOS Digital IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

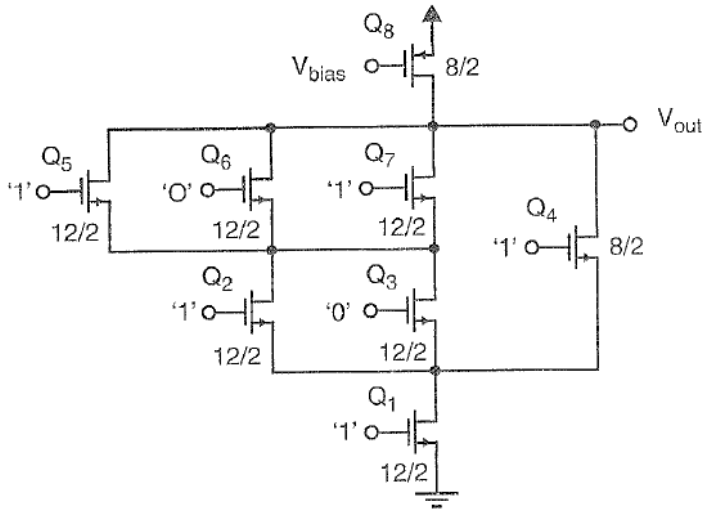
**

SECTION-I

1	A	With a neat circuit diagram, explain the operation of a Pseudo NMOS inverter and derive the inverter threshold voltage	**[7M]**
	B	Draw the Pseudo NMOS realization of exclusive OR function. Clearly indicate the sizing of NMOS transistor to obtain an equivalent delay of a Pseudo NMOS inverter	**[7M]**

OR

2	A	Replace the drive transistor network in the below figure	**[7M]**



	B	With neat circuit sketches, compare the Pseudo NMOS inverter and CMOS inverter.	**[7M]**

SECTION-II

3	A	Draw the circuit diagram of a 2-input NOR gate with depletion NMOS loads and derive its V_{OH} and V_{OL}	**[7M]**
	B	Draw the circuit diagram of a complementary CMOS 2-input NAND gate and draw its mask layout. Clearly label the different parts of the mask layout	**[7M]**

OR

4	A	Draw the circuit diagram of the below circuit using complementary CMOS logic style and draw the mask layout F' = A + BC	**[7M]**
	B	Draw the circuit diagram of a two-input multiplexer using CMOS	**[7M]**

transmission gates and explain its operation

SECTION-III

5	A	Draw the gate level, MOS level schematic of a SR latch using NOR gates and explain its operation with the help of a truth table	**[7M]**
	B	Describe the operation of a D-Latch and provide its CMOS implementation	**[7M]**
		OR	
6	A	Draw the gate level, MOS Level AOI schematic of clocked SR latch and explain its operation with the help of a neat timing diagram	**[7M]**
	B	With a neat schematic, explain the operation of NOR based master-slave edge triggered flip flop	**[7M]**

SECTION-IV

7	A	Distinguish between static and dynamic logic circuits ?? Also describe the advantages of dynamic logic circuits	**[7M]**
	B	Draw the schematic of the dynamic CMOS logic gate implementing F' = A+BC and explain its operation with the help of a neat timing diagram	**[7M]**
		OR	
8	A	Explain the operation of dynamic logic gates with a circuit example and discuss the charge sharing & leakage issues	**[7M]**
	B	Draw the circuit diagram of a dynamic D-Latch and discuss its operation	**[7M]**

SECTION-V

9	A	Classify memory circuits based on data storage and the type of memory access	**[7M]**
	B	Draw the circuit diagram of a full CMOS 6-transistor static RAM cell and describe the read and write operations with a neatly labelled timing diagram	**[7M]**
		OR	
10	A	Describe the construction of NOR based row-decoder and NOR ROM array and explain its operation	**[7M]**
	B	Write short notes on sense amplifiers and row decoders in SRAM memories	**[7M]**

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Code No: **R20D6806**

R20

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, November 2022

CMOS Digital IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	A	Determine the pull-up to pull-down ratio for an NMOS inverter?	**[7M]**
	B	Explain and derive the necessary DC region equations of a CMOS inverter?	**[7M]**
2	A	Define Threshold Voltage. Express threshold voltage and discuss the dependency of V_T on various parameters?	**[7M]**
	B	Write a short note on Transistor equivalency?	**[7M]**
3	A	How the MOS inverters connected in cascade can drive large capacitive loads? Explain?	**[7M]**
	B	Discuss the transient analysis of the CMOS transmission gate by replacing it with a resistor equivalent circuit?	**[7M]**
4	A	Realize NMOS complex logic gates using the Boolean function Z=A(D+C)+BE.	**[7M]**
	B	Write short notes on transmission gates with the relevant circuits?	**[7M]**
5	A	Draw the edge triggered D flip-flop by using CMOS logic and explain its operation in detail?	**[7M]**
	B	Explain behavior of bistable elements.	**[7M]**
6	A	Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table?	**[7M]**
	B	Differentiate flip-flop and latches?	**[7M]**

7	A	Explain voltage boots trapping with an example?	**[7M]**
	B	Write a short note on High performance Dynamic CMOS circuits?	**[7M]**
8	A	Explain the principle of NAND gate flash memory with a neat diagram?	**[7M]**
	B	Compare the SRAM and DRAM?	**[7M]**

Code No: **R20D6806**

R20

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Regular/Supplementary Examinations, June 2

CMOS Digital IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	A	What are the criteria for voltage threshold for high level and low level in NMOS inverter characteristics? Explain.	**[7M]**
	B	Explain the DC noise margin of CMOS logic?	**[7M]**
2	A	Explain the voltage transfer characteristics of a CMOS inverter with a neat diagram?	**[7M]**
	B	Define Threshold Voltage. Express threshold voltage and discuss the dependency of V_T on various parameters?	**[7M]**
3	A	Design and implement AOI and OIA gates using CMOS?	**[7M]**
	B	With the aid of necessary expressions explain the design CMOS NAND2 gate.	**[7M]**
4	A	Explain the propagation delay and power consumption issues of CMOS gate?	**[7M]**

	B	Design and implement CMOS full adder circuit?	**[7M]**
5	A	Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table?	**[7M]**
	B	Differentiate static and dynamic latches?	**[7M]**
6	A	Draw the D latch by using CMOS logic and explain its operation in detail?	**[7M]**
	B	Write a short note on Clocked latch?	**[7M]**
7	A	Explain voltage bootstrapping with an example?	**[7M]**
	B	Write a short note on High performance Dynamic CMOS circuits?	**[7M]**
8	A	Describe the leakage currents in SRAM cell?	**[7M]**
	B	Draw and explain the operation of a single bit dynamic RAM cell?	**[7M]**

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Code No: **R20D6806**

R20

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Regular Examinations, July 2021

CMOS Digital IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	Develop 2 Input NOR gate by Pseudo NMOS Logic and perform its functional verification by using functional verification table.	**[14M]**
2	Perform the Rise time and Fall time analysis of Pseudo NMOS logic with one example.	**[14M]**
3	Sketch the circuit schematic of OAI operation using NMOS logic and Explain its working.	**[14M]**
4	Realize one bit full adder using CMOS logic and explain its working.	**[14M]**
5	Explain Clocked SR Flip Flop operation using appropriate circuit diagram.	**[14M]**

6	Compare Latches and Flip- Flops and list the drawbacks of SR Latch, how those can be overcome by D Latch	**[14M]**
7	Realize Edge triggered D-Flip-Flop using Transmission gates and explain its operation.	**[14M]**
8	Draw the DRAM cell and explain its Read and Write operation and compare DRAM cell with SRAM cell	**[14M]**

Code No: **R20D6806**

R20

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, December 2021

CMOS Digital IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	Compare CMOS logic Inverter and Pseudo NMOS Logic inverter; list the drawbacks of Pseudo NMOS Logic over CMOS logic.	**[14M]**
	OR	
2	Realize 3 Input NAND gate by Pseudo NMOS Logic and perform its functional verification by using functional verification table.	**[14M]**

SECTION-II

3	Develop a 2 X 1 Multiplexer using Transmission gates and interpret its operation using different input combinations.	**[14M]**
	OR	
4	Sketch the circuit schematic of AOI using NMOS logic and explain its operation.	**[14M]**

SECTION-III

5	What are the characteristics of SR Latch? Realize basic SR latch using CMOS logic.	**[14M]**
	OR	
6	Develop Clocked latch and explain its functionality.	**[14M]**

SECTION-IV

7	Realize CMOS Dynamic Latch using transmission gate and explain the Set and Reset conditions of the Latch.	**[14M]**
	OR	
8	Explain about Synchronous dynamic pass transistor circuit with an example.	**[14M]**

SECTION-V

9	Draw the SRAM cell and explain its Read and Write operation.	**[14M]**
	OR	
10	Explain about Leakage currents in DRAM cell and explain why refreshment is needed periodically.	**[14M]**

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Code No: **R18D6810** **R18**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Regular/Supplementary Examinations, January-2020

CMOS Digital Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1 Define Threshold Voltage (V_{TH}). Discuss the dependency of V_{TH} on various parameters. Explain the DC noise margin of CMOS logic. **[14M]**

OR

2 a) Explain in detail about voltage transfer characteristics of CMOS Inverter. **[7M]**

b) Illustrate about pseudo NMOS logic gate. **[7M]**

SECTION-II

3 a) Design and explain the operation of 2 input NMOS NAND. **[7M]**

b) Explain the procedure to design an adder circuit using CMOS logic. **[7M]**

OR

4 Design and implement AOI and OAI using CMOS. **[14M]**

SECTION-III

5	a)	Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table.	**[10M]**
	b)	Differentiate static and dynamic latches.	**[4M]**

OR

6	a)	Draw the D latch by using CMOS logic and explain its operation in detail.	**[8M]**
	b)	Write short notes SR latch in sequential MOS logic.	**[6M]**

SECTION-IV

7	a)	Discuss the transient analysis of CMOS Transmission gate by replacing it with resistor equivalent circuit.	**[8M]**
	b)	Design an EX-OR gate using Transmission gate Logic.	**[6M]**

OR

8	a)	Explain the concept of charge storage and charge leakage associated with pass transistor logic.	**[7M]**
	b)	Explain the speed and power dissipation in dynamic CMOS logic.	**[7M]**

SECTION-V

9		Mention different types of RAM cells. Draw and explain the operation of a single bit dynamic RAM cell.	**[14M]**

OR

10	a)	Write about the leakage currents in SRAM.	**[7M]**
	b)	Explain the principle of NAND flash memory with a neat diagram.	**[7M]**

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Code No: **R17D6807**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, October/November 2020

CMOS Digital Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 2 hours **Max. Marks: 70**

Answer Any **Four** Questions

All Questions carries equal marks.

***

1 a) Derive expression for V_{OL}, V_{OH} ,V_{IL} & V_{IH} of CMOS inverter.

b) Explain and derive the necessary DC region equations of a CMOS inverter.

2 Describe about (i) Pseudo NMOS logic gate and (ii) Dynamic pass transistor

3 Design and implement CMOS full adder circuit.

4 Realize NMOS complex logic gates using the Boolean function Z=A(D+C)+BE.

5 a) Draw the D latch by using CMOS logic and explain its operation in detail.

b) Write short notes on SR latch in sequential MOS logic.

6 a) Discuss about the behaviour of bi-stable elements.

b) Elaborate on edge triggered flipflop.

7 Explain voltage boots trapping with an example.

8 c) Explain the principle of NOR gate flash memory with a neat diagram.

d) Compare the SRAM and DRAM.

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R18

Code No: R18D6810

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, February/March 20

CMOS Digital Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 2 hours 30 min **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1 a	What is threshold voltage? Discuss about Inverter threshold voltage.	**[7M]**
1 b	Realize the XOR gate by using the Pseudo NMOS logic.	**[7M]**
2 a	What is CMOS? Explain the CMOS Inverter logic.	**[7M]**
2 b	Derive the expression for Gain at gate threshold voltage.	**[7M]**
3 a	Summarize the CMOS NAND gate.	**[7M]**
3 b	Realize the following Boolean expression Y = AB + BC + CA by using CMOS gates.	**[7M]**
4 a	Realize the 2 to 1 multiplexer by using Transmission gates.	**[7M]**
4 b	Realize the following Boolean expression Y = (A+B) (B+C) (C+A) by using AOI gates.	**[7M]**
5 a	What do you mean by bistable element? Describe the behavior of bistable elements	**[7M]**
5 b	Discuss the NAND2 based CMOS SR latch with suitable diagram	**[7M]**
6 a		**[7M]**

Draw the clocked NOR based SR latch and explain.

6 b Explain the CMOS implementation of D latch.

R15

7 a **[7M]**

Draw the dynamic bootstrapping arrangement and explain.

8 b Describe the Cascaded domino CMOS logic gates. **[7M]**

Explain the leakage currents in SRAM cell.

8 a **[7M]**

8b Sketch the DRAM cell and explain. **[7M]**

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Code No: R15D6807

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, Dec-18/Jan-19

CMOS Digital Integrated Circuit Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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			Marks	CO	Blooms Level
		SECTION-I			
Q.1.	a)	Determine Pull up to Pull down ratio for an NMOS Inverter?	**[8M]**	**CO1**	**2**
	b)	How MOS inverters connected in cascade can drive large capacitive loads?	**[7M]**	**CO1**	**2**
		OR			
Q.2.	a)	What are the criteria for voltage threshold for high level and low level in NMOS inverter characteristics?	**[8M]**	**CO2**	**2**

	b)	Write a short notes on Pseudo NMOS logic gate?	**[7M]**		

SECTION-II

Q.3.	a)	Explain and derive necessary DC region equations of CMOS inverter?	**[10M]**	**CO3**	**2**
	b)	Consider a CMOS inverter circuit with following parameters: V_{DD}=3.3V,$V_{TO.N}$=0.6V,$V_{TO.P}$=-0.7V,K_N=200uA/V^2,K_P=80uA/V^2.Calculate noise margins of circuit	**[5M]**		
		OR			
Q.4.	a)	Draw and Explain Voltage transfer characteristics of CMOS inverter with relevant expressions?	**[10M]**	**CO2**	**4**
	b)	Explain 2 Input NOR gate with depletion NMOS loads. Calculate output high voltage and output low voltage?	**[5M]**		

SECTION-III

Q.5.	a)	Explain Pseudo NMOS implementation of OAI gate	**[10M]**	**CO3**	**2**
	b)	Explain the behaviour of the two inverter basic bistable element	**[5M]**	**CO3**	**2**
		OR			
Q.6.	a)	Design a CMOS Full adder and Explain its operation using input and output waveforms	**[8M]**	**CO3**	**2**
	b)	Explain how the implementations of AOI and OAI Complex CMOS gate topologies are different	**[7M]**	**CO3**	**3**

SECTION-IV

Q.7.	a)	Explain dynamic CMOS transmission gate logic?	**[8M]**	**CO4**	**4**
	b)	Explain the benefit of Domino CMOS?	**[7M]**	**CO4**	**4**
		OR			
Q.8.		Explain dynamic circuit technique for overcoming threshold voltage drops in digital circuits	**[15M]**	**CO4**	**3**

SECTION-V

Q.9.	a)	Draw the circuit diagram of Dual Port Static RAM and explain its operation.	**[10M]**	**CO5**	**4**

	b)	Classify different types of memories in market.	**[5M]**		
		OR			
Q.10.	a)	Draw the functional diagram of 256-Mb Synchronous DRAM and explain all the signals.	**[10M]**	**CO5**	**5**
	b)	What are the advantages and disadvantages of DRAM over SRAM	**[5M]**		

Code No : **R17D6807**

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, Dec-18/Jan-19

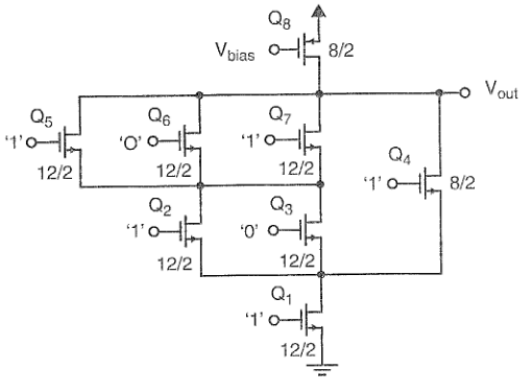
CMOS Digital Integrated Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

*****

			Marks	CO	Blooms Level
		SECTION-I			
Q.1.	a)	Draw the circuit diagram of a Pseudo NMOS inverter and CMOS inverter and compare them	**[7M]**	**CO1**	**2**
	b)	Realize the logic circuit of an ex-or gate using Pseudo NMOS logic	**[7M]**	**CO1**	**2**
		OR			
Q.2.	a)	Derive the inverter switching threshold voltage, output high voltage and output low voltage of a pseudo NMOS inverter	**[7M]**	**CO2**	**2**
	b)	Replace the pull down network (in the circuit shown) by a single equivalent transistor 	**[7M]**		
		SECTION-II			

Q.3.	a)	Draw the circuit diagram of a 2-input NAND gate with NMOS load and derive its output low voltage.	**[7M]**	**CO3**	**2**
	b)	Sketch the CMOS circuit (with both pullup and pull down network) for realizing the Boolean expression $Z' = A(D+E) + BC$	**[7M]**		
		OR			
Q.4.	a)	Draw the circuit diagram of a 2-input CMOS NOR gate and its sample layout (indicating all the layers and their annotation clearly)	**[7M]**	**CO2**	**4**
	b)	Sketch the complementary pass transistor logic implementation of a NAND2 and NOR2 gate	**[7M]**		

SECTION-III

Q.5.	a)	Describe the electrical behavior of bistable element and its potential applications	**[7M]**	**CO3**	**2**
	b)	Sketch the block diagram, gate level schematic and CMOS implementation of a D-Latch. Also explain its operation	**[7M]**	**CO3**	**2**
		OR			
Q.6.	a)	Draw the block diagram, gate level schematic, CMOS schematic and truth table of SR Latch using NOR2 gates	**[7M]**	**CO3**	**2**
	b)	Draw the block diagram, gate level schematic, AOI NAND-based implementation of clocked SR latch and explain its operation	**[7M]**	**CO3**	**3**

SECTION-IV

Q.7.	a)	Distinguish between static logic gates and dynamic logic gates with an example	**[14M]**	**CO4**	**4**
	b)	Describe the cascading problem in dynamic logic gates (with neat circuit diagrams and suggest a solution			
		OR			
Q.8.	a)	With a neat sketch explain the operation of a voltage bootstrapping circuit	**[7M]**	**CO4**	**3**
	b)	Explain in detail about dynamic CMOS circuit techniques.	**[7M]**		

SECTION-V

Q.9.	a)	Classify semiconductor memories and distinguish between SRAM and DRAM memories	**[7M]**	**CO5**	**4**
	b)	Draw the circuit diagram and explain the operation of a 1-bit SRAM cell in both read and write modes	**[7M]**		
		OR			
Q.10.	a)	Draw the circuit diagram of a4-bit X 4-bit NOR based RAM array and explain the operation with its truth table	**[7M]**	**CO5**	**5**
	b)	With a neat sketch explain the operation of a three transistor 1-bit DRAM cell	**[7M]**		