Embedded System Design

(R22D6802)

QUESTION BANK

M.TECH
(I YEAR – I SEM)
(2023-24)

Department of Electronics and Communication Engineering

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution - UGC, Govt. of India)

Recognized under 2(f) and 12 (B) of UGC ACT 1956

(Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2015 Certified)

Maisammaguda, Dhulapally (Post Via. Kompally), Secunderabad – 500100, Telangana State, India

R22

Code No: R22D6802

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, August 2023

Embedded System Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 60**

Note: This question paper contains two parts A and B
Part A is compulsory which carries 10 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART-A (10 Marks)

(Write all answers of this PART at one place)

1	A	Write the ARM nomenclature.	**[1M]**
	B	Compare ARM 10 and ARM 11 families with respect to Pipeline depth and MIPS.	**[1M]**
	C	What is SWI? Write its syntax.	**[1M]**
	D	Draw the *psr* byte fields.	**[1M]**
	E	Illustrate the decoding of simple Thumb ADD instruction into an equivalent ARM ADD instruction.	**[1M]**
	F	Summarize the accessibility of Thumb registers.	**[1M]**
	G	Mention the rules that generate an efficient structure.	**[1M]**
	H	Illustrate the functional view of pipeline executing in ARM state.	**[1M]**
	I	Compare MPU and an MMU.	**[1M]**
	J	What are the possible entries used in L2 page table?	**[1M]**

PART-B (50 Marks)

SECTION-I

2	A	Discuss the ARM design philosophy.	**[5M]**
	B	What are ARM Processor Families? Explain.	**[5M]**
		OR	
3	A	Write a note on Interrupts andVector Table.	**[5M]**
	B	Explain the ARM pipeline executing characteristics.	**[5M]**

SECTION-II

4	A	With coding examples, explain the conditional execution of ARM instructions.	**[5M]**
	B	What are load-store instructions? Explain.	**[5M]**
		OR	
5	A	Explain the arithmetic instructions with code examples.	**[5M]**
	B	What are branch instructions? Explain.	**[5M]**

SECTION-III

6	A	List the complete thumb instructions available in the THUMBv2architecture and describe them.	**[5M]**

	B	Write the syntax of thumb data processing instructions and give two code examples of the same.	**[5M]**
		OR	
7	A	What are multiple register load-store instructions? Explain with examples.	**[5M]**
	B	What is Software Interrupt Instruction? Explain with codeexamples.	**[5M]**
		SECTION-IV	
8	A	Write an example code to create a Queue Structure and to reduce the number of function arguments.	**[5M]**
	B	How to call functions efficiently? Give suitable code examples.	**[5M]**
		OR	
9	A	How can you improve performance by scheduling of load instructions?	**[5M]**
	B	How to allocate variables to register numbers? Explain.	**[5M]**
		SECTION-V	
10	A	Discuss the cache policies that determine the operation of a cache.	**[5M]**
	B	Write a note on Flushing and cleaning cache memory.	**[5M]**
		OR	
11	A	Explain briefly the software configuration and control components in the MMU.	**[5M]**
	B	What are various page tables used by the MMU? Explain briefly about L1 page table.	**[5M]**

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R20

Code No: R20D6802

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, August 2023

Embedded System Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	A	Justify ARM instructions set is suitable for embedded applications?	**[7M]**
	B	What is an Exception? list out the functions of a vector table when Exception occurs?	**[7M]**
		OR	
2	A	Describe the ARM Nomenclature?	**[7M]**
	B	Explain briefly the core Extensions of ARM?	**[7M]**

SECTION-II

3	A	What is the role of Barrel shifter and ALU in Data processing instruction?	**[7M]**
	B	With an example, Explain swap instructions?	**[7M]**
		OR	
4	A	Write about software interrupt instructions?	**[7M]**
	B	Explain about three attributes that is preserved while handling a checked stack	**[7M]**

SECTION-III

5	A	Explain the method for linking ARM and thumb code	**[7M]**
	B	Explain various data processing instruction with their syntax	**[7M]**
		OR	
6	A	Differentiate between variations of branch instructions	**[7M]**
	B	Write short note on single register load store instruction.	**[7M]**

SECTION-IV

7	A	Write the code that creates a queue structure and passes this to function to reduces no. of function arguments and compile it'	**[7M]**
	B	Write a code that identifies a C as vowel and letter.	**[7M]**
		OR	
8	A	Write a assembly code which uses preload method to the string to lower the function	**[7M]**
	B	Write a short note on APCS and ATPCS	**[7M]**

SECTION-V

9	A	Explain the basic Architecture of 4KB cache memory?	**[7M]**
	B	How main memory maps to direct mapped cache?	**[7M]**

OR

10	A	Explain different controls to manage a task's access permission to memory?	**[7M]**
	B	How the FCSE uses page tables and domains? Explain	**[7M]**

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R20

Code No: R20D6802

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, November 2022

Embedded System Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	A	With a neat diagram explain the different hardware components of an embedded device based on ARM core.	**[7M]**
	B	Give different applications of ARM processors.	**[7M]**
2	A	What are interrupts or exceptions? How are they handled in ARM processors?	**[7M]**
	B	Define the architectural inheritance of ARM processor and explain	**[7M]**
3	A	Which are the different features of ARM instruction set that make it suitable for embedded applications.	**[7M]**
	B	Which are the different conditional flags of ARM processor.	**[7M]**
4	A	Examine the implementation of branch, call and return instructions in ARM instruction set.	**[7M]**
	B	Write a program to find the product of two numbers?	**[7M]**

5	A	Explain ARM core dataflow model with a neat diagram.	**[7M]**
	B	Briefly explain the software interrupt instruction.	**[7M]**
6		Write ARM data processing Instructions.	**[14 M]**
7	A	Formulate necessary code using ARM assembly language program for creating a delay?	**[7M]**
	B	Point out the factors that influence the efficiency of loops structure.	**[7M]**
8	A	With neat sketches, explain in detail about shared memory communication and message passing mechanisms	**[7M]**
	B	Explain the mapping between virtual and physical address spaces using translation table.	**[7M]**

Code No: **R20D6802** **R20**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Regular/Supplementary Examinations 2022

Embedded System Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	A	What are interrupt controllers available in ARM Processor? Explain it.	**[7M]**
	B	Explain ARM pipeline with 3,5,6 stages.	**[7M]**
2	A	With a neat diagram explain the different general-purpose registers of ARM processors.	**[7M]**
	B	Explain current program status register (CPSR) with neat diagram.	**[7M]**
3	A	Discuss the instruction set of ARM processor with examples?	**[7M]**
	B	Explain PSR Instructions with examples.	**[7M]**
4	A	With relevant ARM instructions, explain the various forms of base-plus offset addressing.	**[7M]**
	B	Explain briefly the data processing instructions for ARM processor.	**[7M]**

5	A	Differentiate ARM and Thumb instruction set features.	**[7M]**
	B	Explain Multiple – Register of Load-Store Instructions.	**[7M]**
6		Write ARM assembly language code that handles a breakpoint. It should save the necessary registers, call a subroutine to communicate with the host, and upon return from the host, cause the break pointed instruction to be properly executed.	**[14M]**
7	A	Conclude on Optimizing the assembly code in ARM processor.	**[7M]**
	B	Analyze the structure arrangement in programming ARM processor.	**[7M]**
8	A	Briefly explain about co-operative multitasking and pre-emptive multitasking. Bring out the difference between these two contexts switching techniques.	**[7M]**
	B	Discuss the role of LI and L2 cache memories in ARM processor.	**[7M]**

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Code No: **R20D6802**

R20

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Regular Examinations, July 2021

Embedded System Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	Discuss the ARM7-3 Stage pipeline, ARM9-5 Stage pipeline, ARM10-6 Stage pipeline process with an example.	**[14M**
2	Explain the various ARM families and their features.	**[14M**
3	(a). Describe the ARM arithmetic instructions with an example.	**[7M**
	(b). How the branch instructions in ARM programming used to change the flow of execution with an example?	**[7M**
4	(a). How to control the Program Status Register(PSR) instruction?	**[7M**
	(b). With an example explain, how to increase the performance and code density of ARM using conditional execution instructions.	**[7M**
5	List and explain the Thumb register instructions.	**[14M**
6	Explain the Single Register and Multi Register Load Store instructions in thumb mode of ARM programming.	**[14M**
7	(a). Discuss the ARM9TDMI pipelining timings in ARM state.	**[7M**

(b). Elaborate process of the instruction load scheduling by Preloading, Unrolling

8 (a). How the main memory maps to a direct memory mapped (MMU) cache with schematics.

(b). Explain the context switch for write policy of the cache controller.

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R18

Code No: R18D6803

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, February/M 2021

Embedded System Design

(VLSI&ES)

Roll No										

Time: 2 hours 30 min **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	a) Explain architectural features of ARM processor.	**[7M]**
	b) Describe ARM programmer's model with a neat sketch illustrating its visible registers.	**[7M]**
2	a) Write a short note on ARM development tools.	**[7M]**
	b) Summarize the ARM instruction set for Embedded Systems.	**[7M]**
3	a) Discuss about ARM multiple register data transfer instructions along with the syntax formats.	**[7M]**
	b)Discuss about single-Register transfer load store instructions with syntax	**[7M]**
4	a) Describe the conditional execution of ARM instructions with examples.	**[7M]**
		[7M]

	b) Explain about Barrel shifter and its operation for data processing instructions.	
5	a) Illustrate the ARM-Thumb internetworking with suitable example.	**[7M]**
	b) Explain Multiple-Register load store instructions with syntax.	**[7M]**
6	a) Summarize the ARM-Thumb Register usage and explain how we can access its registers in thumb state.	**[7M]**
	b) Tabulate the ARM-Thumb Move, Shift, Comparison and Multiply instructions with syntax.	**[7M]**
7	a) Discuss about the ARM C compiler and its optimization techniques.	**[7M]**
	b)Describe inline functions and inline assembly	**[7M]**
8	a) Differentiate between memory protection unit(MPU) and memory management unit(MMU) .	**[7M]**
	b) Explain about caches and write buffer and write the procedure to configure cache and write buffer for a page.	**[7M]**

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R18

Code No: R18D6803

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Regular/Supplementary Examinations, January-2020
Embedded System Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1 a) Discuss about various types of ARM Registers. **[7M]**
b) Describe about the instruction pipeline. **[7M]**

OR

2 a) Explain about the interrupts and vector table of ARM. **[7M]**
b) Explain about the architecture revision. **[7M]**

SECTION-II

3 a) Explain about the addressing modes of ARM. **[7M]**
b) With a suitable example, explain about the PSR instructions. **[7M]**

OR

4 Why do we use controllers in embedded systems? Explain the instruction set of ARM programming model-1. **[14M]**

SECTION-III

5	a)	What is the difference between instruction set and thumb instruction set?	**[7M]**
	b)	Explain about the Branch instructions and register usage instructions.	**[7M]**

OR

6	a)	Discuss about Software Interrupt Instructions	**[6M]**
	b)	Explain about Single-Register and Multi Register Load-Store Instructions	**[8M]**

SECTION-IV

7	a)	Explain about the conditional execution and loops in ARM programming with a suitable example.	**[7M]**
	b)	With a suitable example, explain about the assembly code using instruction scheduling in ARM programming.	**[7M]**

OR

8	a)	Explain about ARM programming with one example.	**[7M]**
	b)	Describe about the integer and floating point with a suitable example.	**[7M]**

SECTION-V

9	a)	Explain about the Memory management unit and page tables.	**[7M]**
	b)	Explain about the cashe architecture in memory management.	**[7M]**

OR

10	Write a short notes on		
	(i)	Context switch and Register allocation	**[7 M]**
	(ii)	Flushing and cashes	**[7 M]**

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Code No: **R17D9303**

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, October/November 2020

Embedded System Design

(VLSI&ES)

Time: 2 hours **Max. Marks: 70**

Answer Any **Four** Questions

All Questions carries equal marks.

1 a) What is meant by ARM? Explain the ARM design philosophy.
b) Explain the different types of ARM processor families.

2 a) With a suitable example explain about the pipeline of ARM.
b) Draw the CPSR format of ARM and explain with each bit in detail.

3 What is meant by ARM, explain the instruction set of ARM programming model-1.

4 a) With a suitable example explain about the data processing instructions.
b) What is meant by PSR, why we are using in embedded system design?

5 a) What is meant by stack, explain with a suitable example
b) Discuss about the stack and software interrupt instructions in detail

6 Discuss about instruction set and thumb instruction set of ARM Programming.

7 a) Discuss about the assembly code using instruction scheduling in ARM programming with an example.
b) Elucidate about the pointers and structures of ARM programming

8 Write a short notes on

(iii) Cache Architecture and MMU
(iv) Page Tables and Translation

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Code No: **R15D9303**

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, Dec-18/Jan-19

Embedded System Design
(VLSI&ES & SSP)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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			Marks	CO	Blooms Level
		SECTION-I			
Q.1.	a)	With a neat sketch discuss ARM programming model. b) What do you mean by pipelining? Briefly discuss about five stage pipeline in ARM.	**[8M]**	**CO1**	**2**
	b)	With a neat sketch discuss ARM programming model. b) What do you mean by pipelining? Briefly discuss about five stage pipeline in ARM.	**[7M]**	**CO1**	**2**
		OR			
Q.2.		Explain how to measure the processor performance of an embedded hardware in detail and explain the major application areas of embedded system.	**[15M]**	**CO2**	**2**
		SECTION-II			
Q.3.	a)	Explain Load, store instructions with examples.	**[10M]**	**CO3**	**2**
	b)	b) What is the primary difference between a load/store architecture and a register/memory architecture	**[5M]**		
		OR			
Q.4.	a)	What are the unique features of the ARM instruction set? Explain	**[7M]**	**CO2**	**4**
	b)	Briefly explain the ARM data processing instructions in detail with suitable example	**[8M]**		
		SECTION-III			
Q.5.		Explain processor modes of ARM7 , also specify different branch instruction used to exchange branch from ARM mode to THUMB mode.	**[15M]**	**CO3**	**2**

		OR			
Q.6.		Draw the format of ARM data processing instructions Explain the various data operations in ARM.	**[15M]**	**CO3**	**2**

SECTION-IV

Q.7.	a)	Explain the different features of FPA10.	**[8M]**	**CO4**	**4**
	b)	Discuss the coprocessor Register transfer instructions? Why the instruction cannot used for Register transfer of CP15 coprocessor.	**[7M]**	**CO4**	**4**
		OR			
Q.8.		Briefly explain the functions, pointers and structures using in ARM C programming	**[15M]**	**CO4**	**3**

SECTION-V

Q.9.	a)	With a neat diagram discuss set associate cache and fully associative cache.	**[10M]**	**CO5**	**4**
	b)	Elaborate advantages of having embedded memory on chip? How it is useful in increasing the efficiency of the system.	**[5M]**		
		OR			
Q.10.		What are the different types of memories used in embedded system design? Explain each with examples.	**[15M]**	**CO5**	**5**