RTL Simulation and Synthesis with PLDs
(R22D6801)

QUESTION BANK

M.TECH
(I YEAR – I SEM)
(2023-24)

Department of Electronics and Communication Engineering

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
Recognized under 2(f) and 12 (B) of UGC ACT 1956
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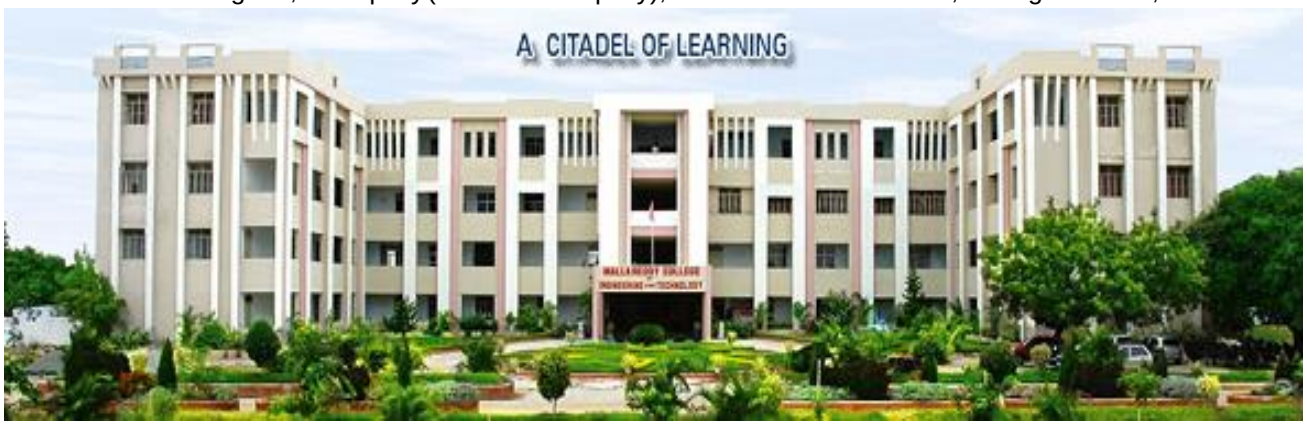

R22

Code No: R22D6801

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, August 2023

RTL Simulation and Synthesis with PLDs

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 60**

Note: This question paper contains two parts A and B
Part A is compulsory which carries 10 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART-A(10 MARKS)

(Write all answers of this PART at one place)

1	A	What is synthesis	**[1M]**
	B	Why design for testability	**[1M]**
	C	What is the importance of HDL	**[1M]**
	D	Why HDL is needed in VLSI	**[1M]**
	E	Why HDL is not a program language	**[1M]**
	F	What is Link	**[1M]**
	G	Distinguish between Link and Layout	**[1M]**
	H	What is link in page layout	**[1M]**
	I	What is advantage of FSM	**[1M]**
	J	What are major components of FSM	**[1M]**

PART-B (50 MARKS)

SECTION-I

2	A	What is the purpose of synthesis in VLSI? What is the basic process of synthesis?	**[5M]**
	B	What are the 5 steps of simulation explain?	**[5M]**
		OR	
3	A	What are the steps involved in the synthesis of a VHDL program	**[5M]**
	B	Why few statements cannot be synthesized in HDLs? Explain	**[5M]**

SECTION-II

4		Explain Various HDL coding issues encountered with suitable example	**[10M]**
		OR	
5	A	Write a VHDL code for 8x3 priority encoder	**[5M]**
	B	Write a Verilog code for 4-bit asynchronous counter using T Flip-Flops	**[5M]**

SECTION-III

6	A	What is scan compression DFT and how does it work?	**[5M]**
	B	Can you explain some uses of clock gating in design?	**[5M]**
		OR	
7	A	What is test point insertion? Can you explain its scenario.	**[5M]**
	B	Write a short note on design complier timing reports.	**[5M]**

SECTION-IV

8	A	Explain different phases of the compiler with example	**[5M]**
	B	Describe the function of hierarchical analysis	**[5M]**
		OR	
9	A	Draw and explain with example the structure of compiler	**[5M]**
	B	What is synthesis compiler and describe compile time language	**[5M]**

SECTION-V

10	A	What is FSM in VLSI design? what are the states and limitations of FSM	**[5M]**
	B	Analyse the block box cell model with example	**[5M]**
		OR	
11	A	What are the constrains to optimize the design of FSM	**[5M]**
	B	Explain terms 1. Setup 2. Hold timing analysis	**[5M]**

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R20

Code No: R20D6801

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, August 2023

RTL Simulation and Synthesis with PLDs

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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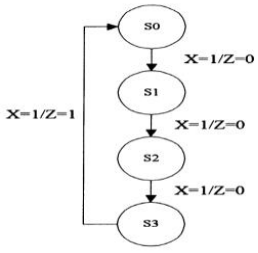
SECTION-I

1	A	Write and explain about Register Transfer Level.	**[7M]**
	B	Explain the RTL Behavioral and Gate-Level Simulation.	**[7M]**
		OR	
2	A	How Design Re-Use helps in complex designs? explain.	**[7M]**
	B	Explain about the Scan Design Technique in brief.	**[7M]**

SECTION-II

3	A	Classify State Machines and explain with the need diagram.	**[7M]**
	B	Write a Verilog code for the given state transition diagram	**[7M]**



OR

4	A	List and discuss basic issues related to HDL coding for synthesis	**[7M]**
	B	Explain One-hot Encoding using VHDL code	**[7M]**

SECTION-III

5	A	Discuss floor planning in brief	**[7M]**
	B	Explain the working of RTL floorplanning.	**[7M]**
		OR	
6	A	List and explain few commonly used Test Compiler commands.	**[7M]**
	B	Write a short note on the following scan techniques (i) Clocked Scan Cell **(ii)** Auxiliary LSSD cell	**[7M]**

SECTION-IV

7	A	Explain how Design Rule Constraints helps in optimization.	**[7M]**
	B	Write a short note on Design Compiler Timing Reports	**[7M]**
		OR	
8	A	Explain the Commonly Used Design Compiler Commands briefly.	**[7M]**
	B	Discuss the Guidelines for Logic Synthesis.	**[7M]**

SECTION-V

9	A	Explain the Procedure for FSM synthesis.	**[7M]**
	B	Discuss about the Fixing Min Delay Violations in detail.	**[7M]**
		OR	
10	A	Explain the Translating Designs with Black-Box Cells	**[7M]**
	B	Discuss any two case studies and speed issues in detail.	**[7M]**

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Code No: R20D6801

R20

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, November 2022

RTL Simulation and Synthesis with PLDs

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions
All Questions carries equal marks.

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1	A	Explain logic synthesis of combination and sequential circuits	**[7M]**
	B	Explain Design Analyzer and Design compiler	**[7M]**
2		Briefly discuss about design reuse, behavioral synthesis, and concepts.	**[14M]**
3	A	Explain the pre-defined and user-defined data types of VHDL language.	**[7M]**
	B	Briefly discuss about HDL Coding issues.	**[7M]**
4		What is the need of hardware description language? Explain the design flow and basic terminology of VHDL language with suitable diagrams.	**[14M]**
5	A	Enumerate the design flow using floor plan manger.	**[7M]**
	B	Explain the steps which are using to generate wire load models	**[7M]**
6	A	Briefly discuss the in-place optimization steps.	**[7M]**
	B	Write short notes on Grouping and Ungrouping of designs	**[7M]**
7	A	List out the different types of compiler commands	**[7M]**
	B	Write a short note on compilers strategies in synthesis	**[7M]**
8	A	Briefly discuss about pad synthesis	**[7M]**
	B	Calculate the static timing delay for Latches and sequential circuits	**[7M]**

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Code No: R20D6801

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Regular/Supplementary Examinations, June 2022

RTL Simulation and Synthesis with PLDs

(VLSI&ES)

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions
All Questions carries equal marks.
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1		Explain the synthesis-based ASIC design flow with a neat diagram	**[14M]**
2	A	Briefly discuss about VHDL Libraries in the Synthesis Environment.	**[7M]**
	B	Explain RTL behavioural and gate level simulation.	**[7M]**
3	A	Briefly discuss about HDL Coding issues.	**[7M]**
	B	Design an FSM for detecting a sequence of 1010 overlapping sequence	**[7M]**
4	A	Write a VHDL code of 16 to 1 multiplexer using CASE statement.	**[7M]**
	B	Explain various loop statements in Verilog	**[7M]**
5	A	Briefly discuss about the DFT flow in synthesis	**[7M]**
	B	Explain advanced critical path resynthesis.	**[7M]**
6	A	Enumerate test synthesis using test complier.	**[7M]**
	B	Discuss floor planning in brief.	**[7M]**
7	A	Explain about clock specification in Synthesis.	**[7M]**
	B	List out the different types of compiler commands	**[7M]**
8		With an example explain the FSM synthesis steps clearly.	**[14M]**

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R20

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Regular Examinations, July 2021

RTL Simulation and Synthesis with PLD's

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	(a)	Summarize the steps involved in the synthesis based ASIC design flow.	**[7M]**
	(b)	Infer VHDL and Verilog code for a positive edge triggered D-flip flop.	**[7M]**
2	(a)	Describe the different VHDL simulation models of the technology library cells to simulate a synthesized gate-level netlist.	**[7M]**
	(b)	Develop VHDL and Verilog code for a AND gate.	**[7M]**
3		Consider a Mealy machine with one input (X) and one output (Z),when X = 0, the current state of the state machine remains unchanged and output Z remains at 0. When X = 1, the state machine makes a transition from one state to the next binary state i.e .. , 00 -> 01 -> l0 -> 11 -> 00 ... The output Z is equal to 1, only when the state is 11 and the input X is equal to 1, else Z is equal to 0. Represent State Transition Diagram and Develop VHDL and Verilog code for the machine.	**[14M]**
4	(a)	Discuss some general issues related to HDL coding for synthesis	**[7M]**
	(b)	Infer the design required for coding in FSM with an example	**[7M]**
5	(a)	List out the critical issues which involved in the conventional Floor Planning.	**[7M]**
	(b)	Describe briefly the commonly used Test Compiler (TC) commands.	**[7M]**
6		Outline the steps involved in test synthesis using the Test Compiler (TC)	**[14M]**
7	(a)	List out the guidelines suggested rules for effective logic synthesis.	**[7M]**
	(b)	Why the timing is report showing "time given to start point" and why is there a violation?	**[7M]**
8		What is the difference between " - " and 'X" in the std _logic type? Synthesis results seem to be the same regardless of which one is used.	**[14M]**