R15

Code No: R15A0401

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, April 2023

Electronic Devices and Circuits

(ECE & CSE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART-A (25 Marks)

1). a	Draw the ideal diode model for forward and reverse bias.	**[2M]**
b	Compare the V-I Characteristics of Ideal diode and non-ideal diode.	**[3M]**
c	Draw the circuit diagram of half wave rectifier.	**[2M]**
d	Draw the block diagram of the regulated power supply. Name the function of each block.	**[3M]**
e	Enumerate the operating regions of a transistor. In which regions it operates like a switch.	**[2M]**
f	The operating point of a Class B amplifier is located at which portion in the load line. What is its maximum efficiency?	**[3M]**
g	What do you mean by Thermal runaway?	**[2M]**
h	List out the advantages of self-biasing circuit?	**[3M]**
i	Draw the drain characteristics of JFET	**[2M]**
j	Mention three different regions of operation of MOSFET. In which region MOSFET acts as resistor?	**[3M]**

PART-B (50 MARKS)

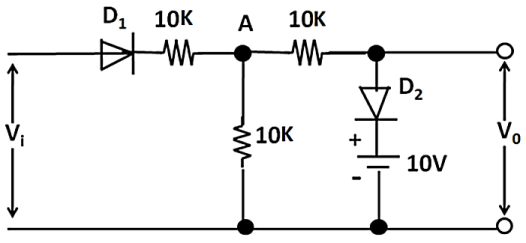
SECTION-I

2	Construct a PN-junction diode and illustrate the formation of the depletion region in a p-n junction. How does the width of this region change when the junction is: (i) Forward biased (ii) Reverse biased. At the temperature of 27^{o}C, calculate the thermal voltage.	**[10M]**

OR

3	Define static and dynamic resistance of a junction diode. Derive an expression for dynamic resistance.	**[10M]**

SECTION-II

4	 Consider the diode circuit shown in Fig. Sketch Vo if Vi = 40 sin ωt.	**[10M]**

Indicate all voltage levels. Assume that all diodes are ideal.

OR

5 Explain the working principle and operation of centre tapped transformer based full wave rectifier. **[10M]**

SECTION-III

6 Draw and explain input and output characteristics of an NPN transistor in CE configuration. Suppose the base current is 100AμandI_{CO} is 0.5mA. Calculate the collector and emitter currents for CE configuration. Assume α=0.9. **[10M]**

OR

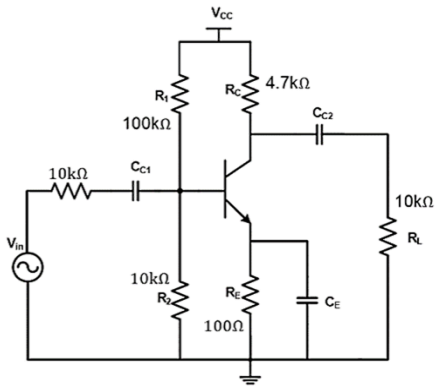
7 Develop hybrid model for transistor in CE configuration. **[10M]**

SECTION-IV

8 Derive the expressions for operating point and stability factor ofvoltage divider bias method. **[10M]**

OR

9 For the amplifier shown in the Figure below, assume $h_{ie} = 1\ K\Omega$ and$h_{fe} = 100$ Also$h_{oe} = h_{re} = 0$. Find A_v, A_{vs}, R_i and R_0 . Assume all capacitors **[10M]**



to be short circuit.

SECTION-V

10 Explain the operation of N-channel enhancement MOSFET and draw its I_D-V_{DS}characteristics. **[10M]**

OR

11 Explain the transfer and drain characteristics of Junction Field Effect Transistor. **[10M]**

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