

Code No: **R17A0401****MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY**

(Autonomous Institution – UGC, Govt. of India)

**II B.Tech I Semester Supplementary Examinations, April 2023****Electronic Devices and Circuits****(EEE, ECE, CSE & IT)**

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**Time: 3 hours****Max. Marks: 70**

**Note:** This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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**SECTION-I**

- 1    **A**    The reverse saturation current of a germanium diode is  $100\mu\text{A}$  at room temperature of  $27^\circ\text{C}$ . Calculate the current in forward biased condition, if forward bias voltage is  $0.2\text{V}$  at room temperature. If temperature is increased by  $20^\circ\text{C}$ , calculate the reverse saturation current and the forward current for same forward voltage at new temperature **[7M]**
- B**    Explain the operation of Zener diode and explain how it act as voltage regulator in detail. **[7M]**

OR

- 2    **A**    (i) Compare Zener and Avalanche break downs **[7M]**  
           (ii) Determine the value of forward current in the case of p-n junction silicon diode with  $I_0 = 10\mu\text{A}$ ,  $V_f = 0.8\text{V}$ ,  $T = 300\text{K}$ .
- B**    Explain in detail about the forward and reverse biased conditions of p-n junction diode and also explain about the estimation of static and dynamic resistances. **[7M]**

**SECTION-II**

- 3    **A**    Derive the expression for the following parameters **[7M]**  
           (i)  $I_{\text{DC}}$  (ii)  $E_{\text{DC}}$  (iii)  $I_{\text{rms}}$  (iv) efficiency (v) ripple factor  
           of a Full-wave-rectifier.
- B**    A  $230\text{V}$ ,  $50\text{Hz}$  voltage is applied to the primary of a 3:1 step down transformer used in a Half wave rectifier having a load of  $10\text{K}\Omega$ . If the diode resistance and the secondary coil resistance are  $75\Omega$  and  $10\Omega$ , determine maximum, average and RMS values of current, DC voltage across the load, efficiency, ripple factor. **[7M]**

OR

- 4    **A**    Derive the expression for the following parameters **[6M]**  
           (i)  $I_{\text{DC}}$  (ii)  $E_{\text{DC}}$  (iii)  $I_{\text{rms}}$  (iv) efficiency (v) ripple factor  
           of a Half Wave rectifier.
- B**    A centre tapped full wave rectifier circuit the RMS half secondary voltage is  $9\text{V}$  assuming ideal diodes and load resistance  $R_L = 1\text{K}\Omega$ . Calculate
- i)    Peak Current **[2M]**  
           ii)    DC load Voltage **[2M]**  
           iii)     $I_{\text{rms}}$  **[2M]**  
           iv)    ripple factor **[2M]**

### SECTION-III

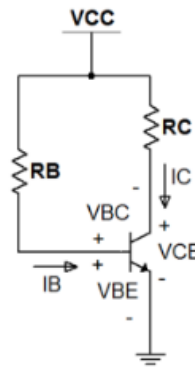
- 5    **A**    For a certain transistor  $I_C = 5.255\text{mA}$ ,  $I_B = 100\text{ }\mu\text{A}$  and  $I_{CBO} = 5\text{ }\mu\text{A}$  [7M]  
          (i) calculate  $\alpha$ ,  $\beta$  and  $I_E$ .  
          (ii) Determine the new level of  $I_B$  required to make  $I_C = 15\text{ mA}$   
**B**    Explain in detail about the operation of Transistor in CB configuration with suitable diagrams . [7M]

OR

- 6    **A**    For a single-stage Transistor Amplifier,  $R_S = 2\text{ k}\Omega$  and  $R_L = 5\text{ k}\Omega$ . The  $h$ -parameter values are  $h_{fb} = 0.98$ ,  $h_{ib} = 21\Omega$ ,  $h_{rb} = 2.9 \times 10^{-4}$  and  $h_{ob} = 0.49\text{ }\mu\text{A/V}$ . Find  $A_I$ ,  $A_V$ ,  $R_i$  and  $R_o$  for CB transistor configuration [7M]  
**B**    Differentiate CB, CE, CC configurations on indicating all parameters necessary and with suitable basic diagrams of configurations. [7M]

### SECTION-IV

- 7    **A**    Define biasing? Draw the Self bias circuit and obtain the expression for the stability factor? [7M]  
**B** [7M]



For circuit shown is subjected to temperature change ; and the value of  $\beta = 100$  at  $25^\circ\text{C}$  and  $\beta = 125$  at  $75^\circ\text{C}$  determine the percentage change in the Q-point values over the temperature range .

OR

- 8    **A**    What is the need for biasing and explain the DC and AC load line analysis for Q- point identification [7M]  
**B**    Design a collector to base bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: [7M]  
 $V_{CC} = 16\text{V}$ ,  $V_{BE} = 0.7\text{V}$ ,  $V_{CEQ} = 8\text{V}$ ,  $I_{CQ} = 4\text{mA}$  &  $\beta = 50$

### SECTION-V

- 9    **A**    Explain the construction and operation of JFET with its characteristics and explain the different regions in VI characteristics? [7M]  
**B**    Analyze the operation of FET with fixed bias and derive the values of Input impedance, output impedance, voltage gain. [7M]

OR

- 10   **A**    Explain the construction & operation of a n-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics? [7M]  
**B**    Compare BJT and FET and list out their advantages and disadvantages. [7M]

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