R18

Code No: R18A0404

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, April 2023

Switching Theory & Logic Design

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	***A***	Perform the following addition using 2's complement of 386+756	**[4M]**
	B	Given the 8bit data word 01010011, generate the 12 bit composite word for the hamming code that corrects and detects single errors	**[10M]**
		OR	
2	***A***	Convert the given expression in standard SOP form f(A,B,C)=AC+BA+BC	**[7M]**
	B	What is the difference between canonical form and standard form? Explain	**[7M]**

SECTION-II

3	***A***	Simplify the following Boolean expressions using K-map and implement it by using NAND gates. F(A,B,C,D)=AB'C' +AC+A'CD'	**[7M]**
	B	Simplify the following Boolean expressions using K-map and implement it by using NAND gates. F(W,X,Y,Z)=w' x'y'z' + wxy'z' + w'x'yz + wxyz	**[7M]**
		OR	
4	***A***	Design BCD to gray code converter and realize using logic gates.	**[7M]**
	B	Design and implement a two bit comparator using logic gates.	**[7M]**

SECTION-III

5	***A***	Draw the logic diagram of a JK flip- flop and using excitation table explain its operation	**[7M]**
	B	Convert D flip-flop into JK flip-flops.	**[7M]**
		OR	
6	***A***	Draw the logic diagram of a SR latch using NOR gates. Explain its Operation using excitation table.	**[7M]**
	B	Explain the working of JK Flipflop. What is race around condition? How is it overcome?	**[7M]**

SECTION-IV

7	***A***	What is a Universal shift register and explain the operation with neat sketch.	**[7M]**
	B	Explain how a shift register is used as a converter from i) serial to parallel data and ii) parallel to serial data	**[7M]**
		OR	
8	***A***	How does ripple counter differ from synchronous counter?	**[7M]**
	B	Design Mod-10 Asynchronous counter.	**[7M]**

SECTION-V

9 **A** Convert the following Mealy machine into equivalent Moore machine. Draw the state transition diagrams for both. **[8M]**

P.S	N.S			
	A		B	
	state	o/p	state	o/p
Q1	Q1	1	Q2	0
Q2	Q4	1	Q4	1
Q3	Q2	1	Q3	1
Q4	Q3	0	Q1	1

B Compare Mealy and Moore Machines **[6M]**

OR

10 ***A*** Explain about state diagrams & state tables **[7M]**

B With the help of State table and State diagram explain the operation of Sequence generator. **[7M]**

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