Code No: **R20A0404**

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, July/August 2023

Digital Logic Design

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	A	Differentiate between combinational and sequential logic circuits.	[7M]
	B	Explain the operation of clocked JK flip flop with the help of truth table.	[7M]
		OR	
2	A	Construct a T flip flop using a SR flip flop and other logic gates.	[7M]
	B	Explain the operation of D flip flop with the help of logic diagram. Also derive its characteristic equation.	[7M]

SECTION-II

3	A	Explain the analysis of sequential circuits in detail with an example.	[7M]
	B	A sequential circuit has two J-K flip-flops A and B and one input X. The circuit is described by the following flip-flop input equations: $J_A = X \quad K_A = B' \quad J_B = X \quad K_B = A$ Derive the state equations A(t+1) and B(t+1) and draw the state diagram of the circuit	[7M]
		OR	
4	A	Draw the logic diagram of 4-bit right shift register using D Flip-flops and explain the operation.	[7M]
	B	Design a 3 bit binary ripple counter and explain its operation.	[7M]

SECTION-III

5	A	Explain the keyword module with an example.	[7M]
	B	Differentiate between synthesis and simulation.	[7M]
		OR	
6	A	What are the levels of abstraction in digital design? Expain with examples.	[7M]
	B	Explain in detail about the operators in Verilog.	[7M]

SECTION-IV

7	A	Write short note on AND and OR gate primitives.	[7M]
	B	Write Verilog code of 4-bit binary adder using full adder module.	[7M]
		OR	
8	A	Write Verilog code and test bench of 4 to 1 multiplexer using ternary operator.	[7M]
	B	Explain continuous assignment structures with examples.	[7M]

SECTION-V

9	A	Explain initial construct with example.	[7M]
	B	Write Verilog code to model ALU.	[7M]
		OR	
10	A	Differentiate between blocking and nonblocking assignments with examples.	[7M]
	B	Design module of up counter and write test bench for the same.	[7M]

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