**R15**

**Code No: R15A0407**

# MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

**(Autonomous Institution – UGC, Govt. of India)**

## II B.Tech II Semester Supplementary Examinations, April 2023

**Switching Theory and Logic Design**

**(ECE)**

| Roll No | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|

**Time: 3 hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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**PART-A (25 Marks)**

| | | |
|---|---|---|
| 1). a | Subtract 111001 from 101011 using 2's complement. | **[2M]** |
| b | Convert the following numbers<br>i) $(41.6875)_{10}$ to binary ii) $(1001001.011)_2$ to decimal<br>iii) Find the 9's Complement of number $(25.639)_{10}$ | **[3M]** |
| c | Draw the logic diagram of 4-bit adder subtractor. | **[2M]** |
| d | What is the importance of prime implicants? | **[3M]** |
| e | Discuss the disadvantages of level triggering | **[2M]** |
| f | Define excitation table. Explain D-flip flop | **[3M]** |
| g | Define State diagram and State assignment. | **[2M]** |
| h | Draw the logic diagram of a 4 - bit binary ripple counter using positive edge triggering. | **[3M]** |
| i | Draw the block diagrams of Mealy and Moore state machines. | **[2M]** |
| j | Discuss limitations of Finite State Machines. | **[3M]** |

**PART-B (50 MARKS)**

**SECTION-I**

| | | |
|---|---|---|
| 2 | Simplify the following Boolean expressions using Boolean algebra:<br>i) AB + AB'C(B'C' + C) + (AC)'<br>ii) A'BC' + A'BC + AB'C' + ABC<br>iii) ABC'D' +ABC'D + ABCD' +ABCD<br>iv) AB + ABC' + A'BC +ABC<br>v) ABCD + ABCD' +A'BCD +A'BCD' | **[10M]** |
| | OR | |
| 3 | Implement the following logical expression using AND-OR-INVERTER gates and also using only NOR gates. A + BC'(D' + BE') | **[10M]** |

**SECTION-II**

| | | |
|---|---|---|
| 4 | Simplify the Boolean function using K-map<br>F (A.B, C, D) = A'B'C'+ B'CD'+ A'BCD'+AB'C' | **[10M]** |
| | OR | |
| 5 | Given F(A,B,C,D)=BC+ABD'+A'C'D. Implement using 8x1 multiplexer. | **[10M]** |

## SECTION-III

| | | |
|---|---|---|
| 6 | Convert SR Flip-Flop to JK Flip-Flop. | **[10M]** |
| | OR | |
| 7 | Define race-around problem and discuss how it is eliminated in JK Master-Slave flip-flop. | **[10M]** |

## SECTION-IV

| | | |
|---|---|---|
| 8 | Design a MOD-8 synchronous counter using T Flip-Flops. | **[10M]** |
| | OR | |
| 9 | Explain the operation of a 4 bit shift register and Johnson counter. | **[10M]** |

## SECTION-V

| | | |
|---|---|---|
| 10 | With an example explain the simplification of incompletely specified machines. | **[10M]** |
| | OR | |
| 11 | Explain the procedure of state minimization using merger graph and merger table. | **[10M]** |

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