R17

Code No: R17A0407

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester Supplementary Examinations, April 2023

Switching Theory and Logic Design

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1 Generate Hamming code for the given 11 bit message 10001110101 and rewrite the entire message with hamming code. **[14M]**

OR

2 Write the decimal numbers 9,6 and 3 in terms of the following weighted binary codes:

a) 4,2,2,1 **[7M]**

b) 8,4,2,1 **[7M]**

SECTION-II

3 a) Prove that AB′C+B+BD′+ABD′+A′C=B+C. **[7M]**

b) Expand minterms and maxterm AB′+ABD′+A+ABC′D **[7M]**

OR

4 a) Simplify the following Boolean expression using K- map and implement them with NOR logic gates F(A,B,C,D)= Σ m (1,3,7,11,15) + d(0,2,5). **[7M]**

b). Explain the Boolean algebra theorems and properties. **[7M]**

SECTION-III

5 What is a full adder? Implement a full adder with multiplexers. **[14M]**

OR

6 a) Realize the expression F=Σm(0,1,3,5,8,11,12,14,15)using 8×1 MUX. **[7M]**

b) What is decoder? Implement 3:8 line decoder **[7M]**

SECTION-IV

7 Explain master slave JK flipflop with neat timing diagram. **[14M]**

OR

8 a) What are the fundamentals of Sequential machine operation? **[7M]**

b) Discuss about binary cell in detail. **[7M]**

SECTION-V

9 Design a synchronous counter to count the sequence 0-1-3-5-6-7 using JK Flip-Flop. **[14M]**

OR

10 a) With a neat block diagram, explain the moore model of a clocked synchronous sequential circuit. **[7M]**

b) Illustrate partition techniques in sequential circuits. **[7M]**

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