R15

Code No: R15A0410

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Supplementary Examinations, April 2023

Digital Design Through Verilog

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART-A (25 Marks)

1). a	Define Verilog HDL.	**[2M]**
b	What is Module?	**[3M]**
c	What is AND gate primitive?	**[2M]**
d	Define strengths and content resolution.	**[3M]**
e	What is initial construct?	**[2M]**
f	Explain force-release construct.	**[3M]**
g	Explain tranif1 and tranif0.	**[2M]**
h	Define module path.	**[3M]**
i	What is capacitive model?	**[2M]**
j	Explain about Testbench?	**[3M]**

PART-B (50 MARKS)

SECTION-I

2	a) Differentiate between synthesis and simulation.	**[5M]**
	b) Explain levels of abstraction in digital design with examples.	**[5M]**
	OR	
3	Explain the following:	
	a) Programming Language interface	**[5M]**
	b) Functional verification	**[5M]**

SECTION-II

4	a) Explain continuous assignments and strengths with example	**[5M]**
	b) Explain delays with continuous assignments	**[5M]**
	OR	
5	a) Write short notes on Tri state gates and delays associated with them.	**[5M]**
	b) Write Verilog code and test bench of 4 to 1 multiplexer using ternary operator.	**[5M]**

SECTION-III

6	a) Write Verilog description of JK flip flop with preset and clear facility.	**[5M]**
	b) Differentiate between blocking and nonblocking assignments with examples.	**[5M]**
	OR	
7	Write Verilog code to model ALU and write the test bench for the same.	**[10M]**

SECTION-IV

8	Explain in detail about Basic switch primitives and resistive switches.	**[10M]**
	OR	
9	Design a half adder module with time delay assignment through parameter declaration and write the test bench for the same.	**[10M]**

SECTION-V

10	Write short notes on sequential models.	**[10M]**
	OR	
11	Differentiate between combinational circuits testing and sequential circuits testing.	**[10M]**

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