R17

Code No: R17A0410

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Supplementary Examinations, April 2023

Digital System Design Through Verilog

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	***A***	Write short notes on (a) Concurrency (b) Simulation (c) Synthesis	**[2M]** **[2M]** **[2M]**
	B	Differentiate the scalars and vectors in verilog modules with examples.	**[8M]**
		OR	
2	***A***	Explain the following operators supported by Verilog HDL with examples. i) Bitwise Operators ii) Equality Operators	**[3M]** **[3M]**
	B	Describe the following levels of design description: Circuit level, Gate level, Data flow, Behavioral level.	**[8M]**

SECTION-II

3	***A***	Discuss about the array of instances and develop the verilog code for a byte comparator with relevant diagram	**[8M]**
	B	Explain about the concurrent statements in data flow level. Give one example to each one.	**[6M]**
		OR	
4	***A***	Write Verilog HDL source code for a data level description of 4 to 1 multiplexer circuit. Draw the relevant logic diagram.	**[7M]**
	B	Design a 4 bit parallel adder in Gate level modeling.	**[7M]**

SECTION-III

5	***A***	Develop a verilog module of the D_FF module with asynchronous active high preset and clear through if- else construct.	**[7M]**
	B	Explain disable construct with an example.	**[7M]**
		OR	
6	***A***	Design a 8:1 Mux using case statement.	**[7M]**
	B	Explain the blocking and non-blocking statements in Verilog with suitable example.	**[7M]**

SECTION-IV

7	***A***	Develop a verilog module for a 2-to-1 multiplexer using tri-state switches.	**[7M]**
	B	Describe the CMOS switches operation in detail.	**[7M]**
		OR	
8	***A***	Prepare a verilog module for a CMOS NOR Gate	**[7M]**

	B	Discuss the regular and resistive switches in detail with primitive keywords and explain how the resistive switches differ from regular switches.	**[7M]**

SECTION-V

9	***A***	Differentiate between combinational and sequential UDPs with suitable example	**[7M]**
	B	Illustrate the path delays with relevant example	**[7M]**

OR

10	***A***	Illustrate the Parameter Declarations and Assignments, design an ALU module with its size declared as a parameter.	**[8M]**
	B	Explain the system tasks with suitable examples	**[6M]**

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