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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
III B.Tech I Semester Supplementary Examinations, April 2023
Linear & Digital IC
(EEE & ECE)

Roll No										

Time: 3 hours   **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I
1	**A**	What are characteristics of ideal Op-Amp? Draw the equivalent circuit of ideal Op-amp.	**[7M]**
	B	Explain the DC characteristics of Op-Amp.	**[7M]**

OR

2	**A**	Draw the inverting amplifier and find its gain. Design an amplifier with gain of -10 and input resistance of 20KΩ.	**[7M]**
	B	Derive the output voltage of a Differential amplifier.	**[7M]**

SECTION-II
3	**A**	What are the characteristics of bandpass and band reject filters?	**[7M]**
	B	Draw the first order Butterworth LPF and find it's Transfer function.	**[7M]**

OR

4	**A**	Draw the block schematic of PLL and describe each block in detail.	**[9M]**
	B	List the applications of PLL.	**[5M]**

SECTION-III
5	**A**	Explain the basic DAC technique. Calculate the values of the LSB, MSB and full scale output of an 8 bit DAC for the 0 to 10V range.	**[7M]**
	B	Illustrate the functioning of Weighted resistor DAC.	**[7M]**

OR

6	**A**	What are the specifications of ADC's? Explain any two.	**[6M]**
	B	Describe the working principle of successive approximation type ADC with an example.	**[8M]**

SECTION-IV
7	**A**	Explain about the classification of Integrated circuits.	**[7M]**
	B	Make differences between two major logic families CMOS and TTL.	**[7M]**

OR

8	**A**	Design 4 bit Binary to Grey code converter	**[7M]**
	B	Draw and explain 3 to 8 line decoder	**[7M]**

SECTION-V
9	**A**	Draw the JK flip-flop and explain it's operation with truth table.	**[7M]**
	B	What is the shift register? What are the different kinds of shift Register? List the applications.	**[7M]**

OR

10	**A**	Design a 3 bit Synchronous counter and explain its operation.	**[7M]**
	B	Describe the RAM Architecture and its functioning.	**[7M]**

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