R20

Code No: R20A0411

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Supplementary Examinations, May/June 2023

Computer Organization & Architecture

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	**A**	With a typical flow chart, explain Floating-Point multiplication.	**[7M]**
	B	Consider a floating-point format with 8-bits for the biased exponent and 23-bits for the significand. Show the bit pattern for the following numbers in this format: i). -720 ii). 0.645.	**[7M]**
		OR	
2	**A**	With the help of a flow chart explain Booth's algorithm for twos complement multiplication.	**[7M]**
	B	With the help of flowchart explain unsigned binary division.	**[7M]**

SECTION-II

3	**A**	What is meant by an instruction cycle? Describe its two phases.	**[7M]**
	B	With the help of diagram explain the functioning of microprogrammed control unit.	**[7M]**
		OR	
4	**A**	What is mean addressing mode?	**[2M]**
	B	Explain direct, indirect, register direct, register indirect, immediate, implicit, relative, index, and base address modes of addressing.	**[12M]**

SECTION-III

5	**A**	Explain how page replacement management is handled in a virtual memory system.	**[7M]**
	B	Discuss the common frame works of memory hierarchy.	**[7M]**
		OR	
6	**A**	Discuss the associative mapping function related to cache memory.	**[7M]**
	B	List and explain the key properties of semiconductor memory.	**[7M]**

SECTION-IV

7	**A**	Draw and explain the architecture of Universal Serial Bus (USB).	**[7M]**
	B	With a typical block diagram, describe the functionality of DMA.	**[7M]**
		OR	
8	**A**	Discuss the following three techniques for input of a block of data with the help of flow diagram:	**[3M]** **[3M]**
		i). Programmed I/O	**[4M]**
		ii). Interrupt-driven I/O	
		iii). DMA	
	B	Differentiate Interrupts and exceptions.	**[4M]**

SECTION-V

9	**A**	Explain with example the concept of shared memory.	**[6M]**
	B	Introduce the basic concepts of parallel processors with the necessary examples.	**[8M]**
		OR	
10	**A**	How is the concept of pipelining implemented effectively in a computer system?	**[4M]**
	B	Explain different pipeline hazards with suitable examples.	**[10M]**

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