R20

Code No: R20A0410

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Supplementary Examinations, May/June 2023

LDIC

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	**A**	Describe the ideal Op-Amp characteristics.	**[7M]**
	B	Discuss the measurement of CMRR and output offset voltage in op-amp	**[7M]**
		OR	
2	**A**	Draw the active integrator circuit and discuss about its frequency response	**[7M]**
	B	Explain the working of Non-Inverting amplifier and derive the equation of its Gain.	**[7M]**

SECTION-II

3	**A**	Derive the expression for the duty cycle of Astable multivibrator using IC 555 with a neat circuit and waveforms	**[7M]**
	B	Design a square wave generator of frequency 100 Hz and duty cycle of 75%	**[7M]**
		OR	
4	**A**	Design a first order wide band reject filter with a higher cut-off frequency of 100 Hz and a lower cut-off frequency of 1 KHz. Calculate the Q-factor of the filter	**[7M]**
	B	Design and explain the operation of All Pass Filter with its characteristics?	**[7M]**

SECTION-III

5	***A***	Design a 4-bit weighted resistor DAC whose full scale output voltage is 10 volts. Assume R_f = 10KΩ, logic '1' level as +5 volts and logic '0' level as 0 volts. What is the output voltage when the input is 1011.	**[7M]**
	B	Draw the block diagram and illustrate the conversion process of the successive approximation A/D Converter	**[7M]**
		OR	
6	***A***	Calculate the conversion time for a full scale input in case of a 12-bit counter type ADC driven by 4 MHz clock	**[6M]**
	B	What are the important observations can be made for dual slope integrating type ADC and draw backs of it.	**[8M]**

SECTION-IV

7	***A***	Design a Priority encoder circuit and which 74XX series IC is used for it.	**[7M]**
	B	Compare TTL and CMOS logic families.	**[7M]**
		OR	
8	***A***	Design a 2-bit magnitude comparator using ICs.	**[7M]**
	B	Design a 4-bit parallel adder/ subtractor circuit.	**[7M]**

SECTION-V

9	***A***	Design a modulo 12 ripple counter using 74×74 IC.	**[7M]**

	B	Design a Serial input and Serial Output shift register with suitable ICs.	**[7M]**
		OR	
10	***A***	How many address and data lines are required to access all the locations of dynamic RAM cell arrays specified below? a) 4M X 4 b) 1M X 1 c) 1M X 4 d) 4M X 1	**[8M]**
	B	Draw the ROM architecture and explain its operation in detail	**[6M]**

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