**R15**

**Code No: R15A0420**

# MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

**(Autonomous Institution – UGC, Govt. of India)**

## IV B.Tech I Semester Supplementary Examinations, April 2023

**VLSI Design**

**(ECE)**

| Roll No | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|

**Time: 3 hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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**PART-A (25 Marks)**

| | | | |
|---|---|---|---|
| 1). a | List the advantages of CMOS process.. | **[2M]** |
| b | Explain pass transistor & Describe figure of merit. | **[3M]** |
| c | Explain different MOS layers. | **[2M]** |
| d | Explain λ- based design rules?. | **[3M]** |
| e | What is fan-in and fan-out?. | **[2M]** |
| f | Define inter layer capacitance.. | **[3M]** |
| g | What are the advantages of PLAs | **[2M]** |
| h | Draw the schematic of 2-bit Array Multiplier.. | **[3M]** |
| i | What is ATPG?. | **[2M]** |
| j | What is Observability and Controllability?. | **[3M]** |

**PART-B (50 MARKS)**

**SECTION-I**

| | | |
|---|---|---|
| 2 | Interpret the Pull-up to pull-down ratio (Zpu/Zpd) for an nMOS inverter driven by another nMOS inverter. | **[10M]** |
| | OR | |
| 3 | Explain different fabrication process of CMOS transistor.. | **[10M]** |

**SECTION-II**

| | | |
|---|---|---|
| 4 | Explain steps in VLSI design flow. | **[10M]** |
| | OR | |
| 5 | Develop a stick diagram and layout for 2-inputs CMOS AND gate. | **[10M]** |

**SECTION-III**

| | | |
|---|---|---|
| 6 | Explain about dynamic CMOS logic and give its advantages and disadvantages.. | **[10M]** |
| | OR | |
| 7 | Discuss about the methods for driving large capacitive loads.. | **[10M]** |

**SECTION-IV**

| | | |
|---|---|---|
| 8 | Design a 4-bitParity generator and draw its logic diagram. | **[10M]** |
| | OR | |
| 9 | Compare simple PLDs, CPLDs and FPGAs | **[10M]** |

**SECTION-V**

| | | |
|---|---|---|
| 10 | Discuss scan-based test techniques. | **[10M]** |
| | OR | |
| 11 | Analyze the issues to be considered while implementing BIST and explain each.. | **[10M]** |

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