R17

Code No: R17A0420

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

IV B.Tech I Semester Supplementary Examinations, April 2023

VLSI Design

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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		SECTION-I	
1	***A***	What are the steps involved in the NMOS fabrication? Explain with neat sketches.	**[7M]**
	B	Discuss various forms of pull-up with neat diagrams.	**[7M]**
		OR	
2	***A***	Derive an equation for transconductance of an n-channel enhancement MOSFET operating in active region..	**[8M]**
	B	Discuss the Basic Electrical Properties of MOS and Bi-CMOS Circuits.	**[6M]**
		SECTION-II	
3	***A***	Draw the flow chart of VLSI Design flow and explain the operation of each step in detail.	**[7M]**
	B	Classify different types of MOS scaling. Derive their effects on various parameters of MOSFET.	**[7M]**
		OR	
4	***A***	Explain about the 2μm CMOS Design rules and discuss with a layout example	**[6M]**
	B	Draw and explain the stick diagram and layout for CMOS 2-input NAND gate.	**[8M]**
		SECTION-III	
5	***A***	What is Gate-level design, explain in detail.	**[8M]**
	B	Calculate on resistance of an inverter from VDD to GND. If n- channel sheet resistance Rsn=104Ω per square and P-channel sheet resistance Rsp = 3.5 × 104 Ω per square. (Zpu=4:4 and Zpd=2:2).	**[6M]**
		OR	
6	***A***	What is inverter delay? How delay is calculated to for multiple stages?	**[7M]**
	B	Discuss about the choice of fan – in and fan – out selection in gate level design	**[7M]**
		SECTION-IV	
7	***A***	Explain Architecture of FPGA in detail.	**[7M]**
	B	Write a note on the different Parameters influencing low power design	**[7M]**
		OR	
8	***A***	Draw the basic block diagram of 4-bit adder and explain its operation in detail.	**[8M]**
	B	What is CPLD? Draw its basic structure and give its applications.	**[6M]**

		SECTION-V	
9	***A***	Explain the following in detail. a) Chip level Test Techniques b) Testability and practices.	**[7M]**
	B	What is ATPG? Explain a method of generation of test vector.	**[7M]**
		OR	
10	***A***	Explain CMOS test principles in detail.	**[7M]**
	B	Draw the basic structure of parallel scan and explain how it reduces the long scan chains.	**[7M]**
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