R18

Code No: R18A0418

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

IV B.Tech I Semester Supplementary Examinations, April 2023

VLSI Design

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION-I

1	***A***	With neat sketches explain the CMOS n-well fabrication process indicating the masks used.	**[7M]**
	B	Discuss various forms of pull-up with neat diagrams.	**[7M]**
		OR	
2	***A***	Derive an equation for I_{DS} Vs V_{DS} of an n-channel Enhancement MOSFET .	**[7M]**
	B	Explain the operations of CMOS inverter in various regions.	**[7M]**
		SECTION-II	
3	***A***	Tabulate the encoding scheme for a simple single metal nMOS process with respect to various MOS layers.	**[7M]**
	B	Explain lambda based design rules of CMOS / BiCMOS	**[7M]**
		OR	
4	***A***	Draw the flow chart of VLSI Design flow and explain the operation of each step in detail.	**[7M]**
	B	What is stick diagram and explain about different symbols used for components in Stick diagram. Draw the stick and layout for a two input CMOS NAND gate.	**[7M]**
		SECTION-III	
5	***A***	Explain dynamic CMOS logic and give its advantages and disadvantages	**[7M]**
	B	Derive the expression for time delay Tsd in case of MOSFET.	**[7M]**
		OR	
6	***A***	Explain clocked CMOS logic and n-p CMOS logic. Mention their advantages and disadvantages.	**[7M]**
	B	Discuss about the choice of fan – in and fan – out selection in gate level design	**[7M]**
		SECTION-IV	
7	***A***	Design a comparator using XNOR gates?	**[7M]**
	B	Write a note on the different Parameters influencing low power design	**[7M]**
		OR	
8	***A***	Draw the basic block diagram of 4-bit adder and explain its operation in detail.	**[8M]**
	B	What is CPLD? Draw its basic structure and give its applications.	**[6M]**
		SECTION-V	
9	***A***	Explain system-level test techniques.	**[7M]**
	B	Explain about memory-self test with the help of a schematic.	**[7M]**

OR

10	***A***	Explain built in self-test technique.	**[7M]**
	B	Explain fault models.	**[7M]**

****