Code No: **R18A0427**

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

IV B.Tech - II Semester Regular/Supplementary Examinations, April 2023

Digital Signal Processors & Architectures

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	***A***	Explain the decimation and interpolation process with an example.	**[7M]**
	B	Illustrate the Dynamic range, Resolution and Precision	**[7M]**
		OR	
2	***A***	Explain how to simulate the impulse responses of FIR and IIR filters	**[8M]**
	B	Illustrate the block diagram of a Digital signal-processing system	**[6M]**

SECTION-II

3	***A***	What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter, with a diagram	**[7M]**
	B	Identify the addressing modes of the operands in each of the following instructions & their operation	**[7M]**
		OR	
4	***A***	Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier	**[8M]**
	B	Explain the features of a program sequencer unit of a programmable DSP with a neat block diagram	**[6M]**

SECTION-III

5	***A***	Describe the multiplier/adder unit of TMS320c54xx processor with a neat block diagram.	**[7M]**
	B	With a block diagram explain the indirect addressing mode of TMS320C54XX processor using dual data memory operand.	**[7M]**
		OR	
6	***A***	Illustrate the On chip peripherals of TMS320C54XX processor	**[7M]**
	B	Draw and explain the functional diagram of the central processing unit of the TMS320C54xx processors	**[7M]**

SECTION-IV

7	***A***	Explain the Base Architecture of ADSP 2100	**[7M]**
	B	Outline how efficient data transfer is achieved with the use of buses in ADSP-2181.	**[7M]**
		OR	
8	***A***	Illustrate the operation of MAC unit with neat block diagram	**[7M]**
	B	Describe in detail the bus architecture of Blackfin processor.	**[7M]**

SECTION-V

9	***A***	Explain the significance of External bus interfacing signals of TMS320C5416	**[7M]**
	B	Explain the memory interface block diagram for the TMS 320 C54xx processor.	**[7M]**

OR

10	***A***	Describe the programmed I/O with a neat diagram	**[8M]**
	B	Write a short notes on Direct Memory Access(DMA)	**[6M]**

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