R18

Code No: R18A0427

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

IV B.Tech - II Semester Advance Supplementary Examinations, June 2023

Digital Signal Processors & Architectures

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	***A***	Explain different number formats with an example	**[7M]**
	B	Outline the sources of errors in DSP implementations	**[7M]**
		OR	
2	***A***	Why signal sampling is required? Explain the sampling process	**[7M]**
	B	List the major architectural features used in DSP system to achieve high speed program execution	**[7M]**

SECTION-II

3	***A***	Compute the indices for an 8-point FFT using Bit reversed Addressing Mode	**[7M]**
	B	Explain the features for external interfacing	**[7M]**
		OR	
4	***A***	With a neat block diagram explain MAC of DSP system.	**[7M]**
	B	Discuss about the data addressing capabilities of programmable DSP devices with examples	**[7M]**

SECTION-III

5	***A***	Compare architectural features of TMS320C25 and DSP6000 fixed point digital signal processors.	**[7M]**
	B	Describe any four data addressing modes of TMS320c54xx processor	**[7M]**
		OR	
6	***A***	Explain pipeline operation of TMS320c54xx processor	**[7M]**
	B	Draw and explain the functional diagram of the barrel shifter of the TMS320C54xx processors	**[7M]**

SECTION-IV

7	***A***	Explain the significant features of ADSP2100	**[7M]**
	B	Discuss about the basic peripherals of Blackfin processor	**[7M]**
		OR	
8		Explain with a neat architecture ADSP 2181	**[14M]**

SECTION-V

9	***A***	Describe DMA with respect to TMS320C54XX processors	**[7M]**
	B	Design an interface to connect a 32Kx16 flash memory to TMS320C5416	**[7M]**
		OR	
10	***A***	What are the classes of interrupts available in the TMS320C54xx processor? How interrupts are handled by C54xx DSP Processors.	**[7M]**
	B	Illustrate the timing sequence of memory access with neat diagram.	**[7M]**

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