

ANALOG CIRCUITS

LECTURE NOTES

(R24A0401)

B.TECH

(II YEAR B.Tech – I SEM)

(2025-26)

Prepared by:

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MALLAREDDY COLLEGE OF ENGINEERING & TECHNOLOGY

Autonomous Institution – UGC, Govt. of India

(Affiliated to JNTU, Hyderabad, Approved by AICTE – Accredited by NBA & NAAC – 'A' Grade – ISO 9001:2008 Certified)
Maisammaguda, Dhulapally (Post Via Hakimpet), Secunderabad – 500100

(R24A0401) ANALOG CIRCUITS

Course Objectives:

1. Learn the concepts of, load line analysis and biasing techniques
2. Learn the concepts of high frequency analysis of transistors.
3. To give understanding of various types of amplifier circuits
4. Learn the concepts of small signal analysis of BJT and FET amplifiers and biasing techniques
5. To familiarize the Concept of feedback in amplifiers so as to differentiate between negative and positive feedback. To design an oscillators at different frequencies.

UNIT – I

BJT Biasing: Transistor Biasing and Stabilization - Operating point, Need for biasing, DC Load line, Biasing - Fixed Bias, Self Bias, Bias Stability, Bias Compensation using Diode. Analysis of Small Signal Low Frequency BJT Amplifiers: Transistor Hybrid model, Analysis of single stage transistor amplifier using h-parameters: voltage gain, current gain, Input Impedance and Output impedance. Comparison of transistor configurations in terms of A_i , R_i , A_v , and R_o .

UNIT -II

BJT Amplifiers-Frequency Response: Frequency response of an amplifier, Analysis at low and High Frequencies, Hybrid- π (π) common emitter transistor model, Derive the hybrid- π model parameters, Millers theorem and it's dual. Multistage Amplifiers: Distortion in amplifiers, Analysis of cascaded BJT amplifier, Darlington pair and derive their input impedance(R_i) and current gain(A_i), coupling schemes-RC coupled amplifier, Transformer coupled amplifier, and Direct coupled Amplifier.

UNIT - III

FET-Biasing and FET Amplifiers: FET biasing: fixed bias and self bias. FET Amplifiers :Analysis of Common source (C.S), Common Drain (C.D) JFET Amplifiers, comparison of performance with BJT Amplifiers, Basic Concepts of MOSFET Amplifiers.

UNIT -IV

FEEDBACK AMPLIFIERS: Concept of Feedback and types, Effects of negative feed back on amplifiers characteristics, voltage series, current series, current shunt, and voltage shunt feedback amplifiers.

UNIT -V

OSCILLATORS: Classification of oscillators, Barkhausen criterion, RC phase Shift oscillator, Wien-bridge oscillator, LC oscillators- Hartley and Colpitts oscillator.

TEXT BOOKS:

1. Jacob Millman, Christos C Halkias -Integrated Electronics, McGraw Hill Education.
2. Robert L. Boylestead, Louis Nashelsky -Electronic Devices and Circuits theory, 11th Edition, 2009, Pearson

REFERENCE BOOKS:

1. David A. Bell – Electronic Devices and Circuits, 5th Edition, Oxford.
2. Adel S. Sedra, Kenneth C. Smith- Microelectronic Circuits-Theory and Applications, Oxford.
3. Chinmoy Saha, Arindam Halder, Debaati Ganguly -Basic Electronics-Principles and Applications,

Course Outcomes:

Upon completing this course, the students will be able to

1. Design the amplifiers with various biasing techniques.
2. Design single stage amplifiers using BJT and FET amplifier
3. Design multistage amplifiers and understand the concepts of High Frequency Analysis of BJT.
4. Utilize the Concepts of negative feedback to improve the stability of Amplifiers and Positive feedback to sustained oscillations and Analysis of oscillators at different frequencies

UNIT-1

TRANSISTOR BIASING AND STABILIZATION

NEED FOR TRANSISTOR BIASING

If the o/p signal must be a faithful reproduction of the i/p signal, the transistor must be operated in active region. That means an operating point has to be established in this region. To establish an operating point (proper values of collector current I_c and collector to emitter voltage V_{CE}) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

There are four conditions to be met by a transistor so that it acts as a faithful amplifier:

- 1) Emitter base junction must be forward biased ($V_{BE}=0.7V$ for Si, $0.2V$ for Ge) and collector base junction must be reverse biased for all levels of i/p signal.
- 2) V_{CE} voltage should not fall below $V_{CE(sat)}$ ($0.3V$ for Si, $0.1V$ for Ge) for any part of the i/p signal. For V_{CE} less than $V_{CE(sat)}$ the collector base junction is not probably reverse biased.
- 3) The value of the signal I_c when no signal is applied should be at least equal to the max. collector current I_c due to signal alone.
- 4) Max. rating of the transistor $I_{c(max)}$, $V_{CE(max)}$ and $P_{D(max)}$ should not be exceeded at any value of i/p signal.

Consider the fig shown in fig 2.12. If operating point is selected at A, A representation condition when no bias is applied to the transistor i.e, $I_c=0$, $V_{CE}=0$. It does not satisfy the above said conditions necessary for faithful amplification.

Point C is too close to $P_{D(max)}$ curve of the transistor. Therefore the o/p voltage swing in the positive direction is limited.

Point B is located in the middle of active region. It will allow both positive and negative half cycles in the o/p signal. It also provides linear gain and larger possible o/p voltages and currents.

Hence operating point for a transistor amplifier is selected to be in the middle of active region.

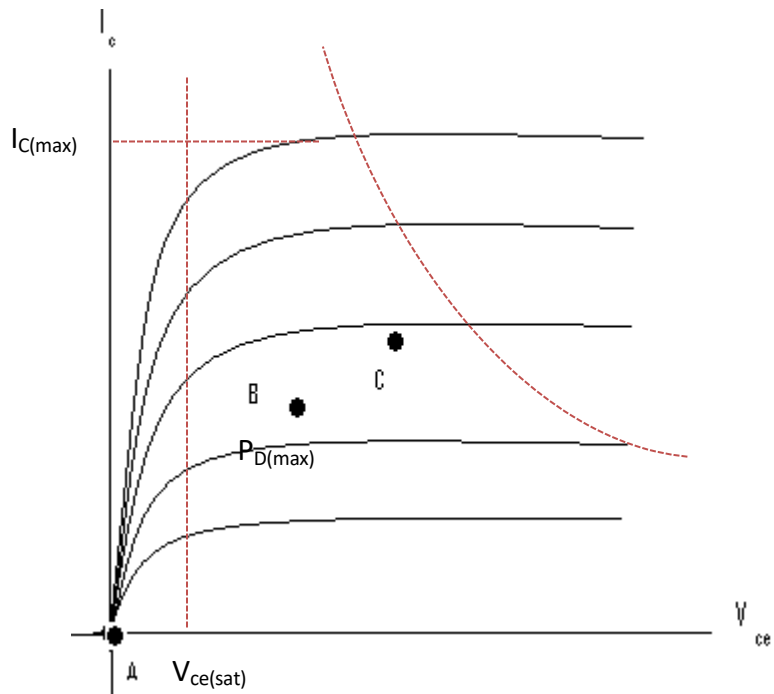


Fig2.12CEOutputCharacteristics

DCLOADLINE

Referring to the biasing circuit of fig 2.13 a, the values of V_{CC} and R_C are fixed and I_C and V_{CE} are dependent on R_B .

Applying Kirchhoff's voltage law to the collector circuit in fig. 2.13, we get

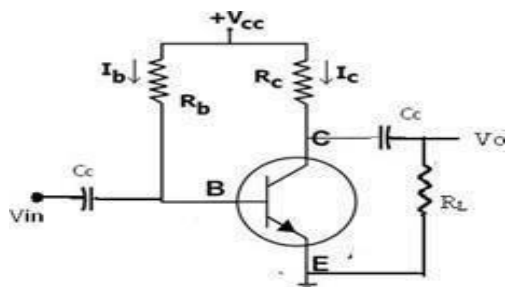
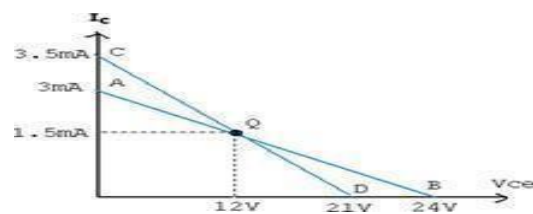


Fig2.13(a)CE Amplifier Circuit (b) Load line

$$V_{CC} = I_C R_C + V_{CE}$$

The straight line represented by AB in fig 2.13b is called the dc load line. The coordinates of the end point A are obtained by substituting $V_{CE}=0$ in the above equation. Then $I_C = \frac{V_{CC}}{R_C}$. Therefore the coordinates of A are $V_{CE}=0$ and $I_C = \frac{V_{CC}}{R_C}$.

The coordinates of B are obtained by substituting $I_C=0$ in the above equation. Then $V_{CE} = V_{CC}$. Therefore the coordinates of B are $V_{CE}=V_{CC}$ and $I_C=0$. Thus the dc load line AB can be drawn if the values of R_C and V_{CC} are known.

As shown in the fig 2.13b, the optimum POINT IS LOCATED AT THE MID POINT OF THE MIDWAY BETWEEN a AND b. In order to get faithful amplification, the Q point must be well within the active region of the transistor.

Even though the Q point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q point shifts nearer to either A or B, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

- 1) Reverse saturation current, I_{CO} , which doubles for every 10°C rise in temperature
- 2) Base emitter Voltage, V_{BE} , which decreases by 2.5mV per $^\circ\text{C}$
- 3) Transistor current gain, h_{FE} or β which increases with temperature.

If base current I_B is kept constant since I_B is approximately equal to V_{CC}/R_B . If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current I_C for a given I_B . Hence, in the o/p characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completely unsatisfactory.

AC LOADLINE

After drawing the dc load line, the operating point Q is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence the ac load line should also pass through the operating point Q. The effective ac load resistance R_{ac} , is a combination of R_C parallel to R_L , i.e. $R_{ac} = R_L || R_C$. So the slope of the ac load line CQD will be $\left(\frac{-1}{R_{ac}}\right)$. To draw the ac load line, two end points, i.e. $V_{CE(\max)}$ and $I_{C(\max)}$ when the signal is applied are required.

$V_{CE(\max)} = V_{CEQ} + I_{CQ} R_{ac}$, which locates point D on the V_{CE} axis.

$I_{C(\max)} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, which locates the point C on the I_C axis.

By joining point sc and D, a load line CD is constructed. As $R_C > R_{ac}$, The dc load line is less steep than ac load line.

STABILITY FACTOR(S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current I_{co} . So, I_C also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which I_C is stabilized with varying I_{co} is measured by stability factor S

$$S = \frac{\partial I_C}{\partial I_{co}} \approx \frac{dI_C}{dI_{co}} \approx \frac{\Delta I_C}{\Delta I_{co}}, \beta \text{ and } I_B \text{ constant}$$

$$\text{For CE configuration } I_C = \beta I_B + (1 + \beta) I_{co}$$

Differentiate the above equation w.r.t. I_C , We get

$$1 = \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{dI_{co}}{dI_C}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta + 1)}{S}$$

$$\therefore S = \frac{1 + \beta}{1 - \beta \frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'':

S' is defined as the rate of change of I_C with V_{BE} , keeping I_{co} and V_{BE} constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

S'' is defined as the rate of change of I_C with β , keeping I_{co} and V_{BE} constant.

$$S'' = \frac{\partial I_C}{\partial \beta}$$

METHODS OF TRANSISTOR BIASING

1) Fixed bias(base bias)

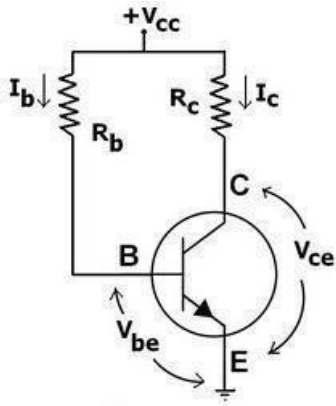


Fig2.14 Fixed Biasing Circuit

This form of biasing is also called *base bias*. In the fig 4.3 shown, the single power source (for example, battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit, V_{cc}

$$= I_B R_B + V_{be}$$

$$\text{Therefore, } I_B = (V_{cc} - V_{be}) / R_B$$

Since the equation is independent of current I_C , $dI_B / dI_C = 0$ and the stability factor is given by the equation..... reduces to

$$S = 1 + \beta$$

Since β is a large quantity, this is a very poor biasing circuit. Therefore in practice the circuit is not used for biasing.

For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of fixed value, on selection of R the base current I_B is fixed. Therefore this type is called *fixed bias* type of circuit. Also for given circuit, $V_{cc} = I_C R_C + V_{ce}$

Therefore, $V_{ce} = V_{cc} - I_C R_C$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gain of the stage.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.

2) EMITTER-FEEDBACK BIAS:

The emitter feedback bias circuit is shown in the fig 2.15. The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point. From Kirchhoff's voltage law, the voltage across the base resistor is

$$V_{Rb} = V_{CC} - I_E R_E - V_{be}$$

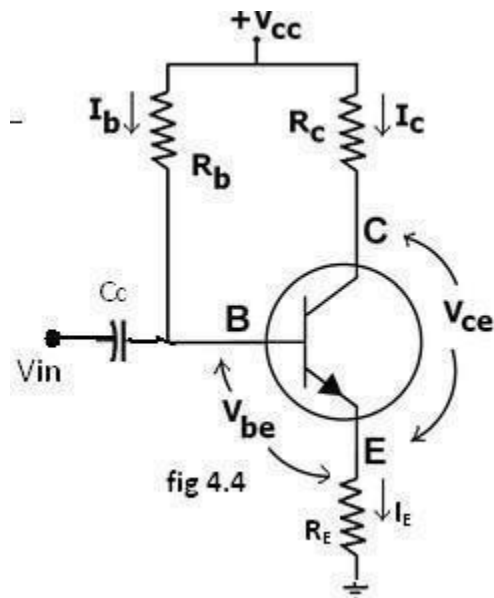


Fig2.15 Self Biasing Circuit

From Ohm's law, the base current is

$$I_b = V_{Rb} / R_b.$$

The way feedback controls the bias point is as follows. If V_{be} is held constant and temperature increases, emitter current increases. However, a larger I_e increases the emitter voltage $V_e = I_e R_e$, which in turn reduces the voltage V_{Rb} across the base resistor. A lower base-resistor voltage drop reduces the base current, which results in less collector current because $I_c = \beta I_b$. Collector current and emitter current are related by $I_c = \alpha I_e$ with $\alpha \approx 1$, so increase in emitter current with temperature is opposed, and operating point is kept stable.

Similarly, if the transistor is replaced by another, there may be a change in I_c (corresponding to change in β -value, for example). By similar process as above, the change is negated and operating point kept stable.

For the given circuit,

$$I_B = (V_{CC} - V_{be}) / (R_B + (\beta + 1)R_E).$$

Merits:

The circuit has the tendency to stabilize operating point against changes in temperature and β -value.

Demerits:

- In this circuit, to keep I_c independent of β the following condition must be met:

$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{be})}{R_B + (\beta + 1)R_E} \approx \frac{(V_{CC} - V_{be})}{R_E}$$

which is approximately the case if $(\beta + 1)R_E \gg R_B$.

- As β -value is fixed for a given transistor, this relation can be satisfied either by keeping R_E very large, or making R_B very low.
- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
- If R_B is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.
- In addition to the above, R_E causes a feedback which reduces the voltage gain of the amplifier.

3) COLLECTOR TO BASE BIAS OR COLLECTOR FEED-BACK BIAS:

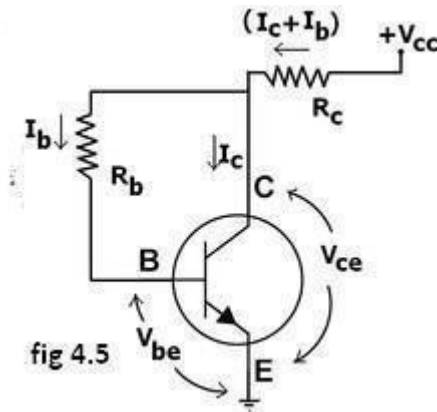


Fig2.16 CollectortoBaseBiasingCircuit

This configuration shown in fig2.16 employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_b is connected to the collector instead of connecting it to the DC source V_{cc} . So any thermal runaway will induce a voltage drop across the R_c resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage V_{R_b} across the base resistor R_b is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers-Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If V_{be} is held constant and temperature increases, then the collector current I_c increases. However, a larger I_c causes the voltage drop across resistor R_c to increase, which in turn reduces the

voltage V_{R_b} across the base resistor R_b . A lower base-resistor voltage drop reduces the base current I_b , which results in less collector current I_c . Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

- In this circuit, to keep I_c independent of β , the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

$$\beta R_c \gg R_b.$$

- As β -value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_c fairly large or making R_b very low.
- If R_c is large, a high V_{cc} is necessary, which increases cost as well as precautions necessary while handling.
- If R_b is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor R_b causes an AC feedback, reducing the [voltage gain](#) of the amplifier. This undesirable effect is a trade-off for greater [Q-point](#) stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

4) COLLECTOR–EMITTERFEEDBACKBIAS:

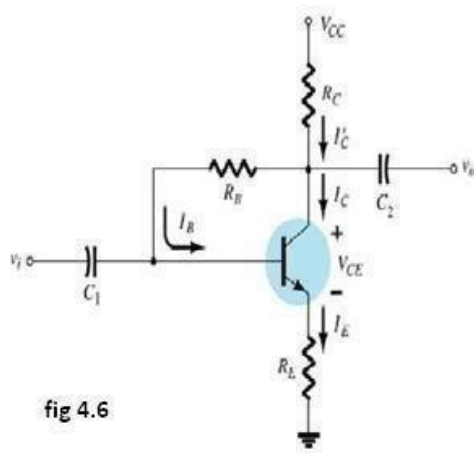


Fig2.17Collector-EmitterBiasingCircuit

The above fig 2.17 shows the collector –emitter feedback bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here the collector feedback is provided by connecting a resistance R_B from the collector to the base and emitter feedback is provided by connecting an emitter R_E from emitter to ground. Both feed backs are used to control collector current and base current I_B in the opposite direction to increase the stability as compared to the previous biasing circuits.

5) VOLTAGE DIVIDER BIAS OR SELF BIAS OR EMITTER BIAS

The voltage divider as shown in the fig 2.18 is formed using external resistors R_1 and R_2 . The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2 , the operating point of the transistor can be made independent of β . In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

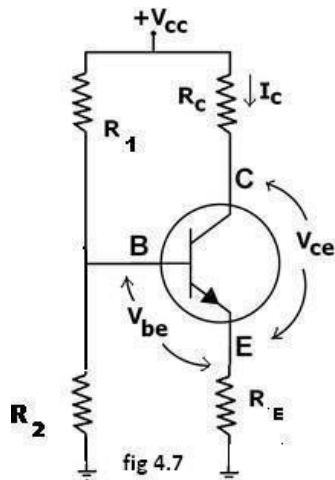


Fig2.18VoltageDividerBiasingCircuit

Inthiscircuitthebasevoltageisgivenby:

$$V_B = \text{voltage across } R_2 = V_{cc} \frac{R_2}{(R_1 + R_2)} - I_B \frac{R_1 R_2}{(R_1 + R_2)}$$

$$\approx V_{cc} \frac{R_2}{(R_1 + R_2)} \text{ provided } I_B \ll I_2 = V_B / R_2.$$

$$\text{Also } V_B = V_{be} + I_E R_E$$

For the given circuit,

$$I_B = \frac{\frac{V_{CC}}{1 + R_1/R_2} - V_{be}}{(\beta + 1)R_E + R_1 \parallel R_2}.$$

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$V_2 = \frac{V_{CC}}{R_1 + R_2} \cdot R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_F}$$

$$I_C = \frac{V_2 - V_{BE}}{R_F} \quad \because I_C \cong I_E$$

$$I_C = \frac{\frac{V_{CC}}{R_1 + R_2} \cdot R_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of β thus the stability is excellent. In all practical cases the value of V_{BE} is quite small in comparison to the V_2 , so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellent stability.

Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\because I_C \cong I_E$$

$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The resistor R_E provides stability to the circuit. If the current through the collector rises, the voltage across the resistor R_E also rises. This will cause V_{CE} to increase as the voltage V_2 is independent of collector current. This decreases the base current, thus collector current increases to its former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1 + \beta)(R_{eq} + R_E)}{R_{eq} + R_E(1 + \beta)}$$

$$R_{eq} = R_1 || R_2$$

$$S = \frac{(1 + \beta) \left(1 + \frac{R_{eq}}{R_E} \right)}{\frac{R_{eq}}{R_E} + 1 + \beta}$$

If R_{eq}/R_E is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1 + \beta}{1 + \beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since R_{eq}/R_E cannot be ignored as compared to 1.

Merits:

- Unlike above circuits, only one dc supply is necessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1 + R_1/R_2} - V_{be}}{(\beta + 1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1 + R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if $(\beta + 1)R_E \gg R_1 \parallel R_2$

where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

- As β -value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making $R_1 \parallel R_2$ very low.
- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
- If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises V_B closer to V_C , reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R_2 lowers V_{be} , reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
- AC as well as DC feedback is caused by R_E , which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

BIAS COMPENSATION USING DIODE AND TRANSISTOR

The various biasing circuits considered use some type of negative feedback to stabilize the operation point. Also, diodes, thermistors and sensistors can be used to compensate for variations in current.

DIODE COMPENSATION:

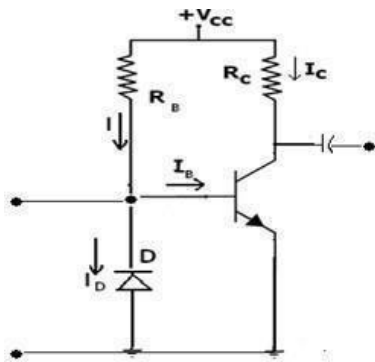


Fig2.19 Diode Compensation Circuit

The following fig 2.19 shows a transistor amplifier with a diode D connected across the base-emitter junction for compensation of change in collector saturation current I_{CO} . The diode is of the same material as the transistor and it is reverse biased by the emitter-base junction voltage V_{BE} , allowing the diode reverse saturation current I_D to flow through diode D . The base current $I_B = I - I_D$.

As long as temperature is constant, diode D operates as a resistor. As the temperature increases, I_{CO} of the transistor increases. Hence, to compensate for this, the base current I_B should be decreased.

The increase in temperature will also cause the leakage current I_D through D to increase and thereby decrease the base current I_B . This is the required action to keep I_C constant.

This type of bias compensation does not need a change in I_C to effect the change in I_C , as both I_D and I_{CO} can track almost equally according to the change in temperature.

THERMISTOR COMPENSATION:

The following fig 2.20 a thermistor R_T , having a negative temperature coefficient is connected in parallel with R_2 . The resistance of thermistor decreases exponentially with increase of temperature. An increase of temperature will decrease the base voltage V_{BE} , reducing I_B and I_C .

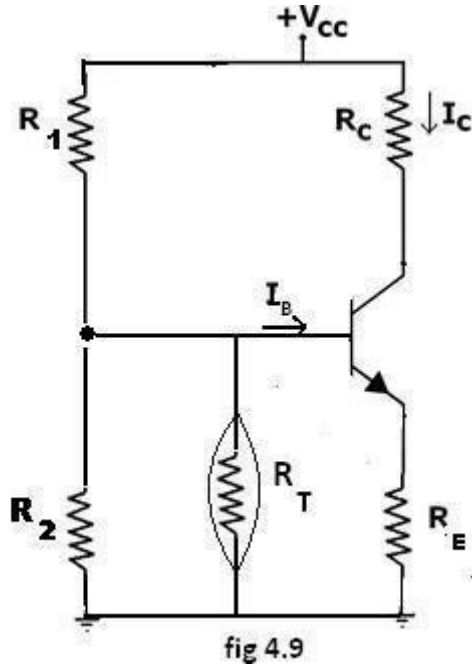


Fig2.20ThermistorCompensation

SENSISTORCOMPENSATION:

In the following fig2.21 shown a sensistor R_s having a positive temperature coefficient is connected across R_1 or R_E . R_s increases with temperature. As the temperature increases, the equivalent resistance of the parallel combination of R_1 and R_s also increases and hence V_{BE} decreases, reducing I_B and I_C . This reduced I_C compensates for increased I_C caused by the increase in V_{BE} , I_{CO} and β due to temperature.

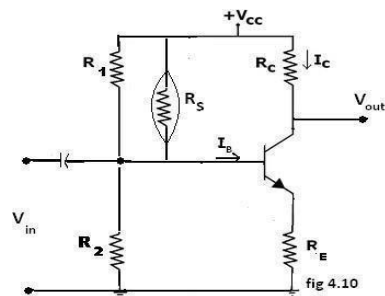


Fig2.21SensistorCompensation

BJT Hybrid Model and Transistor Amplifier

BJT Hybrid Model and Transistor Amplifier's s-parameter representation of a transistor, Conversion of h-parameters, Analysis of single stage transistor amplifier using H-parameters: voltage gain, current gain, Input impedance and Output impedance. Comparison of transistor configurations in terms of A_i , R_i , A_v , and R_o ,

BJT HYBRID MODEL

Small signal low frequency transistor Models:

All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in **fig. 1**.

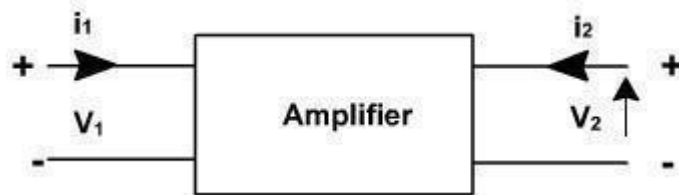


Fig.3.1: Transistor as a two port Network

A two-port network is represented by four external variables: voltage V_1 and current I_1 at the input port, and voltage V_2 and current I_2 at the output port, so that the two-port network can be treated as a black box modeled by the relationships between the four variables, V_1, V_2, I_1, I_2 . Out of four variables two can be selected as are independent variables and two are dependent variables. The dependent variables can be expressed in terms of independent variables. This leads to various two port parameters out of which the following three are important:

1. Impedance parameters (z-parameters)
2. Admittance parameters (y-parameters)
3. Hybrid parameters (h-parameters)

z-parameters

A two-port network can be described by z-parameters as

$$\begin{aligned}V_1 &= Z_{11}I_1 + Z_{12}I_2 \\V_2 &= Z_{21}I_1 + Z_{22}I_2\end{aligned}$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Where

$$z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0}$$

Input impedance with output port open circuited

$$z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1=0}$$

Reverse transfer impedance with input port open circuited

$$z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2=0}$$

Forward transfer impedance with output port open circuited

$$z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1=0}$$

Output impedance with input port open circuited

Y-parameters

A two-port network can be described by Y-parameters as

$$\begin{aligned}I_1 &= Y_{11}V_1 + Y_{12}V_2 \\I_2 &= Y_{21}V_1 + Y_{22}V_2\end{aligned}$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0}$$

Input admittance with output port shortcircuited

$$y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0}$$

Reverse transfer admittance with input port shortcircuited

$$y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0}$$

Forward transfer admittance with output port shortcircuited

$$y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0}$$

Output admittance with input port shortcircuited

Hybrid parameters (h-parameters)

If the input current I_1 and output voltage V_2 are taken as independent variables, the dependent variables V_1 and I_2 can be written as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Where $h_{11}, h_{12}, h_{21}, h_{22}$ are called as hybrid parameters.

$$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0}$$

Input impedance with output port shortcircuited

$$h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0}$$

Reverse voltage transfer ratio with i/p port open circuited

$$h_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0}$$

Forward voltage transfer ratio with o/p port short circuited

$$h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0}$$

output impedance with i/p port open circuited

THE HYBRID MODEL FOR TWO PORT NETWORK:

Based on the definition of hybrid parameters the mathematical model for two port network known as h-parameter model can be developed. The hybrid equations can be written as:

$$V_1 = h_i I_1 + h_r V_2$$

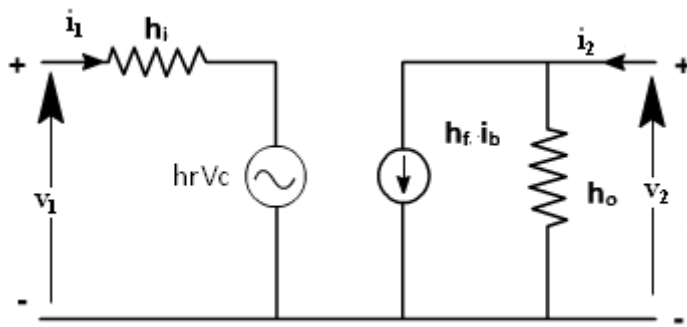
$$I_2 = h_f I_1 + h_o V_2$$

(The following convenient alternative subscript notation is recommended by the IEEE Standards:

i=11=input **o=22=output**

f=21=forward transfer **r=12=reverse transfer**)

We may now use the four h parameters to construct a mathematical model of the device of Fig.(1). The hybrid circuit for any device indicated in Fig.(2). We can verify that the model of Fig.(2) satisfies above equations by writing Kirchhoff's voltage and current laws for input and output ports.



If these parameters are specified for a particular configuration, then suffixes e, b, or c are also included, e.g. h_{fe} , h_{ib} are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in [fig.3.2](#).

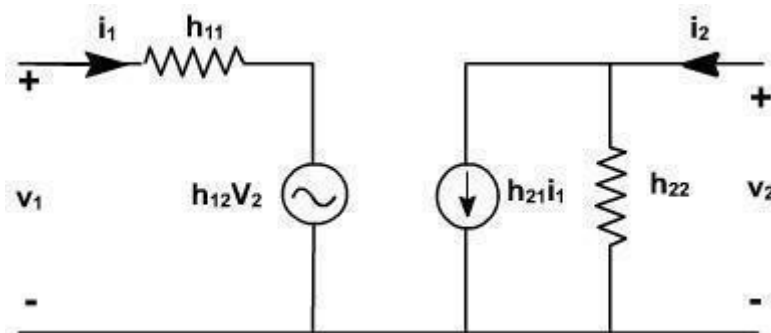


Fig.3.2:-h-parameter equivalent of Transistor

TRANSISTOR HYBRID MODEL:

The hybrid model for a transistor amplifier can be derived as follows:

Let us consider CE configuration as shown in [fig.3.3](#). The variables, i_B , i_C , v_C , and v_B represent total instantaneous currents and voltages. i_B and v_C can be taken as independent variables and v_B , i_C as dependent variables.

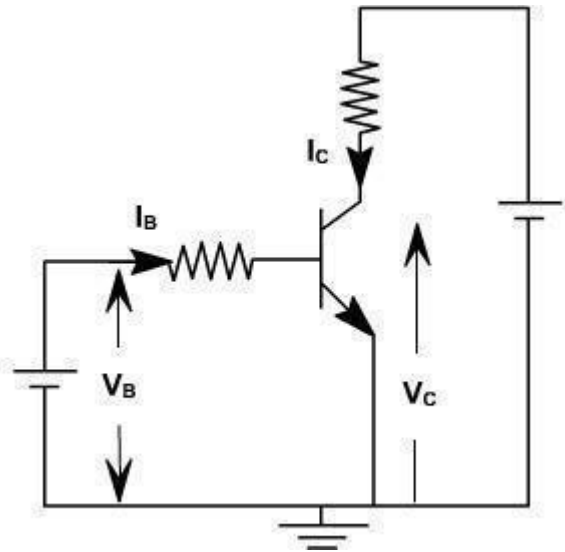


Fig.3.3CE Transistor Amplifier V_B

$$= f_1(i_B, V_C)$$

$$I_C = f_2(i_B, V_C).$$

Using Taylor's series expression, and neglecting higher order terms we obtain.

$$\Delta v_B = \left. \frac{\partial f_1}{\partial i_B} \right|_{V_C} \Delta i_B + \left. \frac{\partial f_1}{\partial V_C} \right|_{i_B} \Delta V_C$$

$$\Delta i_C = \left. \frac{\partial f_2}{\partial i_B} \right|_{V_C} \Delta i_B + \left. \frac{\partial f_2}{\partial V_C} \right|_{i_B} \Delta V_C$$

The partial derivatives are taken keeping the collector voltage or base current constant. The $\Delta v_B, \Delta V_C, \Delta i_B, \Delta i_C$ represent the small signal (incremental) base and collector current and voltage and can be represented as v_B, i_C, i_B, V_C

$$\therefore v_B = h_{ie} i_B + h_{re} V_C$$

$$i_C = h_{fe} i_B + h_{oe} V_C$$

where

$$h_{ie} = \left. \frac{\partial f_1}{\partial i_B} \right|_{V_C} = \left. \frac{\partial v_B}{\partial i_B} \right|_{V_C}; \quad h_{re} = \left. \frac{\partial f_1}{\partial V_C} \right|_{i_B} = \left. \frac{\partial v_B}{\partial V_C} \right|_{i_B}$$

$$h_{fe} = \left. \frac{\partial f_2}{\partial i_B} \right|_{V_C} = \left. \frac{\partial i_C}{\partial i_B} \right|_{V_C}; \quad h_{oe} = \left. \frac{\partial f_2}{\partial V_C} \right|_{i_B} = \left. \frac{\partial i_C}{\partial V_C} \right|_{i_B}$$

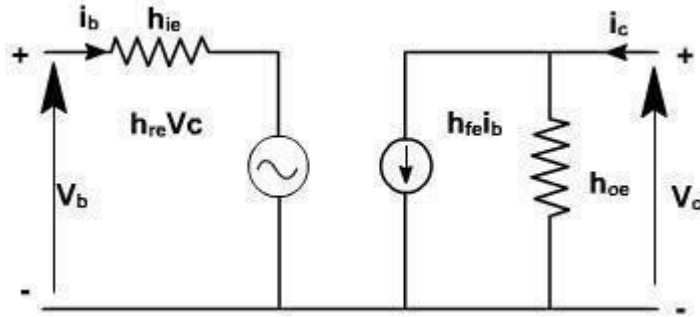


Fig.3.4:h-parameter model of CE Configuration

To determine the four h-parameters of transistor amplifier, input and output characteristics are used. Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter. The output characteristic depicts the relationship between output voltage and output current with input current as parameter. Fig. 5, shows the output characteristics of CE amplifier.

$$h_{fe} = \left. \frac{\partial i_c}{\partial i_b} \right|_{V_c} = \frac{i_{c2} - i_{c1}}{i_{b2} - i_{b1}}$$

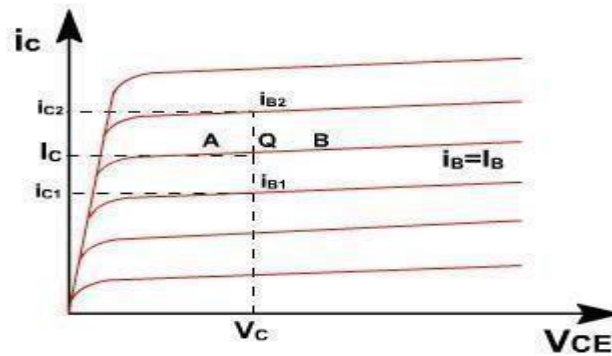


Fig.3.5 Transistor CE Configuration output characteristics

The current increments are taken around the quiescent point Q which corresponds to $i_B = I_B$ and to the collector voltage $V_{CE} = V_C$

$$h_{oe} = \left. \frac{\partial i_c}{\partial V_c} \right|_{i_B}$$

The value of h_{oe} at the quiescent operating point is given by the slope of the output characteristic at the operating point (i.e. slope of tangent AB).

$$h_{ie} = \frac{\partial V_B}{\partial i_B} \approx \left. \frac{\Delta V_B}{\Delta i_B} \right|_{V_c}$$

h_{ie} is the slope of the appropriate input on [fig.3.6](#), at the operating point (slope of tangent EF at Q).

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \left. \frac{\Delta V_B}{\Delta V_C} \right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

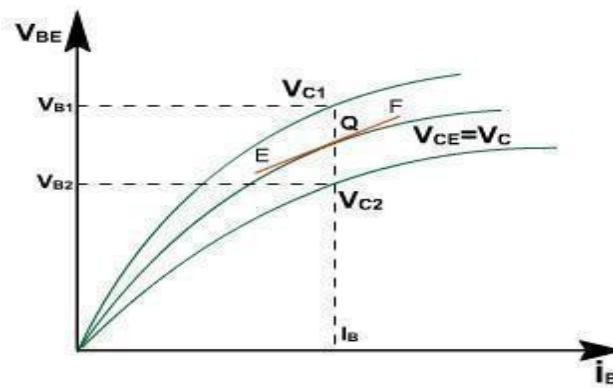


Fig.3.6 Calculation of h-parameters from output characteristics

A vertical line on the input characteristic represents constant base current. The parameter h_{re} can be obtained from the ratio $(V_{B2} - V_{B1})$ and $(V_{C2} - V_{C1})$ for at Q.

Typical CE h-parameters of transistor 2N1573 are given below:

$$h_{ie} = 1000 \Omega$$

$$h_{re} = 2.5 \times 10^{-4}$$

$$h_{fe} = 50$$

$$h_{oe} = 25 \mu A/V$$

ANALYSIS OF A TRANSISTOR AMPLIFIER USING h-PARAMETERS:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in [fig. 3.7](#) and to bias the transistor properly.

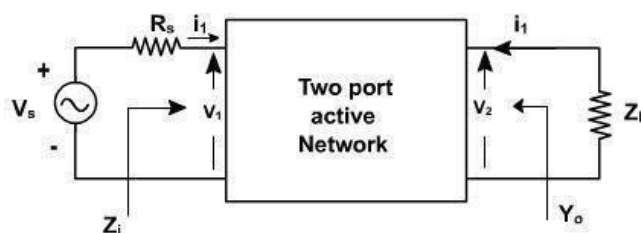


Fig.3.7 Transistor two port Network

Consider the two-port network of CE amplifier. R_S is the source resistance and Z_L is the load impedance. h-parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in fig. 2. (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedance, voltage gain, and output impedance.

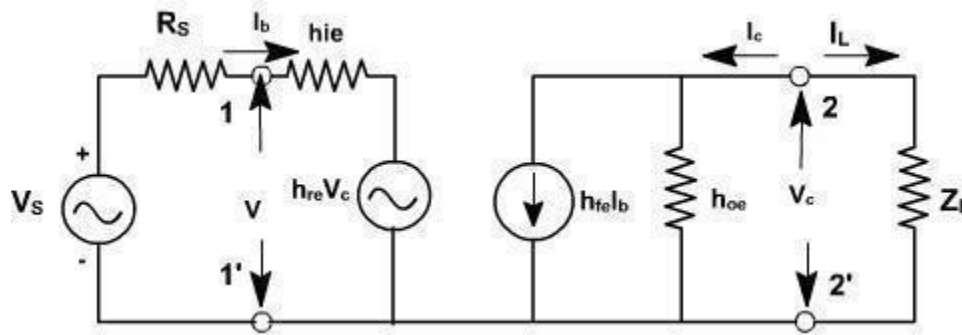


Fig3.8:hparameter equivalent of Transistor in CE configuration

Current gain:

For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_i = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

Input impedance:

The impedance looking into the amplifier input terminals (1, 1') is the input impedance Z_i

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_i Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \quad \left(\text{since } Y_L = \frac{1}{Z_L} \right)$$

Voltage gain:

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_c}{V_b} = - \frac{I_c Z_L}{V_b}$$
$$\therefore A_v = \frac{I_b A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

Output Admittance:

$$Y_0 = \left. \frac{I_c}{V_c} \right|_{V_s=0} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe} \frac{I_b}{V_c} + h_{oe}$$

$$\text{when } V_s = 0, \quad R_s I_b + h_{ie} I_b + h_{re} V_c = 0.$$

$$\frac{I_b}{V_c} = - \frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}$$

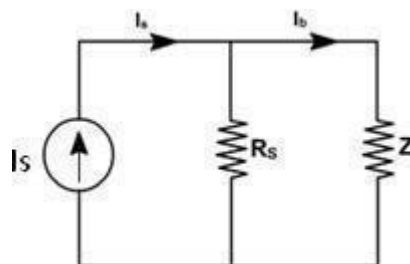
Voltage amplification taking into account source impedance (R_s) is given by

$$A_{vs} = \frac{V_c}{V_s} = \frac{V_c}{V_b} \times \frac{V_b}{V_s} \quad \left(V_b = \frac{V_s}{R_s + Z_i} \times Z_i \right)$$
$$= A_v \cdot \frac{Z_i}{Z_i + R_s}$$
$$= \frac{A_i Z_L}{Z_i + R_s}$$

It is defined as

A_v is the voltage gain for an ideal voltage source ($R_s = 0$).

Consider input source to be a current source I_s in parallel with a resistance R_s as shown in [fig.3](#).



In this case, overall current gain A_{is} is defined as

$$\begin{aligned}
 A_{I_s} &= \frac{I_L}{I_s} \\
 &= -\frac{I_c}{I_s} \\
 &= -\frac{I_c}{I_b} \cdot \frac{I_b}{I_s} \quad \left(I_b = \frac{I_s \cdot R_s}{R_s + Z_i} \right) \\
 &= A_I \cdot \frac{R_s}{R_s + Z_i}
 \end{aligned}$$

If $R_s \rightarrow \infty$, $A_{I_s} \rightarrow A_I$

h-parameters

To analyze multistage amplifier the h-parameters of the transistor used are obtained from manufacture datasheet. The manufacture datasheet usually provides h-parameter in CE configuration. These parameters may be converted into CC and CB values. For example [fig. 4](#) hrc in terms of CE parameter can be obtained as follows.

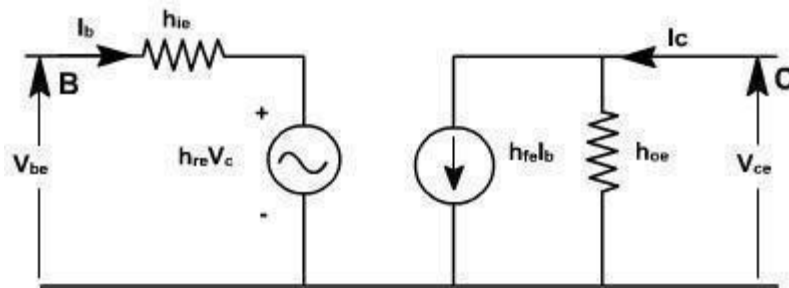


Fig.3.9 CE h-parameter model

For CE transistor configuration V_{be}

$$= h_{ie} I_b + h_{re} V_{ce}$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce}$$

The circuit can be redrawn like CC transistor configuration as shown in [fig.5](#). $V_{bc} =$

$$h_{ie} I_b + h_{rc} V_{ec}$$

$$I_c = h_{fe} I_b + h_{oe} V_{ec}$$

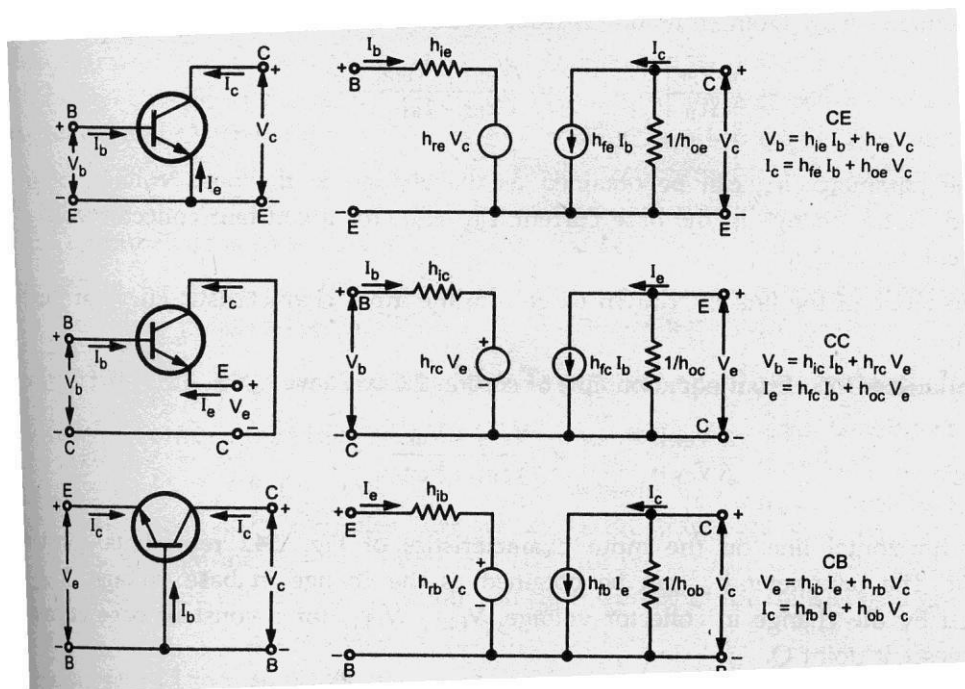


Fig3.10 hybrid model for transistor in three different configurations

Typical h-parameter values for a transistor

Parameter	CE	CC	CB
h_i	1100 Ω	1100 Ω	22 Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	-51	-0.98
h_o	25 $\mu A/V$	25 $\mu A/V$	0.49 $\mu A/V$

Analysis of a Transistor amplifier circuit using h-parameters

A transistor amplifier can be constructed by connecting an external load and signal source and biasing the transistor properly.

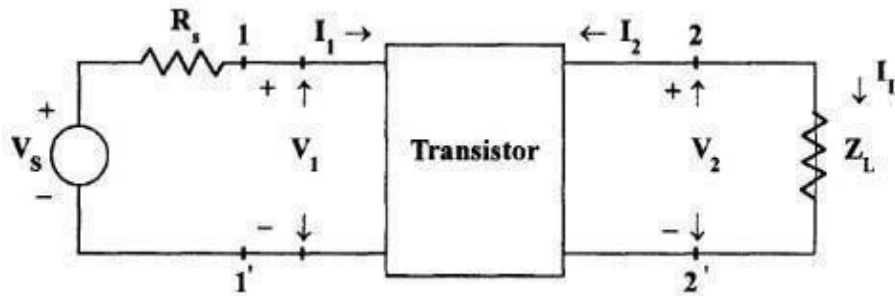


Fig.3.11 Basic Amplifier Circuit

The two port network of Fig. 3.11 represents a transistor in any one of its configuration. It is assumed that h -parameters remain constant over the operating range. The input is sinusoidal and I_1, V_1 and V_2 are phase quantities

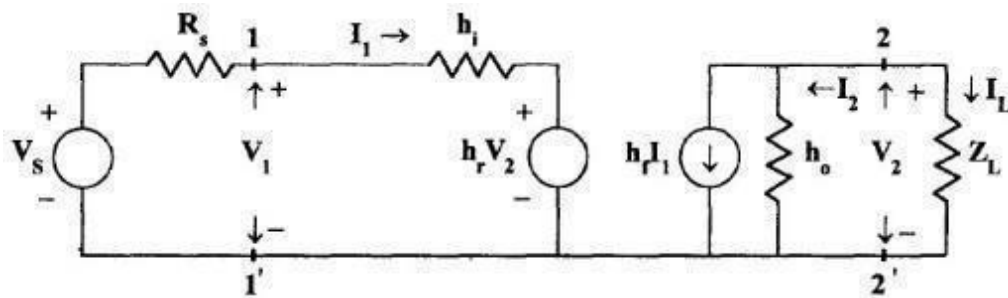


Fig.3.12 Transistor replaced by its Hybrid Model

Current Gain or Current Amplification (A_i)

For transistor amplifier the current gain A_i is defined as the ratio of output current to input current, i.e.,

$$A_i = I_2 / I_1 = -I_2 / I_1$$

From the circuit of Fig

$$I_2 = h_f I_1 +$$

$$h_o V_2$$

$$V_2 = I_2 Z_L = -I_2 Z_L$$

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$$I_2 + I_2 Z_L h_o = h_f$$

$$I_1 I_2 (1 + Z_L h_o) = h_f I_1$$

$$A_i = -I_2 / I_1 = -h_f / (1 + Z_L h_o) \text{ Therefore,}$$

$$A_i = -h_f / (1 + Z_L h_o)$$

Input Impedance (Z_i)

In the circuit of Fig , R_s is the signal source resistance. The impedance seen when looking into the amplifier terminals (1,1') is the amplifier input impedance Z_i ,

$$Z_i = V_1 / I_1$$

From the input circuit of Fig $V_1 = h_i I_1 + h_r V_2$ $Z_i =$

$$(h_i I_1 + h_r V_2) / I_1$$

$$= h_i + h_r V_2 / I_1 \text{ Substituting}$$

$$V_2 = -I_2 Z_L = A_i I_1 Z_L$$

$$Z_i = h_i + h_r A_i I_1 Z_L / I_1$$

$$= h_i + h_r$$

$$A_i Z_L \text{ Substituting}$$

$$\text{or } A_i$$

$$Z_i = h_i - h_f h_r Z_L / (1 + h_o Z_L)$$

$$= h_i - h_f h_r Z_L / Z_L (1/Z_L + h_o)$$

Taking the Load admittance as $Y_L = 1/Z_L$ $Z_i =$

$$h_i - h_f h_r / (Y_L + h_o)$$

Voltage Gain or Voltage Gain Amplification Factor (A_v)

The ratio of output voltage V_2 to input voltage V_1 gives the voltage gain of the transistor i.e.,

$$A_v = V_2 / V_1$$

Substituting

$$V_2 = -I_2 Z_L = A_{11} I_1 Z_L$$

$$A_v = A_{11} I_1 Z_L / V_1 = A_{11} Z_L / Z_i$$

Output Admittance (Y_o)

Y_o is obtained by setting V_s to zero, Z_L to infinity and by driving the output terminals from a generator V_2 . If the current V_2 is I_2 then $Y_o = I_2 / V_2$ with $V_s = 0$ and $R_L = \infty$.

From the circuit of fig

$$I_2 = h_f I_1 + h_o V_2 \text{ Dividing}$$

by V_2 ,

$$I_2 / V_2 = h_f I_1 / V_2 + h_o$$

With $V_2 = 0$, by KVL in input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0 \quad (R_s$$

$$+ h_i) I_1 + h_r V_2 = 0$$

$$\text{Hence, } I_2 / V_2 = -h_r / (R_s + h_i)$$

$$= h_f (-h_r / (R_s + h_i)) + h_o = h_o -$$

$$h_f h_r / (R_s + h_i)$$

The output admittance is a function of source resistance. If the source impedance is resistive then Y_o is real.

Voltage Amplification Factor (A_{vs}) taking into account the resistance (R_s) of the source

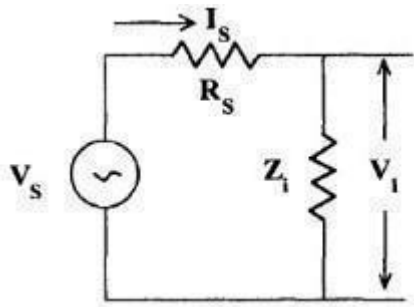


Fig.3.13 Thevenin's Equivalent Input

Circuit This overall voltage gain A_{vs} is given by

$$A_{vs} = V_2 / V_s = V_2 V_1 / V_1 V_s = A_v V_1 / V_s$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig.5.6 $V_1 =$

$$V_s Z_i / (Z_i + R_s)$$

$$V_1 / V_s = Z_i / (Z_i + R_s)$$

Then, $A_{vs} = A_v Z_i / (Z_i + R_s)$

Substituting $A_v = A_i Z_L / Z_i$

$$A_{vs} = A_i Z_L / (Z_i + R_s)$$

$$A_{vs} = A_i Z_L R_s / (Z_i + R_s) R_s$$

$$A_{vs} = A_{is} Z_L / R_s$$

Current Amplification (A_{is}) taking into account the source Resistance (R_s)

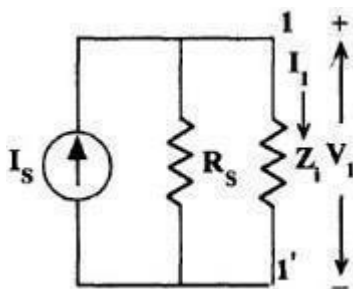


Fig.3.14 Norton's Equivalent Input Circuit

The modified input circuit using Norton's equivalent circuit for the calculation of A_{is} is shown in Fig. 1.7 Overall

Current Gain, $A_{is} = -I_2 / I_5 = -I_2 I_1 / I_1 I_5 = A_i I_1 / I_5$

From Fig. 1.7 $I_1 = I_5 R_S / (R_S + Z_i)$ I_1

$$I_1 / I_5 = R_S / (R_S + Z_i)$$

and hence, $A_{is} = A_i R_S / (R_S + Z_i)$

Operating Power Gain (A_P)

The operating power gain A_P of the transistor is defined as

$$A_P = P_2 / P_1 = -V_2 I_2 / V_1 I_1 = A_v A_i = A_i A_i Z_L / Z_i$$

$$A_P = A_i^2 (Z_L / Z_i)$$

Small Signal analysis of a transistor amplifier

$A_i = -h_f / (1 + Z_L h_o)$	$A_v = A_i Z_L / Z_i$
$Z_i = h_i + h_r A_1 Z_L = h_i - h_f h_r / (Y_L + h_o)$	$A_{vs} = A_v Z_i / (Z_i + R_S) = A_i Z_L / (Z_i + R_S)$ $= A_{is} Z_L / R_S$
$Y_o = h_o - h_f h_r / (R_S + h_i) = 1 / Z_o$	$A_{is} = A_i R_S / (R_S + Z_i) = A_{vs} = A_{is} R_S / Z_L$

UNIT -II BJT AMPLIFIERS FREQUENCY RESPONSE(HYBRIDE PI MODEL)

UNIT I

Small Signal High Frequency Transistor Amplifier models

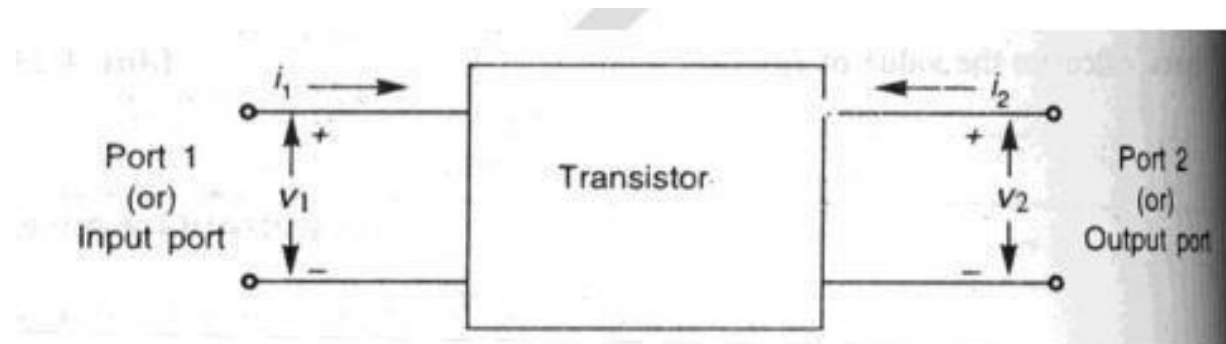
BJT: Transistor at high frequencies, Hybrid- π common emitter transistor model, Hybrid π conductances, Hybrid π capacitances, validity of hybrid π model, determination of high-frequency parameters in terms of low-frequency parameters , CE short circuit current gain, current gain with resistive load, cut-off frequencies, frequency response and gain bandwidth product. **FET:** Analysis of common Source and common drain Amplifier circuits at high frequencies.

Introduction:

Electronic circuit analysis subject teaches about the basic knowledge required to design an amplifier circuit, oscillators etc .It provides a clear and easily understandable discussion of designing of different types of amplifier circuits and their analysis using hybrid model, to find out their parameters. Fundamental concepts are illustrated by using small examples which are easy to understand. It also covers the concepts of MOS amplifiers, oscillators and large signal amplifiers.

Two port devices & Network Parameters:

A transistor can be treated as a two-part network. The terminal behavior of any two-part network can be specified by the terminal voltages V_1 & V_2 at parts 1 & 2 respectively and current i_1 and i_2 , entering parts 1 & 2, respectively, as shown in figure.



Of these four variables V_1 , V_2 , i_1 and i_2 , two can be selected as independent variables and the remaining two can be expressed in terms of these independent variables. This leads to various two part parameters out of which the following three are more important.

1. Z –Parameters (or) Impedance parameters
2. Y –Parameters (or) Admittance parameters
3. H –Parameters (or) Hybrid parameters

Hybrid parameters (or) h –parameters:

The equivalent circuit of a transistor can be drawn using simple approximation by retaining its essential features. These equivalent circuits will aid in analyzing transistor circuits easily and rapidly.

If the input current i_1 and output Voltage V_2 are taken as independent variables, the input voltage V_1 and output current i_2 can be written as

$$\begin{aligned} V_1 &= h_{11} i_1 + h_{12} V_2 \\ i_2 &= h_{21} i_1 + h_{22} V_2 \end{aligned}$$

The four hybrid parameters h_{11} , h_{12} , h_{21} and h_{22} are defined as follows:

$h_{11} = [V_1 / i_1]$ with $V_2 = 0$ Input Impedance with output part short circuited.

$h_{22} = [i_2 / V_2]$ with $i_1 = 0$ Output admittance with input part open circuited.

$h_{12} = [V_1 / V_2]$ with $i_1 = 0$ reverse voltage transfer ratio with input part open circuited.

$h_{21} = [i_2 / i_1]$ with $V_2 = 0$ Forward current gain with output part short circuited

The dimensions of h–parameters are as follows:

h_{11} – Ω

h_{22} –mhos

h_{12} , h_{21} –dimension less.

As the dimensions are not alike, (i.e.) they are hybrid in nature, and these parameters are called as hybrid parameters.

h_{11} = input; h_{22} = output;

h_{21} = forward transfer; h_{12} = Reverse transfer.

Notations used in transistor circuits:

$h_{ie} = h_{11e}$ = Short circuit input impedance

$h_{oe} = h_{22e}$ = Open circuit output admittance

$h_{re} = h_{12e}$ = Open circuit reverse voltage transfer ratio

$h_{fe} = h_{21e}$ = Short circuit forward current Gain.

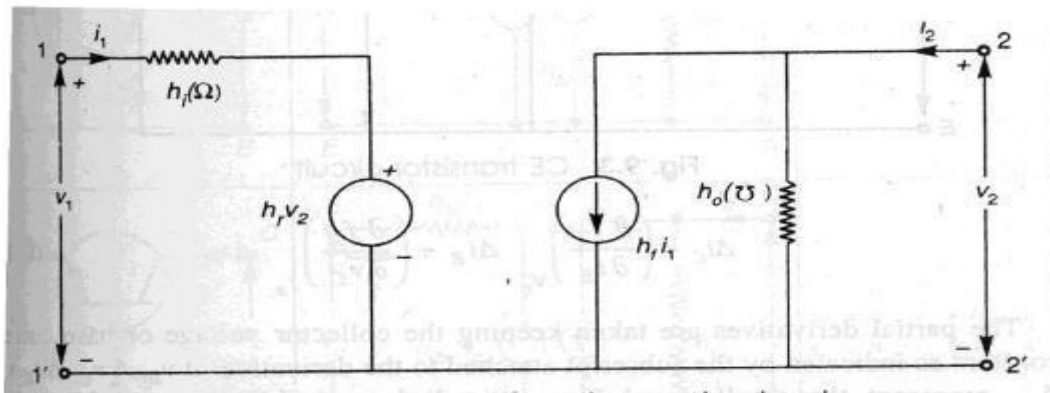
The Hybrid Model for Two-port Network:

$$V_1 = h_{11} i_1 + h_{12} V_2$$

$$I_2 = h_{21} i_1 + h_{22} V_2$$

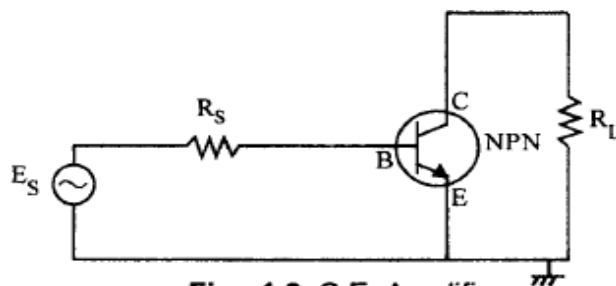
$$V_1 = h_{11} i_1 + h_r V_2$$

$$I_2 = h_{fi} i_1 + h_o V_2$$

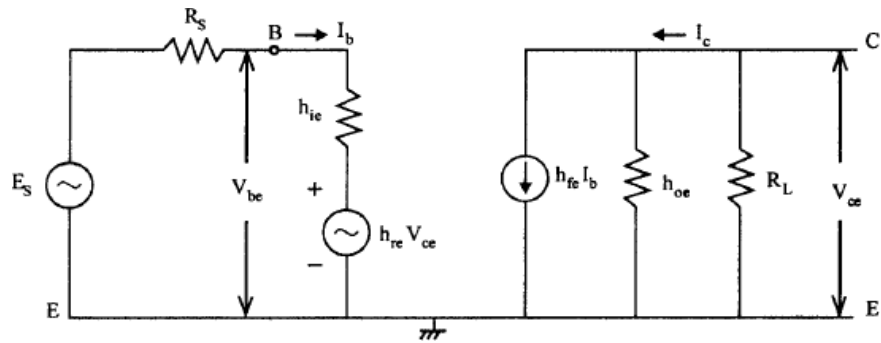


Common Emitter Amplifier

Common Emitter Circuit is as shown in the Fig. The DC supply, biasing resistors and coupling capacitors are not shown since we are performing an AC analysis.



E_s is the input signal source and R_s is its resistance. The h-parameter equivalent for the above circuit is as shown in Fig.



$$h_{ie} = \left. \frac{V_{be}}{I_b} \right|_{V_{ce}=0}$$

$$h_{re} = \left. \frac{V_{be}}{V_{ce}} \right|_{I_b=0}$$

$$h_{oe} = \left. \frac{I_c}{V_{ce}} \right|_{I_b=0}$$

$$h_{fe} = \left. \frac{I_c}{I_b} \right|_{V_{ce}=0}$$

The typical values of the h-parameter for a transistor in Common Emitter configuration are,

$$h_{ie} = \frac{V_{be}}{I_b}$$

$$h_{ie} = \frac{0.2V}{50 \times 10^{-6}} = 4K\Omega$$

$$h_{fe} = I_c / I_b \approx 100 .$$

$$h_{fe} \gg 1 \approx \beta$$

$$h_{re} = \frac{V_{be}}{V_{ce}}$$

$$h_{re} = 0.2 \times 10^{-3}$$

$$h_{oe} = \frac{I_c}{V_{ce}}$$

$$h_{oe} = 8 \mu\text{S}$$

$$R_1 = h_{ie} - \frac{h_{fe} h_{re}}{h_{oe} + \frac{1}{R_L}}$$

$$R_1 = h_{ie} - \frac{h_{fe} h_{re}}{h_{oe} + \frac{1}{R_L}}$$

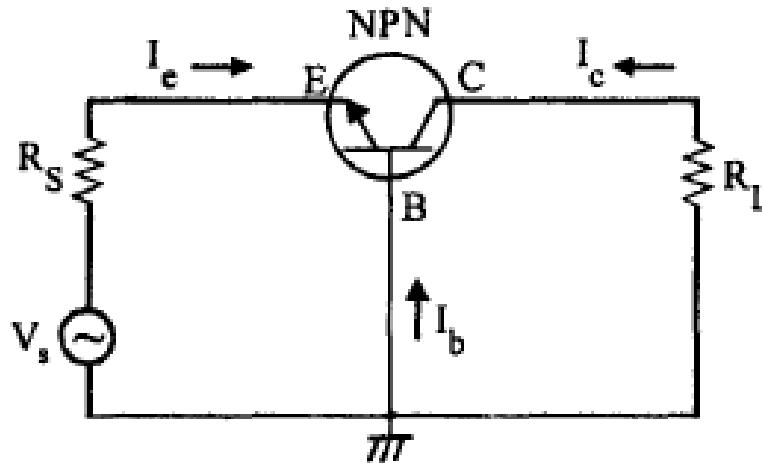
$$R_o = \frac{1}{h_{oe} - \left(\frac{h_{re} h_{fe}}{h_{ie} + R_s} \right)}$$

$$A_1 = \frac{-h_{fe}}{1 + h_{oe} R_L}$$

$$A_v = \frac{-h_{fe} R_L}{h_{ie} + R_L (h_{ie} h_{oe} - h_{fe} h_{re})}$$

Common Base Amplifier

Common Base Circuit is as shown in the Fig. The DC supply, biasing resistors and coupling capacitors are not shown since we are performing an AC analysis.



$$h_{ib} = \left. \frac{V_{eb}}{I_e} \right|_{V_{cb}=0}$$

$$h_{fb} = \left. \frac{I_c}{I_e} \right|_{V_{cb}=0} = -0.99 \text{ (Typical Value)}$$

$$I_c < I_e \quad \therefore \quad h_{fb} < 1$$

$$h_{ob} = \left. \frac{I_c}{V_{cb}} \right|_{I_e=0} = 7.7 \times 10^{-8} \text{ mhos (Typical Value)}$$

$$h_{rb} = \left. \frac{V_{eb}}{V_{cb}} \right|_{I_e = 0} = 37 \times 10^{-6} \text{ (Typical Value)}$$

$$R_i = h_{ib} - \frac{h_{fb} \cdot h_{rb}}{h_{ob} + \frac{1}{R_L}}$$

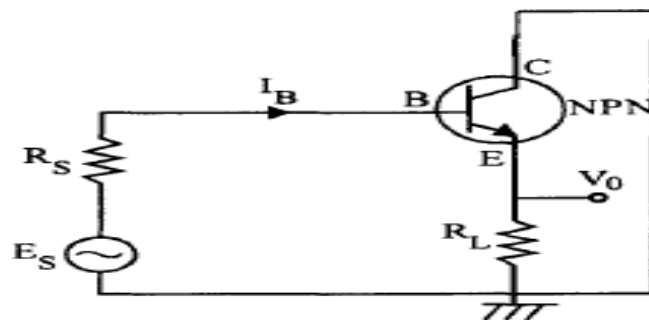
$$R_o = \frac{1}{h_{ob} - \frac{h_{rb} h_{fb}}{h_{ib} + R_s}}$$

$$A_i = \frac{-h_{fb}}{1 + h_{ob} R_L}$$

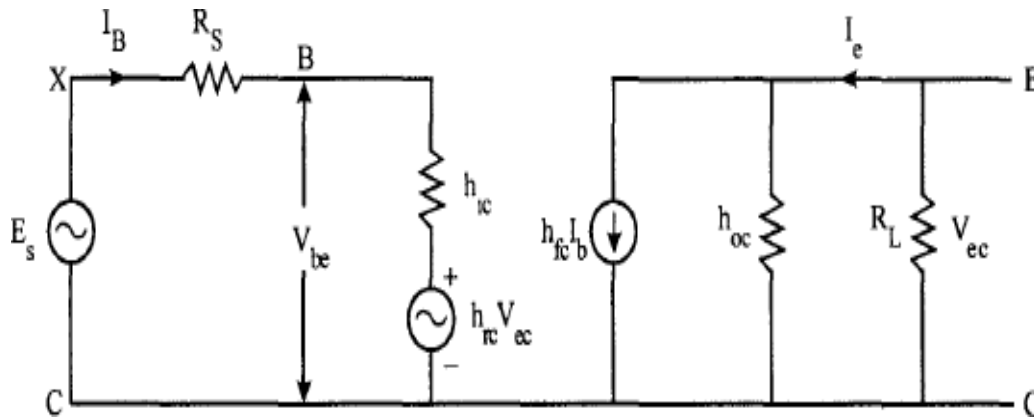
$$A_v = \frac{-h_{fb} R_L}{h_{ib} + R_L (h_{ib} h_{ob} - h_{fb} h_{rb})}$$

Common Collector Amplifier

Common Collector Circuit is as shown in the Fig. The DC supply, biasing resistors and coupling capacitors are not shown since we are performing an AC analysis



The h-parameter model is shown below



$$h_{ie} = \left. \frac{V_{be}}{I_b} \right|_{V_{ec}=0} = 2,780 \, \Omega \text{ (Typical Value)}$$

$$h_{oc} = \left. \frac{I_e}{V_{ec}} \right|_{I_b=0} = 7.7 \times 10^{-6} \text{ mhos (Typical Value)}$$

$$h_{fe} = - \left. \frac{I_e}{I_b} \right|_{V_{ec}=0} = 100 \text{ (Typical value)}$$

$$\therefore I_e \gg I_b$$

$$h_{re} = \left. \frac{V_{be}}{V_{ec}} \right|_{I_b=0} ;$$

Transistors at High Frequencies

At low frequencies it is assumed that transistor responds instantaneously to changes in the input voltage or current i.e., if you give AC signal between the base and emitter of a Transistor amplifier in Common Emitter configuration and if the input signal frequency is low, the output at the collector will exactly follow the change in the input (amplitude etc.,). If 'f' of the input is high (MHz) and the amplitude of the input signal is changing the Transistor amplifier will not be able to respond.

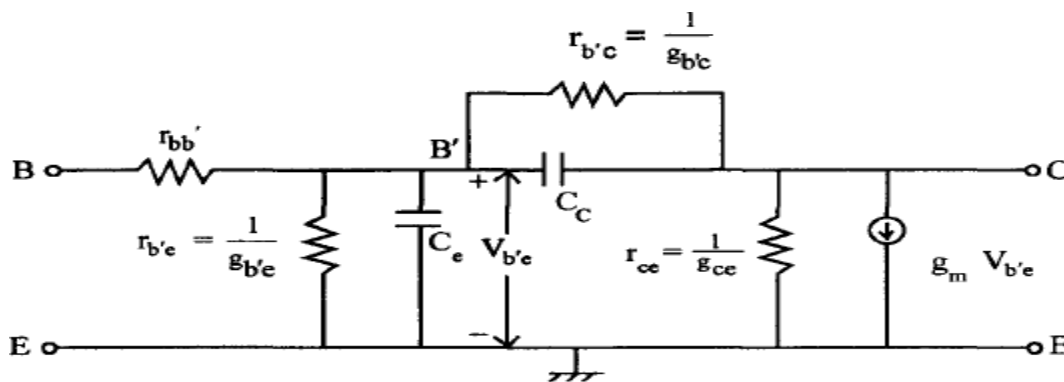
It is because; the carriers from the emitter side will have to be injected into the collector side. These take definite amount of time to travel from Emitter to Base, however small it may be. But if the input signal is varying at much higher speed than the actual time taken by the carriers to

respond, then the Transistor amplifier will not respond instantaneously. Thus, the junction capacitances of the transistor, puts a limit to the highest frequency signal which the transistor can handle. Thus depending upon doping area of the junction etc, we have transistors which can respond in AF range and also RF range.

To study and analyze the behavior of the transistor to high frequency signals an equivalent model based upon transmission line equations will be accurate. But this model will be very complicated to analyze. So some approximations are made and the equivalent circuit is simplified. If the circuit is simplified to a great extent, it will be easy to analyze, but the results will not be accurate. If no approximations are made, the results will be accurate, but it will be difficult to analyze. The desirable features of an equivalent circuit for analysis are simplicity and accuracy. Such a circuit which is fairly simple and reasonably accurate is the Hybrid- π or Hybrid- π model, so called because the circuit is in the form of π .

Hybrid - π Common Emitter Transconductance Model

For Transconductance amplifier circuits Common Emitter configuration is preferred. Why? Because for Common Collector ($h_{rc} < 1$). For Common Collector Configuration, voltage gain $A_v < 1$. So even by cascading you can't increase voltage gain. For Common Base, current gain is $h_{ib} < 1$. Overall voltage gain is less than 1. For Common Emitter, $h_{re} \gg 1$. Therefore Voltage gain can be increased by cascading Common Emitter stage. So Common Emitter configuration is widely used. The Hybrid- π or Giacoletto Model for the Common Emitter amplifier circuit (single stage) is as shown below.



Analysis of this circuit gives satisfactory results at all frequencies not only at high frequencies but also at low frequencies. All the parameters are assumed to be independent of frequency.

Where B' = internal node in base

$r_{bb'}$ = Base spreading resistance

$r_{b'e}$ = Internal base node to emitter resistance

r_{ce} = collector to emitter resistance

C_e = Diffusion capacitance of emitter base junction

$r_{b'c}$ = Feedback resistance from internal base node to collector node

g_m = Transconductance

C_c = transition or space charge capacitance of base collector junction

Circuit Components

B' is the internal node of base of the Transconductance amplifier. It is not physically accessible. The base spreading resistance $r_{bb'}$ is represented as a lumped parameter between base B and internal node B' . $g_m V_{b'e}$ is a current generator. $V_{b'e}$ is the input voltage across the emitter junction. If $V_{b'e}$ increases, more carriers are injected into the base of the transistor. So the increase in the number of carriers is proportional to $V_{b'e}$. This results in small signal current since we are taking into account changes in $V_{b'e}$. This effect is represented by the current generator $g_m V_{b'e}$. This represents the current that results because of the changes in $V_{b'e}$ when C is shorted to E .

When the number of carriers injected into the base increase, base recombination also increases. So this effect is taken care of by $g_{b'e}$. As recombination increases, base current increases. Minority carrier storage in the base is represented by C_e the diffusion capacitance.

According to Early Effect, the change in voltage between Collector and Emitter changes the base width. Base width will be modulated according to the voltage variations between Collector and Emitter. When base width changes, the minority carrier concentration in base changes. Hence the current which is proportional to carrier concentration also changes. I_E changes and I_C changes. This feedback effect [I_E on input side, I_C on output side] is taken into account by connecting $g_{b'e}$ between B' , and C . The conductance between Collector and Base is g_{ce} . C_c represents the collector junction barrier capacitance.

Hybrid - n Parameter Values

Typical values of the hybrid- n parameter at $I_C = 1.3 \text{ mA}$ are as follows:

$$g_m = 50 \text{ mA/V}$$

$$r_{bb'} = 100 \, \Omega$$

$$r_{b'e} = 1 \, \text{k}\Omega$$

$$r_{ee} = 80 \, \text{k}\Omega$$

$$C_c = 3 \, \text{pf}$$

$$C_e = 100 \, \text{pf}$$

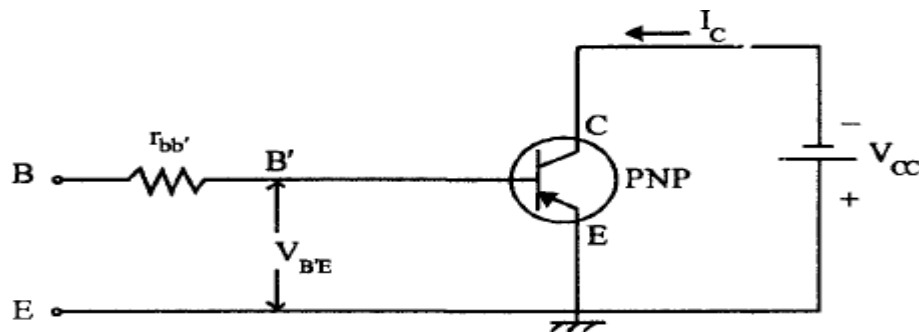
$$r_{b'c} = 4 \, \text{M}\Omega$$

These values depend upon:

1. Temperature
2. Value of I_C

Determination of Hybrid- π Conductances

1. Trans conductance or Mutual Conductance (g_m)



The above figure shows PNP transistor amplifier in Common Emitter configuration for AC purpose, Collector is shorted to Emitter.

$$I_C = I_{C0} - \alpha_0 \cdot I_E$$

I_{C0} opposes I_E . I_E is negative. Hence $I_C = I_{C0} - \alpha_0 I_E$ α_0 is the normal value of α at room temperature.

In the hybrid - π equivalent circuit, the short circuit current = $g_m V_{b'e}$

Here only transistor is considered, and other circuit elements like resistors, capacitors etc are not considered.

$$g_m = \left. \frac{\partial I_C}{\partial V_{b'e}} \right|_{V_{CE} = K}$$

Differentiate (1) with respect to $V_{b'e}$ partially. I_{C0} is constant

$$g_m = 0 - \alpha_0 \frac{\partial I_E}{\partial V_{b'e}}$$

For a PNP transistor, $V_{b'e} = -V_E$ Since, for PNP transistor, base is n-type. So negative voltage is given

$$g_m = \alpha_0 \frac{\partial I_E}{\partial V_E}$$

If the emitter diode resistance is r_e then

$$r_e = \frac{\partial V_E}{\partial I_E}$$

$$g_m = \frac{\alpha_0}{r_e}$$

$$r = \frac{\eta \cdot V_T}{I} \quad \eta = 1, \quad I = I_E \quad r = \frac{V_T}{I_E}$$

$$g_m = \frac{\alpha_0 \cdot I_E}{V_T} \quad \alpha_0 \simeq 1, \quad I_E \simeq I_C$$

$$I_E = I_{C0} - I_C$$

$$g_m = \frac{I_{C0} - I_C}{V_T}$$

Neglect I_{C0}

$$g_m = \frac{|I_C|}{V_T}$$

g_m is directly proportional to I_C is also inversely proportional to T . For PNP transistor, I_C is negative

$$g_m = \frac{-I_C}{V_T}$$

At room temperature i.e. $T=300^0K$

$$g_m = \frac{|I_C|}{26}, I_C \text{ is in mA.}$$

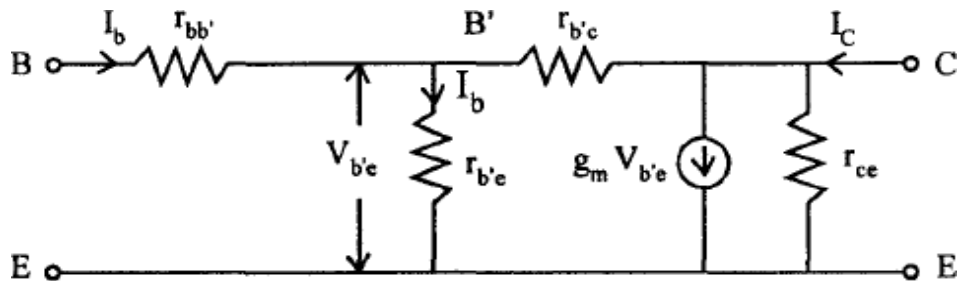
If $I_C = 1.3 \text{ mA}$, $g_m = 0.05 \text{ A/V}$

If $I_C = 10 \text{ mA}$, $g_m = 400 \text{ mA/V}$

Input Conductance ($g_{b'e}$):

At low frequencies, capacitive reactance will be very large and can be considered as Open circuit. So in the hybrid- π equivalent circuit which is valid at low frequencies, all the capacitances can be neglected.

The equivalent circuit is as shown in Fig.



The value of $r_{b'c} \gg r_{b'e}$ (Since Collector Base junction is Reverse Biased) So I_b flows into $r_{b'e}$ only. [This is I_b ($I_E - I_C$) will go to collector junction]

$$V_{b'e} \simeq I_b \cdot r_{b'e}$$

The short circuit collector current,

$$I_C = g_m \cdot V_{b'e}; \quad V_{b'e} = I_b \cdot r_{b'e}$$

$$I_C = g_m \cdot I_b \cdot r_{b'e}$$

$$h_{fe} = \left. \frac{I_C}{I_B} \right|_{V_{CE}} = g_m \cdot r_{b'e}$$

$$r_{b'e} = \frac{h_{fe}}{g_m}$$

$$g_m = \frac{|I_C|}{V_T}$$

$$r_{b'e} = \frac{h_{fe} \cdot V_T}{|I_C|}$$

$$g_{b'e} = \frac{|I_C|}{h_{fe} V_T} \quad \text{or} \quad \frac{g_m}{h_{fe}}$$

Feedback Conductance ($g_{b'c}$)

h_{re} = reverse voltage gain, with input open or $I_b = 0$

$h_{re} = V_{b'e}/V_{ce}$ = Input voltage/Output voltage

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}}$$

[With input open, i.e., $I_b = 0$, V_{ce} is output. So it will get divided between $r_{b'e}$ and $r_{b'c}$ only]

or

$$h_{re}(r_{b'e} + r_{b'c}) = r_{b'e}$$
$$r_{b'e}[1 - h_{re}] = h_{re} r_{b'c}$$

But

$$h_{re} \ll 1$$

$$\therefore r_{b'e} = h_{re} r_{b'c}; \quad r_{b'c} = \frac{r_{b'e}}{h_{re}}$$

or

$$\boxed{g_{b'c} = h_{re} g_{b'e}} \quad \frac{1}{r_{b'c}} = g_{b'c} = \frac{h_{re}}{r_{b'e}}$$

$$h_{re} = 10^{-4}$$

$$\therefore r_{b'c} \gg r_{b'e}$$

Base Spreading Resistance (r_{bb'})

The input resistance with the output shorted is h_{ie}. If output is shorted, i.e., Collector and Emitter are joined; r_{b'e} is in parallel with r_{b'c}.

$$\begin{aligned} h_{ie} &= r_{bb'} + r_{b'e} \\ \boxed{r_{bb'} &= h_{ie} - r_{b'e}} \\ h_{ie} &= r_{bb'} + r_{b'e} \end{aligned} \qquad \begin{aligned} r_{b'e} &= \frac{h_{fe} \cdot V_T}{|I_C|} \\ h_{ie} &= r_{bb'} + \frac{h_{fe} \cdot V_T}{|I_C|} \end{aligned}$$

Output Conductance (g_{ce})

This is the conductance with input open circuited. In h-parameters it is represented as h_{oe}. For I_b= 0, we have,

$$\begin{aligned} I_C &= \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}} + g_m V_{b'e} \\ h_{re} &= \frac{V_{b'e}}{V_{ce}} \qquad \therefore V_{b'e} = h_{re} \cdot V_{ce} \\ I_C &= \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}} + g_m \cdot h_{re} \cdot V_{ce} \end{aligned}$$

$$h_{oe} = \frac{1}{r_{ce}} + \frac{1}{r_{b'c}} + g_m \cdot h_{re}$$

$$= g_{ce} + g_{b'c} + g_m h_{re}$$

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

$$g_m = g_{b'e} \cdot h_{fe}$$

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}} \approx \frac{r_{b'e}}{r_{b'c}} = \frac{g_{b'c}}{g_{b'e}}$$

$$h_{oe} = g_{ce} + g_{b'c} + g_{b'e} h_{fe} \cdot \frac{g_{b'c}}{g_{b'e}}$$

$$g_{ce} = h_{oe} - (1 + h_{fe}) \cdot g_{b'c}$$

$$h_{fe} \gg 1, \quad 1 + h_{fe} \approx h_{fe}$$

$$\boxed{g_{ce} = h_{oe} - h_{fe} \cdot g_{b'c}}$$

$$g_{b'c} = h_{re} \cdot g_{b'e}$$

$$g_{ce} = h_{oe} - h_{fe} \cdot h_{re} \cdot g_{b'e}$$

Hybrid - π Capacitances

In the hybrid - π equivalent circuit, there are two capacitances, the capacitance between the Collector Base junction is the C_C or $C_{b'e'}$. This is measured with input open i.e., $I_E = 0$, and is specified by the manufacturers as C_{Ob} . 0 indicates that input is open. Collector junction is reverse biased.

$$C_C \propto \frac{1}{(V_{CE})^n}$$

$$n = \frac{1}{2} \quad \text{for abrupt junction}$$
$$= 1/3 \quad \text{for graded junction.}$$

C_e = Emitter diffusion capacitance C_{De} + Emitter junction capacitance C_{Te}

C_T = Transition capacitance.

C_D = Diffusion capacitance.

$$C_{De} \gg C_{Te}$$

$$C_e \approx C_{De}$$

$C_{De} \propto I_E$ and is independent of Temperature T .

Validity of hybrid- π model

The high frequency hybrid Pi or Giacoletto model of BJT is valid for frequencies less than the unit gain frequency.

High frequency model parameters of a BJT in terms of low frequency hybrid parameters

The main advantage of high frequency model is that this model can be simplified to obtain low frequency model of BJT. This is done by eliminating capacitance's from the high frequency model so that the BJT responds without any significant delay (instantaneously) to the input signal. In practice there will be some delay between the input signal and output signal of BJT which will be very small compared to signal period ($1/\text{frequency of input signal}$) and hence can be neglected. The high frequency model of BJT is simplified at low frequencies and redrawn as shown in the figure below along with the small signal low frequency hybrid model of BJT.

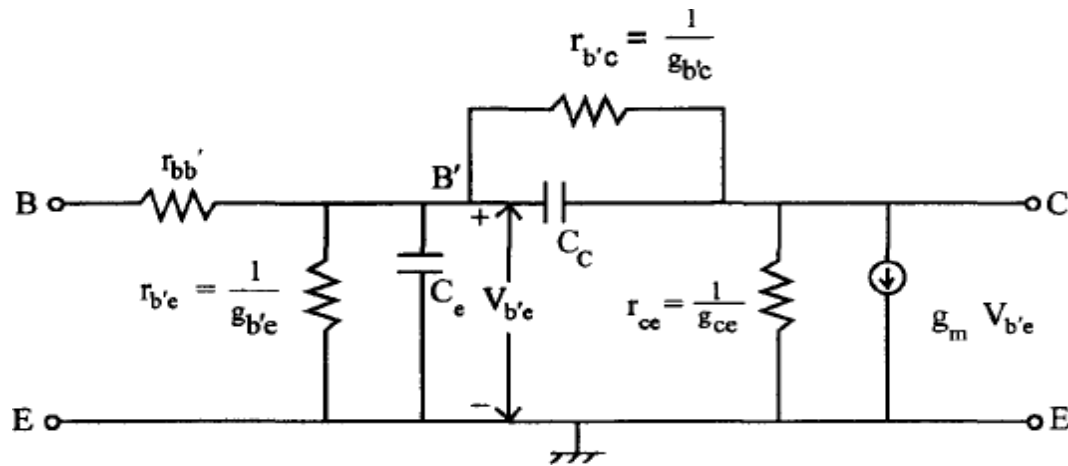


Fig. high frequency model of BJT at low frequencies

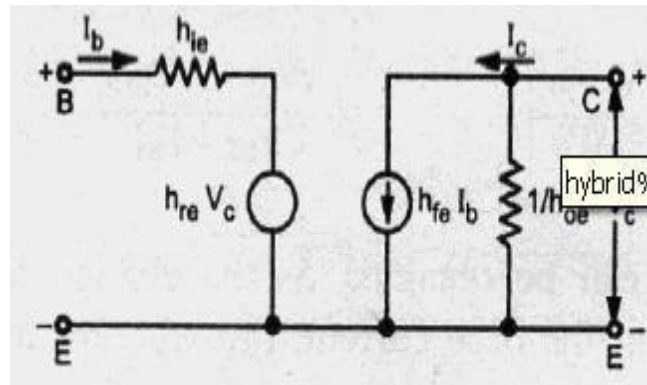


Fig hybrid model of BJT at low frequencies

The High frequency model parameters of a BJT in terms of low frequency hybrid parameters are given below:

Transconductance $g_m = I_c/V_t$

Internal Base node to emitter resistance $r_{b'e} = h_{fe}/g_m = (h_{fe} * V_t)/I_c$

Internal Base node to collector resistance $r_{b'c} = (h_{re} * r_{b'e}) / (1 - h_{re})$ assuming $h_{re} \ll 1$ it reduces to $r_{b'c} = (h_{re} * r_{b'e})$

Base spreading resistance $r_{bb'} = h_{ie} - r_{b'e} = h_{ie} - (h_{fe} * V_t)/I_c$

Collector to emitter resistance $r_{ce} = 1 / (h_{oe} - (1 + h_{fe})/r_{b'c})$

Collector Emitter Short Circuit Current Gain

Consider a single stage Common Emitter transistor amplifier circuit. The hybrid-1t equivalent circuit is as shown:

$$I_L = -g_m V_{b'e}$$
$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)}$$

A_1 under short circuit condition is,

$$A_1 = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

But

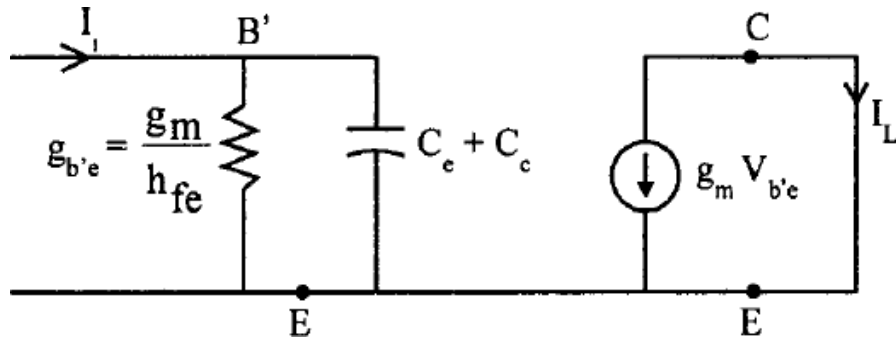
$$g_{b'e} = \frac{g_m}{h_{fe}}, \quad C_e + C_c \simeq C_e$$

$$C_e = \frac{g_m}{2\pi f_T}$$
$$= \frac{-g_m}{\frac{g_m}{h_{fe}} + \frac{j 2\pi \cdot g_m \cdot f}{2\pi f_T}}$$

$\therefore$

$$A_1 = \frac{-1}{\frac{1}{h_{fe}} + j \left(\frac{f}{f_T} \right)}$$

If the output is shorted i.e. $R_L = 0$, what will be the flow response of this circuit? When $R_L = 0$, $V_o = 0$. Hence $A_v = 0$. So the gain that we consider here is the current gain I_L/I_i . The simplified equivalent circuit with output shorted is,



A current source gives sinusoidal current I_c . Output current or load current is I_L . $g_{b'e}$ is neglected since $g_{b'e} \ll g_m$, g_{ce} is in shunt with short circuit $R = 0$. Therefore g_{ce} disappears. The current is delivered to the output directly through C_e and $g_{b'e}$ is also neglected since this will be very small.

$$I_L = -g_m V_{b'e}$$

$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)}$$

A_i under short circuit condition is,

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

But

$$g_{b'e} = \frac{g_m}{h_{fe}}, \quad C_e + C_c \simeq C_e$$

$$C_e = \frac{g_m}{2\pi f_T}$$

$$= \frac{-g_m}{\frac{g_m}{h_{fe}} + \frac{j2\pi \cdot g_m \cdot f}{2\pi f_T}}$$

$$\therefore A_i = \frac{-1}{\frac{1}{h_{fe}} + j\left(\frac{f}{f_T}\right)}$$

$$= \frac{-h_{fe}}{1 + j h_{fe} \left(\frac{f}{f_T} \right)}$$

$$A_i = \frac{-h_{fe}}{1 + j \left(\frac{f}{f_\beta} \right)}$$

$$\frac{f_T}{h_{fe}} = f_\beta$$

$$|A_i| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_\beta} \right)^2}}$$

Where $f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_c)}$

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

$$\therefore f_\beta = \frac{g_m}{h_{fe} 2\pi(C_e + C_c)}$$

At $f = f_\beta$, $A_i = \frac{1}{\sqrt{2}} = 0.707$ of h_{fe} .

Current Gain with Resistance Load:

$$f_T = f_\beta \cdot h_{fe} = \frac{g_m}{2\pi(C_e + C_c)} \Big|$$

Considering the load resistance R_L

$V_{b'e}$ is the input voltage and is equal to V_1

V_{ce} is the output voltage and is equal to V_2

$$K_2 = \frac{V_{ce}}{V_{b'e}}$$

This circuit is still complicated for analysis. Because, there are two time constants associated with the input and the other associated with the output. The output time constant will be much smaller than the input time constant. So it can be neglected.

K = Voltage gain. It will be $\gg 1$

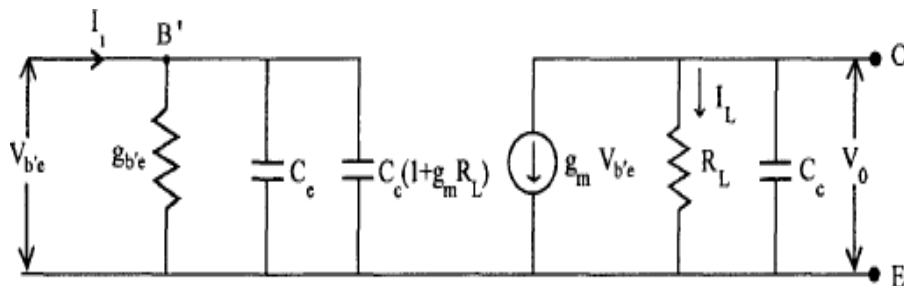
$$g_{b'e} \left(\frac{K-1}{K} \right) \simeq g_{b'e}$$

$$g_{b'e} < g_{ce} \quad \therefore \quad r_{b'e} \simeq 4 \text{ M}\Omega, \quad r_{ce} = 80 \text{ K (typical values)}$$

So $g_{b'e}$ can be neglected in the equivalent circuit. In a wide band amplifier R_L will not exceed $2\text{K}\Omega$. If R_L is small f_H is large.

$$f_H = \frac{1}{2\pi C_S (R_C \parallel R_L)}$$

Therefore g_{ce} can be neglected compared with R_L . Therefore the output circuit consists of current generator $g_m V_{b'e}$ feeding the load R_L so the Circuit simplifies as shown in Fig.



$$K = \frac{V_{ce}}{V_{b'e}} = -g_m R_L; \quad g_m = 50 \text{ mA/V}, \quad R_L = 2 \text{ K}\Omega \text{ (typical values)}$$

$$K = -100$$

Miller's Theorem

It states that if an impedance Z is connected between the input and output terminals, of a network, between which there is voltage gain, K , the same effect can be had by removing Z and connecting an impedance Z_i at the input $= Z/(1-K)$ and Z_o across the output $= ZK/(K-1)$

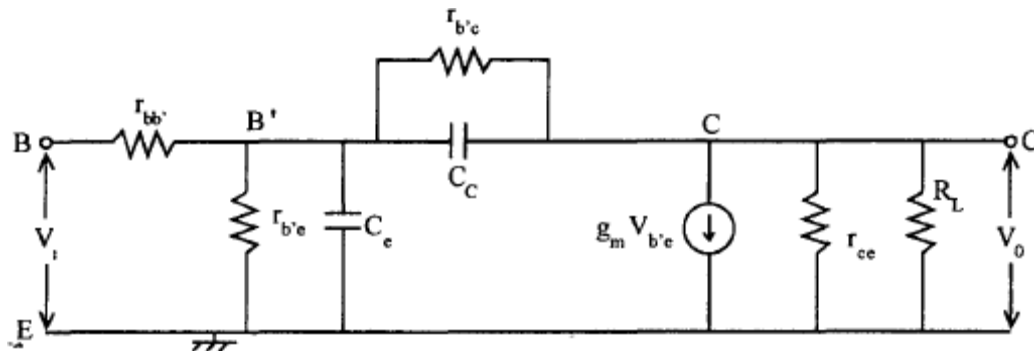


Fig. High frequency equivalent circuit with resistive load R_L

Therefore high frequency equivalent circuit using Miller's theorem reduces to

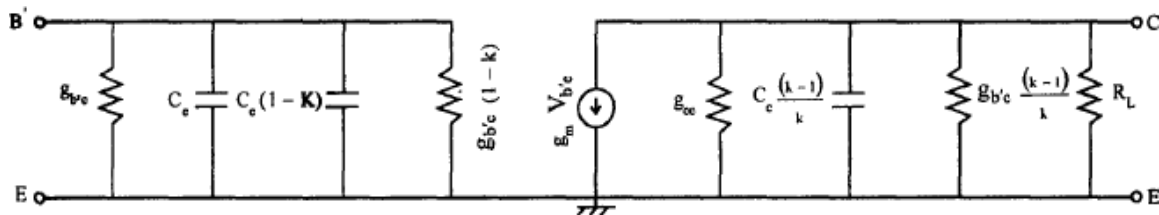


Fig. Circuit after applying Millers' Theorem

$$K = \frac{V_{ce}}{V_{b'e}}$$

$$V_{ce} = -I_c \cdot R_L$$

$$K = \frac{-I_C \cdot R_L}{V_{b'e}}$$

$$\frac{I_C}{V_{b'e}} = g_m$$

$$K = -g_m \cdot R_L$$

The Parameters f_T

f_T is the frequency at which the short circuit Common Emitter current gain becomes unity.

The Parameters f_β

$$A_i = 1, \quad \text{or} \quad \frac{h_{fe}}{\sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}} = 1$$

$$f = f_T, \quad A_i = 1$$

$$h_{fe} = \sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}$$

$$(h_{fe})^2 = 1 + \left(\frac{f_T}{f_\beta}\right)^2 \cong \left(\frac{f_T}{f_\beta}\right)^2$$

$$h_{fe} \simeq \frac{f_T}{f_\beta} \quad \text{when } A_i = 1$$

$$\boxed{f_T \simeq h_{fe} \cdot f_\beta}$$

$$f_\beta = \frac{g_m}{h_{fe} \{C_e + C_c\}}$$

$$f_T = f_\beta \cdot h_{fe} = \frac{g_m}{2\pi(C_e + C_c)}$$

$$C_e \gg C_c$$

$$\boxed{f_T \simeq \frac{g_m}{2\pi C_e}}$$

$$A_i = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

Dividing by $g_{b'e}$, Numerator and Denominator,

$$A_i = \frac{-g_m |g_{b'e}|}{1 + \frac{j2\pi f(C_e + C_c)}{g_{b'e}}}$$

we know that $g_{b'e} = \frac{g_m}{h_{fe}}$

$\therefore \frac{g_m}{g_{b'e}} = h_{fe}$

$$A_i = \frac{-h_{fe}}{1 + jf \left[\frac{2\pi(C_e + C_c)}{g_{b'e}} \right]}$$

But we know that $A_i = \frac{-h_{fe}}{1 + j \frac{f}{f_\beta}}$

Comparing, $f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_c)} = \frac{g_m}{h_{fe} \cdot 2\pi(C_e + C_c)} \quad \therefore g_{b'e} = \frac{g_m}{h_{fe}}$

$\therefore \boxed{f_\beta = \frac{g_m}{h_{fe} \cdot 2\pi(C_e + C_c)}}$

$\boxed{f_T = \frac{g_m}{2\pi(C_e + C_c)}}$

Gain - Bandwidth (B.W) Product

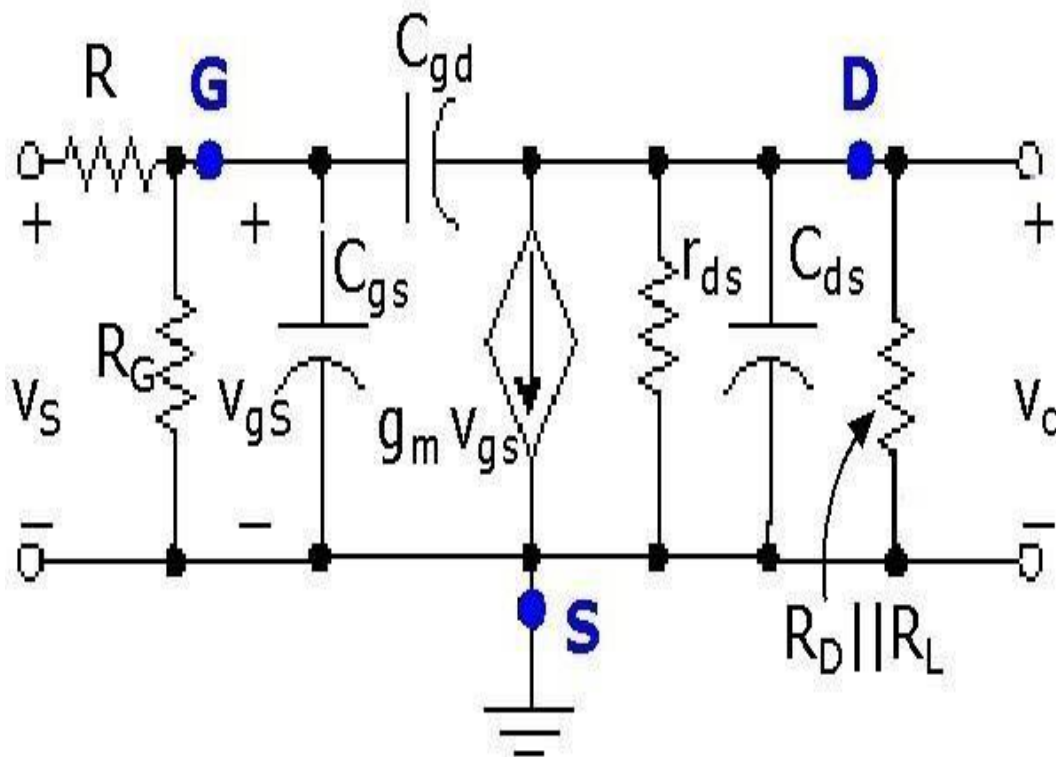
This is a measure to denote the performance of an amplifier circuit. Gain - B. W product is also referred as Figure of Merit of an amplifier. Any amplifier circuit must have large gain and large bandwidth. For certain amplifier circuits, the mid band gain A_m maybe large, but not Band width or Vice - Versa. Different amplifier circuits can be compared with this parameter.

FET: Analysis of common Source and common drain Amplifier circuits at high frequencies.

Just like for the BJT, we could use the original small signal model for low frequency analysis—the only difference was that external capacitances had to be kept in the circuit. Also just like the BJT, for high frequency operation, the internal capacitances between each of the device's terminals can no longer be ignored and the small signal model must be modified. Recall that for high frequency operation, we're stating that external capacitances are so large (in relation to the internal capacitances) that they may be considered short circuits.

High frequency response of Common source amplifier

The JFET implementation of the common-source amplifier is given to the left below, and the small signal circuit in incorporating the high frequency FET model is given to the right below. As stated above, the external coupling and bypass capacitors are large enough that we can model them as short circuits for high frequencies.



We may simplify the small signal circuit by making the following approximations and observations:

1. r_{ds} is usually larger than $R_D || R_L$, so that the parallel combination is dominated by $R_D || R_L$ and r_{ds} may be neglected. If this is not the case, a single equivalent resistance, $r_{ds} || R_D || R_L$ may be defined.
2. The Miller effect transforms C_{gd} into separate capacitances seen in the input and output circuits as

$$C_{M1} = C_{gd}(1 - A_v) \text{ (input circuit)}$$

$$C_{M2} = C_{gd} \left(1 - \frac{1}{A_v} \right) \text{ (output circuit)}$$

3. C_{ds} is very small, so the impedance contribution of this capacitance may be considered to be an open circuit and may be ignored.

$$C_{in} = C_{gs} + C_{M1} = C_{gs} + C_{gd}(1 - A_v),$$

4. The parallel capacitances in the input circuit, C_{gs} and C_{M1} , may be combined to a single equivalent capacitance of value

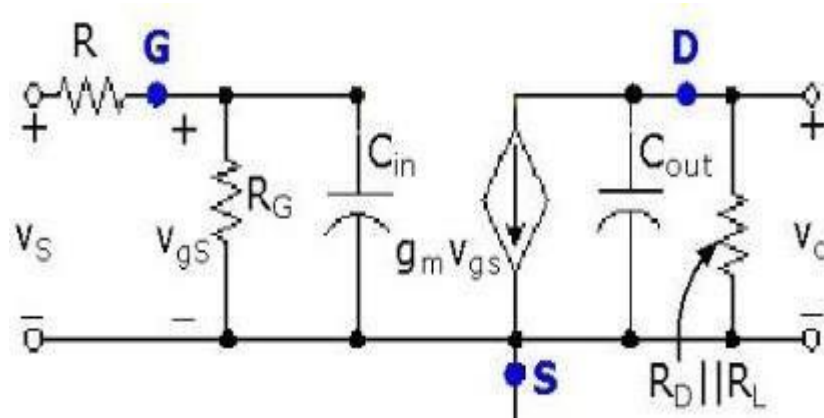
$$C_{in} = C_{gs} + C_{M1} = C_{gs} + C_{gd}(1 - A_v).$$

5. Similarly, the parallel capacitances in the output circuit, C_{ds} and C_{M2} , may be combined to a single equivalent capacitance of value

$$C_{out} = C_{ds} + C_{M2} = C_{ds} + C_{gd} \left(1 - \frac{1}{A_v} \right),$$

Where $A_v = -g_m(R_D || R_L)$ for a common-source amplifier.

Setting the input source, v_S , equal to zero allows us to define the equivalent resistances seen by C_{in} and C_{out} (the Method of Open Circuit Time Constants). Note that, with $v_S=0$, the dependent current source also goes to zero (opens) and the input and output circuits are separated.



$$R_{Cin} = R || R_G .$$

$$R_{Cout} = R_D || R_L .$$

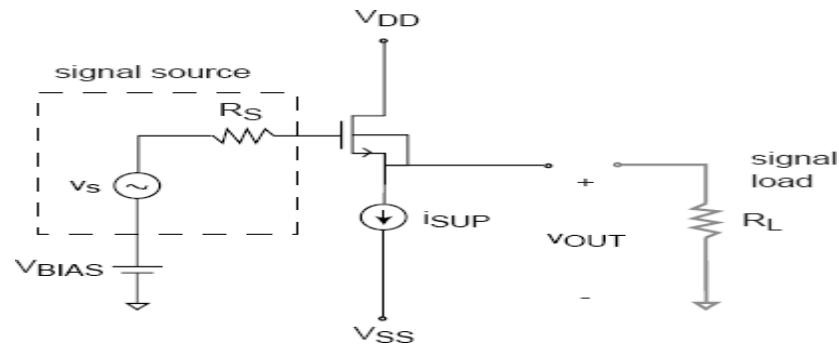
$$\tau_{Cin} = C_{in} R_{Cin} ; \quad \tau_{Cout} = C_{out} R_{Cout} ,$$

$$\omega_H = \frac{1}{\frac{1}{\omega_{Cin}} + \frac{1}{\omega_{Cout}}} = \frac{1}{\tau_{Cin} + \tau_{Cout}} = \frac{1}{C_{in} R_{Cin} + C_{out} R_{Cout}} = \frac{1}{C_{in}(R || R_G) + C_{out}(R_D || R_L)}$$

Generally, the input is going to provide the dominant pole, so the high frequency cut off is given by

$$\omega_H = \frac{1}{C_{in}(R || R_G)} ; \quad f_H = \frac{\omega_H}{2\pi} = \frac{1}{2\pi C_{in}(R || R_G)} .$$

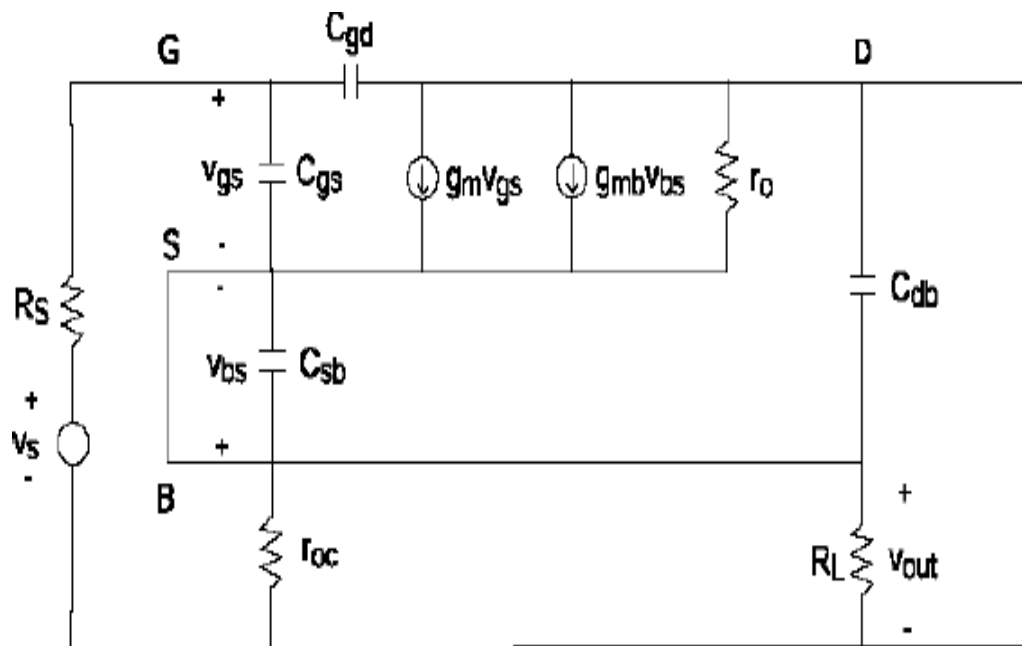
High frequency response of Common source amplifier

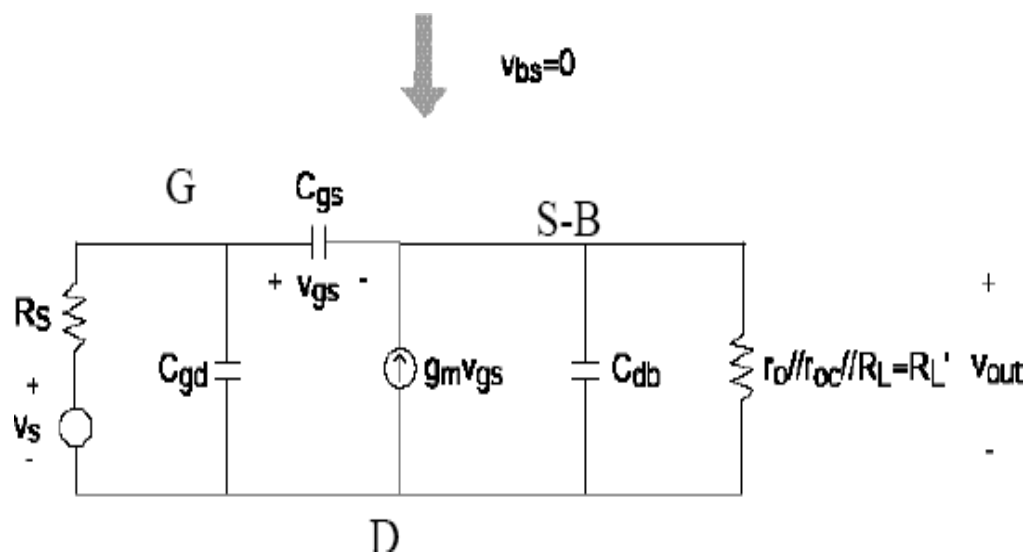


Characteristics of CD Amplifier:

- Voltage gain ≈ 1
- High input resistance
- Low output resistance
- Good voltage buffer

High frequency small signal model





$$A_v C_{gs} = \frac{R_L}{R_{out} + R_L} = \frac{g_m R_L}{1 + g_m R_L}$$

$$C_M = C_{gs} \left(1 - A_v C_{gs} \right) = C_{gs} \left(1 - \frac{g_m R_L}{1 + g_m R_L} \right) = \frac{C_{gs}}{1 + g_m R_L}$$

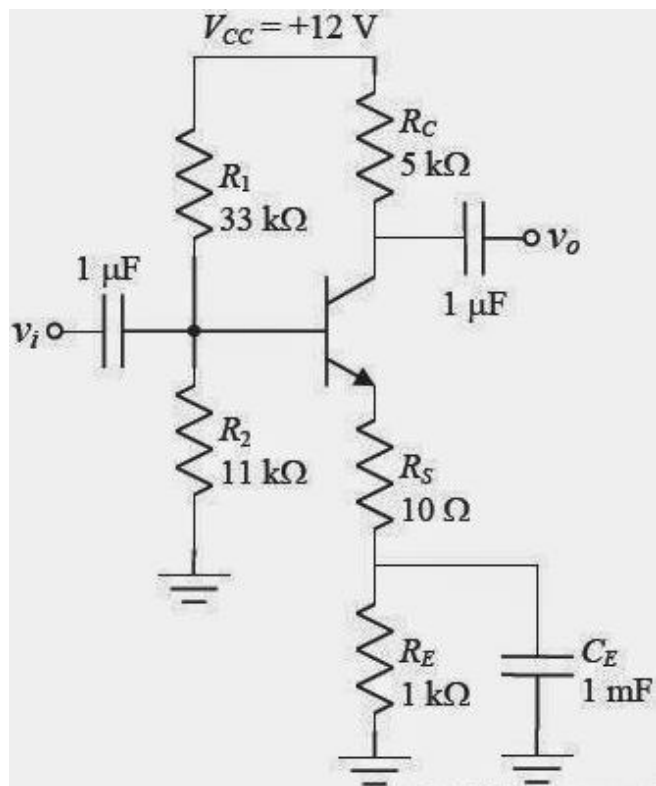
$$C_T = C_{gs} \left(1 - \frac{g_m R_L}{1 + g_m R_L} \right) + C_{gd}$$

$$R_T = R_S \parallel R_{in} = R_S$$

$$R_{C_{db}} = R_{out} \parallel R_L = \frac{R_{out} R_L}{R_{out} + R_L} = \frac{R_L}{1 + g_m R_L}$$

$$\omega_{3dB} \approx \frac{1}{R_S \left(\frac{C_{gs}}{1 + g_m R_L} + C_{gd} \right) + C_{db} \frac{R_L}{1 + g_m R_L}}$$

If R_S is not too high, bandwidth can be rather high and approach ω_T



UNIT-II

Multistage Amplifiers : Classification of amplifiers, methods of coupling, cascaded transistor amplifier and its analysis, analysis of two stage RC coupled amplifier, high input resistance transistor amplifier circuits and their analysis-Darlington pair amplifier, Cascode amplifier, Bootstrap emitter follower, Analysis of multi stage amplifiers using FET, Differential amplifier using BJT.

Classification of amplifiers

Depending upon the type of coupling, the multistage amplifiers are classified as :

1. Resistance and Capacitance Coupled Amplifiers (RC Coupled)
2. Transformer Coupled Amplifiers
3. Direct Coupled DC Amplifiers
4. Tuned Circuit Amplifiers.

Based upon the B. W. of the amplifiers, they can be classified as :

1. Narrow hand amplifiers
2. Untuned amplifiers

Narrow hand amplifiers: Amplification is restricted to a narrow band of frequencies around a centre frequency. There are essentially tuned amplifiers.

Untuned amplifiers: These will have large bandwidth. Amplification is desired over a considerable range of frequency spectrum.

Untuned amplifiers are further classified w.r.t bandwidth.

- | | |
|------------------------------------|-------------------|
| 1. DC amplifiers (Direct Coupled) | DC to few KHz |
| 2. Audio frequency amplifiers (AF) | 20 Hz to 20 KHz |
| 3. Broad band amplifier | DC to few MHz |
| 4. Video amplifier | 100 Hz to few MHz |

The gain provided by an amplifier circuit is not the same for all frequencies because the reactance of the elements connected in the circuit and the device reactance value depend upon

the frequency. Bandwidth of an amplifier is the frequency range over which the amplifier stage gain is reasonably constant within ± 3 db, or 0.707 of A_V Max Value.

Resistance and Capacitance Coupled Amplifiers (RC Coupled)

This type of amplifier is very widely used. It is least expensive and has good frequency response. In the multistage resistive capacitor coupled amplifiers, the output of the first stage is coupled to the next through coupling capacitor and R_L . In two stages Resistor Capacitor coupled amplifiers, there is no separate R_L between collector and ground, but R_{E0} the resistance between collector and V_{CC} (R_C) itself acts as R_L in the AC equivalent circuit.

Transformer Coupled Amplifiers

Here the output of the amplifier is coupled to the next stage or to the load through a transformer. With this overall circuit gain will be increased and also impedance matching can be achieved. But such transformer coupled amplifiers will not have broad frequency response i.e., $(f_2 - f_1)$ is small since inductance of the transformer windings will be large. So Transformer coupling is done for power amplifier circuits, where impedance matching is critical criterion for maximum power to be delivered to the load.

Direct Coupled (DC) Amplifiers

Here DC stands for direct coupled and not (direct current). In this type, there is no reactive element. L or C used to couple the output of one stage to the other. The AC output from the collector of one stage is directly given to the base of the second stage transistor directly. So type of amplifiers is used for large amplification of DC and using low frequency signals. Resistor Capacitor coupled amplifiers cannot be used for amplifications of DC or low frequency signals since X_C the capacitive reactance of the coupling capacitor will be very large or open circuit for DC

Tuned Circuit Amplifiers

In this type there will be one RC or LC tuned circuit between collector and V_{CC} in the place of R_E . These amplifiers will amplify signals of only fixed frequency f_0 which is equal to the resonance frequency of the tuned circuit LC. These are also used to amplify signals of a narrow band of frequencies centered on the tuned frequency f_0 .

Distortion in Amplifiers

If the input signal is a sine wave the output should also be a true sine wave. But in all the cases it may not be so, which we characterize as distortion. Distortion can be due to the nonlinear characteristic of the device, due to operating point not being chosen properly, due to large signal swing of the input from the operating point or due to the reactive elements L and C in the circuit. Distortion is classified as:

(a) Amplitude distortion:

This is also called non linear distortion or harmonic distortion. This type of distortion occurs in large signal amplifiers or power amplifiers. It is due to the non linearity of the characteristic of the device. This is due to the presence of new frequency signals which are not present in the input. If the input signal is of 10 KHz the output signal should also be 10 KHz signal. But some harmonic terms will also be present. Hence the amplitude of the signal (rms value) will be different $V_o \neq A_v V_i$.

(b) Frequency distortion:

The amplification will not be the same for all frequencies. This is due to reactive component in the circuit.

(c) Phase - shift delay distortion:

There will be phase shift between the input and the output and this phase shift will not be the same for all frequency signals. It also varies with the frequency of the input signal. In the output signal, all these distortions may be present or any one may be present because of which the amplifier response will not be good.

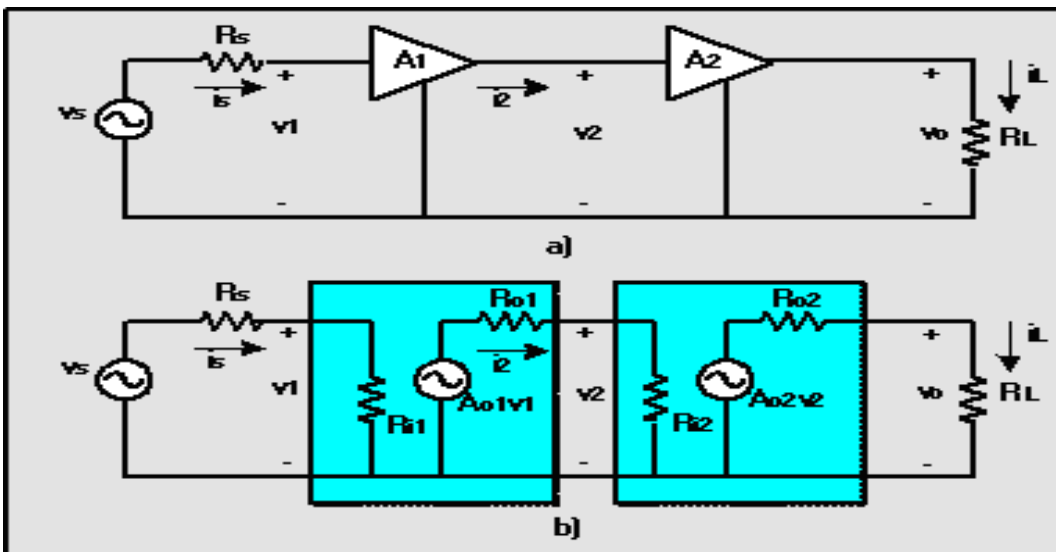
The performance obtainable from a single stage amplifier is often insufficient for many applications; hence several stages may be combined forming a multistage amplifier. These stages may be combined forming a multistage amplifier. These stages are connected in cascade, i.e. output of the first stage is connected to form input of second stage, whose output becomes input of third stage, and so on. The overall gain of a multistage amplifier is the product of the gains of the individual stage (ignoring potential loading effects):

$$\text{Gain (A)} = A_1 * A_2 * A_3 * A_4 * \dots * A_n.$$

Alternately, if the gain of each amplifier stage is expressed in decibels (dB), the total gain is the sum of the gains of the individual stages

$$\text{Gain in dB (A)} = A_1 + A_2 + A_3 + A_4 + \dots + A_n.$$

When we want to achieve higher amplification than a single stage amplifier can offer, it is a common practice to cascade various stages of amplifiers, as it is shown in Fig.1.a. In such a structure the input performance of the resulted multistage amplifier is the input performance of the first amplifier while the output performance is that of the last amplifier. It is understood that combining amplifiers of various types we can create those characteristics that are necessary to fulfill the specifications of a specific application. In addition, using feedback techniques in properly chosen multistage amplifiers can further increase this freedom of the design.



According to the small signal equivalent circuit of a two stage amplifier shown in Fig., we can calculate the ac performance of the circuit.

Voltage amplification

$$A_v = \frac{V_o}{V_1} = \frac{V_o}{V_2} \cdot \frac{V_2}{V_1} = A_{v2} \cdot A_{v1}$$

Current amplification

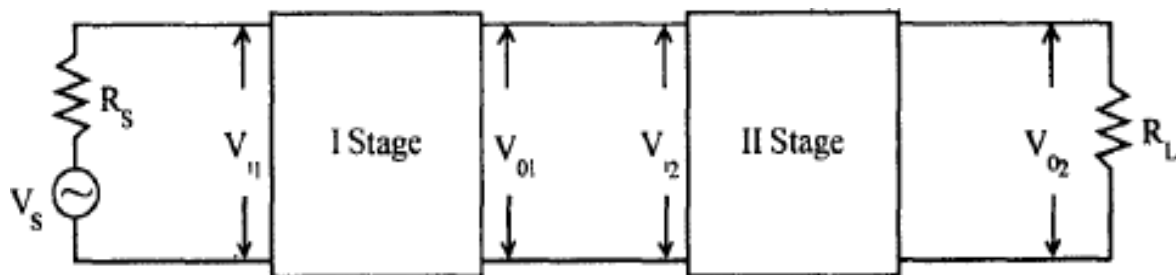
$$A_i = \frac{i_L}{i_s} = \frac{i_L}{i_2} \cdot \frac{i_2}{i_s} = A_{i2} \cdot A_{i1}$$

Power amplification

$$A_P = A_v \cdot A_i = (A_{v2} \cdot A_{i2}) \cdot (A_{v1} \cdot A_{i1}) = A_{P2} \cdot A_{P1}$$

Cascading Transistor Amplifiers

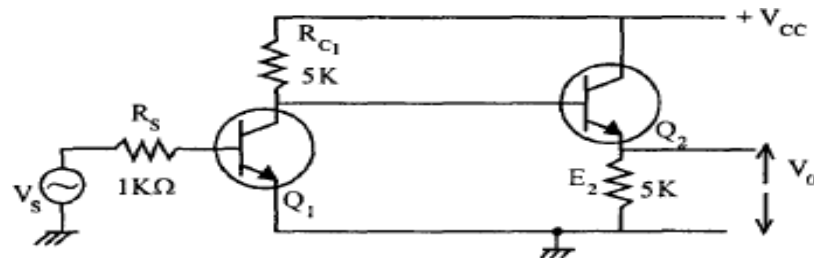
When the amplification of a single transistor is not sufficient for a particular purpose (say to deliver output to the speaker or to drive a transducer etc) or when the input or output impedance is not of the correct magnitude for the desired application, two or more stages may be connected in cascade. Cascade means in series i.e. the output of first stage is connected to the input of the next stage.



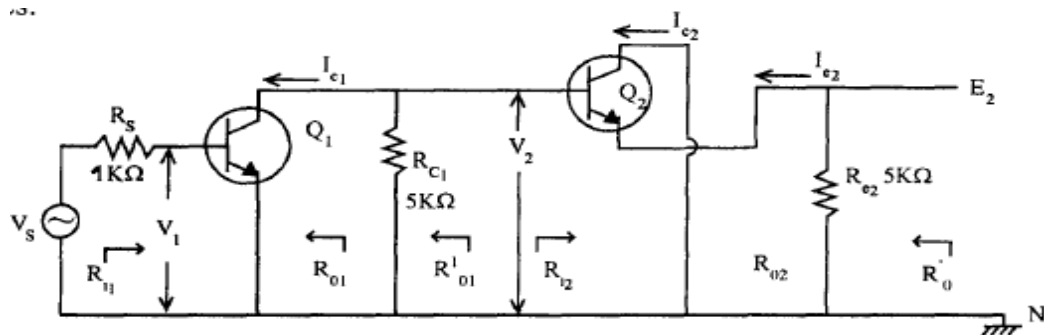
Let us consider two stage cascaded amplifier. Let the first stage is in common emitter configuration. Current gain is high and let the II stage is in common collector configuration to provide high input impedance and low output impedance. So what are the expressions for the total current gain A_i of the entire circuit (i.e. the two stages), Z_i , A_v and Y_o ? To get these expressions, we must take the h-par ammeters of these transistors in that particular configuration. Generally manufactures specify the h-parameters for a given transistor in common emitter configuration. It is widely used circuit and also A_i is high. To get the transistor h-parameters in other configurations, conversion formulae are used.

The Two Stage Cascaded Amplifier Circuit

The Transistor Q_1 is in Common Emitter configuration. The second Transistor Q_2 is in Common Collector (CC) configuration. Output is taken across $5K$, the emitter resistance. Collector is at ground potential in the A.C. equivalent circuit. Biasing resistors are not shown since their purpose is only to provide the proper operating point and they do not affect the response of the amplifier. In the low frequency equivalent circuit, since the capacitors have large value, and so is X_c low, and can be neglected. So the capacitive reactance is not considered, and capacitive reactance X_c is low when C is large and taken as short circuit.



The small signal Common Emitter configuration circuit reduces as shown in Fig. In this circuit Q_2 collector is at ground potential, in AC equivalent circuit. It is in Common Collector configuration and the output is taken between emitter point E_2 and ground. So the circuit is redrawn as shown in Figure indicating voltages at different stages and input and output resistances.



Choice of Transistor in a Cascaded Amplifier Configuration

By connecting transistor in cascade, voltage gain gets multiplied. But what type of configuration should be used? Common Collector(CC) or Common Base(CB) or Common

Emitter(CE)? To get voltage amplification and current amplification, only Common Emitter (CE) configuration is used. Since it is Common Collector amplifier, the voltage gain is less than one for each stage. So the overall amplification is less than 1.

Common Base Configuration is also not used since A_i is less than 1.

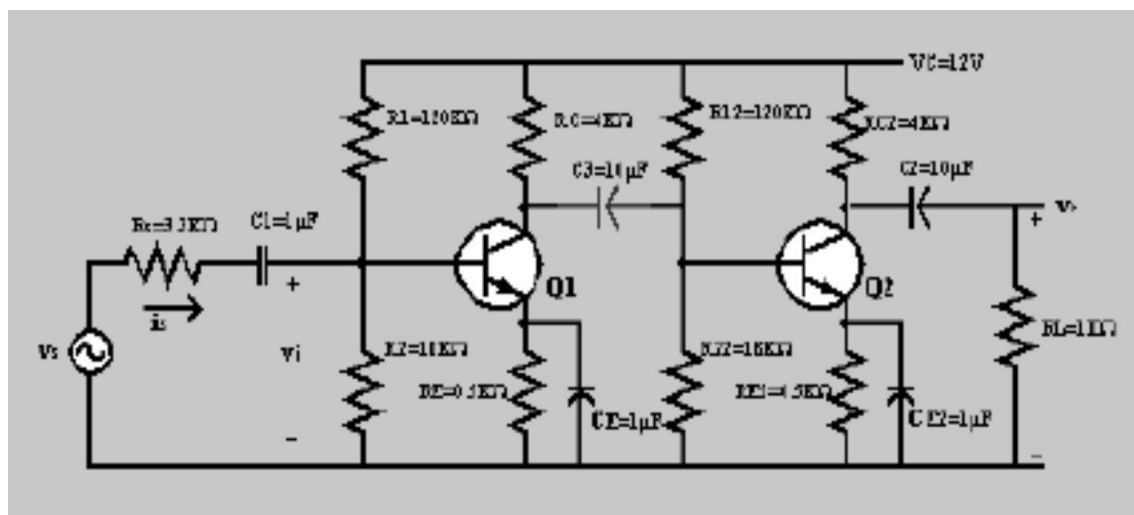
$$A_v = A_i \times \frac{R_L}{R_i}$$

Effective load resistance R_L is parallel combination of R_c and R_i of the following stage, (next stage) (since in multi stage connection, the output of one stage is the input to the other stage). This parallel combination is less than R_i . Therefore $R_L/R_i < 1$.

The current gain A_i in common base configurations is $h_{ib} < 1$ or $=1$. Therefore overall voltage gain $= 1$. Therefore Common Base configuration is not used for cascading. So only Common Emitter configuration is used ($h_{fe} \gg 1$). Therefore overall voltage gain and current gains are > 1 in Common Emitter configuration.

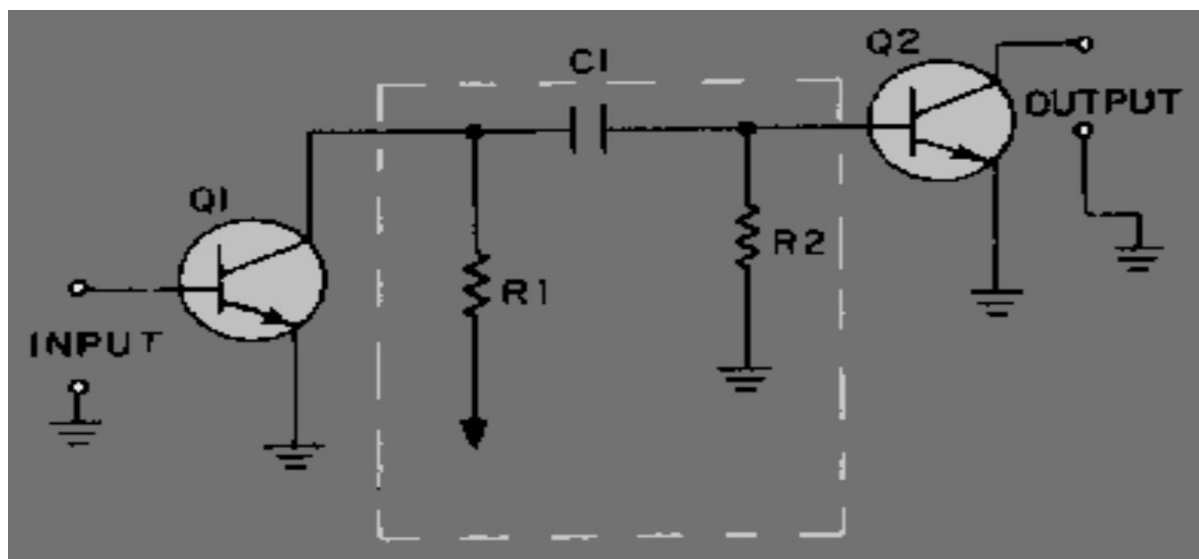
Two stage RC coupled amplifier

One way to connect various stages of a multistage amplifier is via capacitors, as indicated in the two-stage amplifier in Figure. Where two stages of common emitter amplifier are coupled to each other by the capacitor C_3 .



In RC-coupled amplifiers:

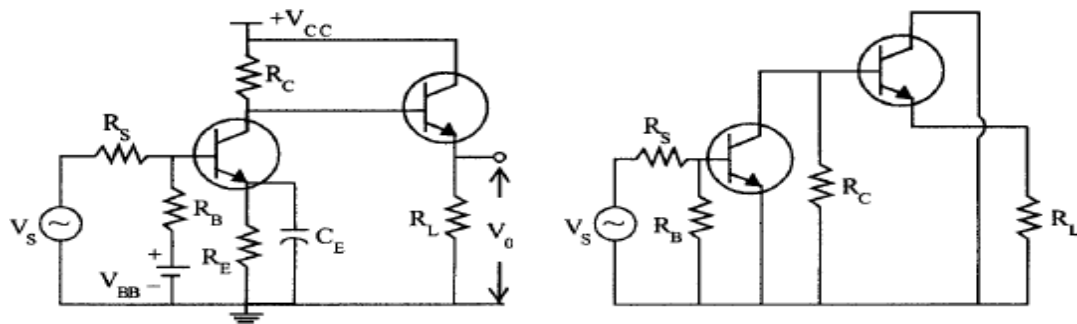
1. The various stages are DC isolated. This feature facilitates the biasing of individual stages.
2. The various stages can be similar. Hence the design of the amplifier is simplified.
3. The coupling capacitors influence the responses of the amplifier.
4. A great number of biasing resistors is necessary.



The most commonly used coupling in amplifiers is RC coupling. An RC-coupling network is shown in the illustration above. The network of R1, R2, and C1 enclosed in the dashed lines of the figure is the coupling network. You may notice that the circuitry for Q1 and Q2 is incomplete. That is intentional so that you can concentrate on the coupling network. R1 acts as a load resistor for Q1 (the first stage) and develops the output signal of that stage. Do you remember how a capacitor reacts to ac and dc? The capacitor, C1, "blocks" the dc of Q1's collector, but "passes" the ac output signal. R2 develops this passed, or coupled, signal as the input signal to Q2 (the second stage). This arrangement allows the coupling of the signal while it isolates the biasing of each stage. This solves many of the problems associated with direct coupling.

CE - CC Amplifiers

This is another type of two-stage BJT amplifier. The first stage in Common Emitter (CE) configuration provides voltage and current gains. The second stage in Common-Collector (CC) configuration provides impedance matching. This circuit is used in audio frequency amplifiers. The circuit is shown in Fig.



$$R_{L2} \simeq R_L$$

$$h_{oc} R_{L1} \leq 0.1$$

$$A_{I2} = A_{I'2} = (1 + h_{fe})$$

$$R_{i2} = (1 + h_{fe}) R_{L2}$$

$$A_{V2} = A_{V2'} = \frac{A_{I2} \cdot R_{L2}}{R_{i2}}$$

$$= \frac{(1 + h_{fe} R_{L2})}{h_{ie} + (1 + h_{fe}) R_{L2}}$$

$$= 1 - \frac{h_{ie}}{R_{i2}} ;$$

$$A_{V2} < 1$$

$$A_{I1} = A_{I1'} = -h_{fe}$$

$$R_{i1} = R_{i1'} = h_{ie}$$

$$A_{V1} = A_{V1'} = (A_{I1} \cdot R_{L1} / R_i)$$

$$A_V = A_{V_1} \cdot A'_{V_2}$$

$$R_i = R_{i_1}$$

$$R_o = R_{o_1}$$

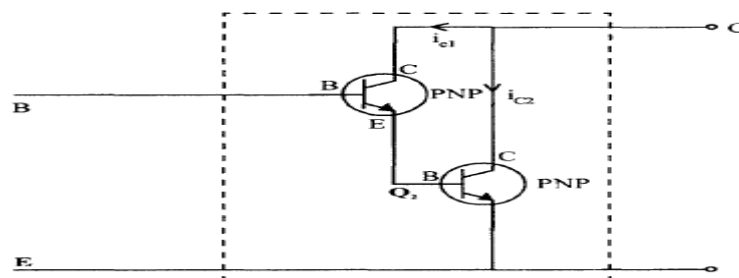
$$A_1 = \frac{A_V \cdot R_{i_1}}{R_{L_2}}$$

High Input Resistance Transistor Circuits

In some applications the amplifier circuit will have to have very high input impedance. Common Collector Amplifier circuit has high input impedance and low output impedance. But it's $A_V < 1$. If the input impedance of the amplifier circuit is to be only 500 KO or less the Common Collector Configuration can be used. But if still higher input impedance is required a circuit. This circuit is known as the Darlington Connection (named after Darlington) or Darlington Pair Circuit.

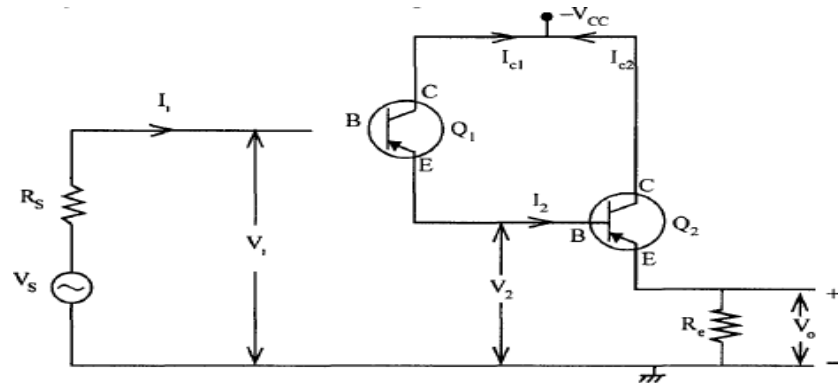
The Darlington Pair

This is two transistors connected together so that the amplified current from the first is amplified further by the second transistor. This gives the Darlington pair a very high current gain such as 10000. Darlington pairs are sold as complete packages containing the two transistors. They have three leads (B, C and E) which are equivalent to the leads of a standard individual transistor.

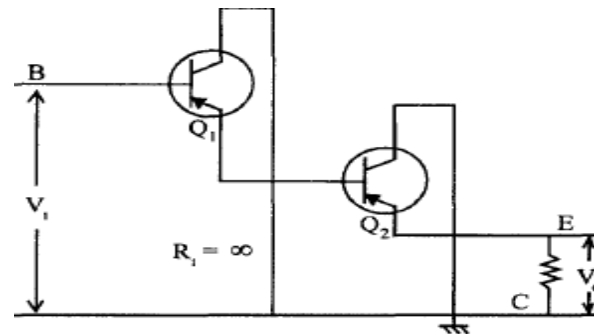


In this circuit, the two transistors are in Common Collector Configuration. The output of the first transistor Q_1 (taken from the emitter of the Q_1) is the input to the second transistor Q_2 at

the base. The input resistance of the second transistor constitutes the emitter load of the first transistor. So, Darlington Circuit is nothing but two transistors in Common Collector Configuration connected in series. The same circuit can be redrawn as AC equivalent circuit. So, DC is taken as ground shown in below Fig. Hence 'C' at ground potential, Collectors of transistors Q_1 and Q_2 is at ground potential.



There is no resistor connected between the emitter of Q_1 and ground i.e., Collector Point. So, we can assume that infinite resistance is connected between emitter and collector.



The overall current gain is equal to the two individual gains multiplied together:

Darlington pair current gain, $h_{FE} = h_{FE1} \times h_{FE2}$

Here h_{FE1} and h_{FE2} are the gains of the individual transistors

If both the transistors are identical then

Current gain

$$A_I = \frac{I_c}{I_{b1}} \cong (h_{fe})^2$$

Input resistance

$$R_i \cong \frac{(1 + h_{fe})^2 R_e}{1 + h_{oe} h_{fe} R_e}$$

Voltage gain

$$A_v \cong \left(1 - \frac{h_{ie}}{R_{i2}} \right)$$

Output resistance

$$R_{o2} = \frac{R_s + h_{ie}}{(1 + h_{fe})^2} + \frac{h_{ie}}{1 + h_{fe}}$$

Therefore, the characteristic of Darlington Circuit are

1. Very High Input Resistance
2. Very Large Current Gain
3. Very Low Output Resistance
4. Voltage Gain, $A_v < 1$.

This gives the Darlington pair a very high current gain, such as 10000, so that only a tiny base current is required to make the pair switch on.

A Darlington pair behaves like a single transistor with a very high current gain. It has three leads (B, C and E) which are equivalent to the leads of a standard individual transistor. To turn on there must be 0.7V across both the base-emitter junctions which are connected in series inside the Darlington pair, therefore it requires 1.4V to turn on.

Darlington pairs are available as complete packages but you can make up your own from two transistors; TR1 can be a low power type, but normally TR2 will need to be high power. The maximum collector current $I_{c(max)}$ for the pair is the same as $I_{c(max)}$ for TR2.

A Darlington pair is sufficiently sensitive to respond to the small current passed by your skin and it can be used to make a touch-switch as shown in the diagram. For this circuit which just lights an LED the two transistors can be any general purpose low power transistors. The 100k resistor protects the transistors if the contacts are linked with a piece of wire. Two transistors may be combined to form a configuration known as the Darlington pair which behaves like a single transistor with a current gain equivalent to the product of the current gain of the two transistors. This is especially useful where very high currents need to be controlled as in a power amplifier or power-regulator circuit. Darlington transistors are available whereby two transistors are combined in one single package. The base-emitter volt-drop is twice that of a small transistor.

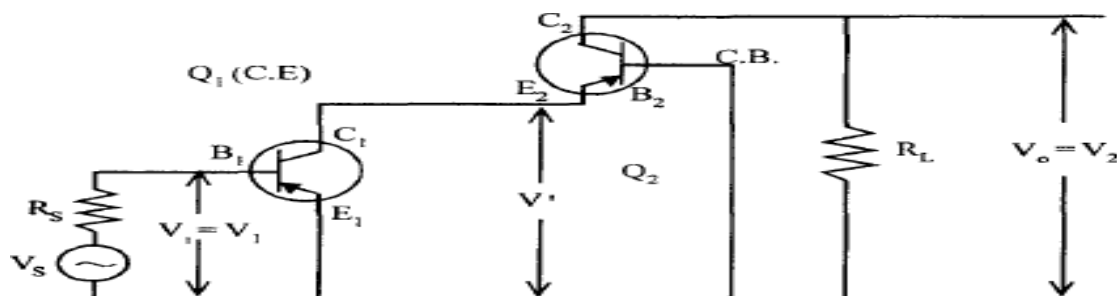
Disadvantages

1. The h-parameters for both the transistors will not be the same.
2. Leakage Current is more

The CASCODE Transistor Configuration

The circuit is shown in Figure. This transistor configuration consists of a Common Emitter Stage in cascade with a Common Base Stage. The collector current of transistor Q_1 equals the emitter current of Q_2 .

The transistor Q_1 is in Common Emitter Configuration and transistor Q_2 is in Common Base Configuration. Let us consider the input impedance (h_{11}) etc., output admittance (h_{22}) i.e. the h - parameters of the entire circuit in terms of the h- parameters of the two transistors



Input impedance

$$h_{11} = \text{Input } Z = \left. \frac{V_1}{I_1} \right|_{V_2 = 0}$$

$$h_{11} \cong h_{ie}$$

Short circuit current gain

$$h_{21} = \left. \frac{I_2}{I_1} \right|_{V_2 = 0}$$

$$h_{21} = \frac{I_2}{I_1} = \frac{I}{I_1} \times \frac{I_2}{I_0} \bigg|_{V_2 = 0}$$

$$\frac{I'}{I_1} = h_{fe} \quad \text{since, } I = I_{C1}, I_1 = I_{B1}$$

$$\frac{I_2}{I'} = -h_{fb} \quad \text{since, } I = I_{E2}, I_2 = I_{C2}$$

$$h_{21} = -h_{fe} \cdot h_{fb}$$

$$h_{fe} \gg 1 \therefore -h_{fb} \simeq 1, \quad \text{since } h_{fb} = \frac{I_C}{I_E}$$

$$\boxed{h_{21} \cong h_{fe}}$$

Output conductance

$$h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1 = 0}$$

Reverse voltage gain

$$\begin{aligned}
 h_{12} &= \left. \frac{V_1}{V_2} \right|_{I_1 = 0} \\
 &= \left. \frac{V_1}{V'} \times \frac{V'}{V_2} \right|_{I_1 = 0} \\
 \left. \frac{V_1}{V'} \right|_{I_1 = 0} &= h_{re} \cdot \left. \frac{V'}{V_2} \right| = h_{rb}
 \end{aligned}$$

$$\begin{aligned}
 h_{12} &\cong h_{re} h_{rb} \\
 h_{re} &\cong 10^{-4} \quad h_{rb} = 10^{-4} \quad \therefore h_{12} \text{ is very small} \\
 h_i = h_{11} &\cong h_{ie} \quad \text{Typical value} = 1.1 \text{ K}\Omega \\
 h_f = h_{21} &\cong h_{fe} \quad \text{Typical value} = 50 \\
 h_o = h_{22} &\cong h_{ob} \quad \text{Typical value} = 0.49 \mu \text{ A/V} \\
 h_r = h_{12} &\cong h_{re} h_{rb} \quad \text{Typical value} = 7 \times 10^{-8}
 \end{aligned}$$

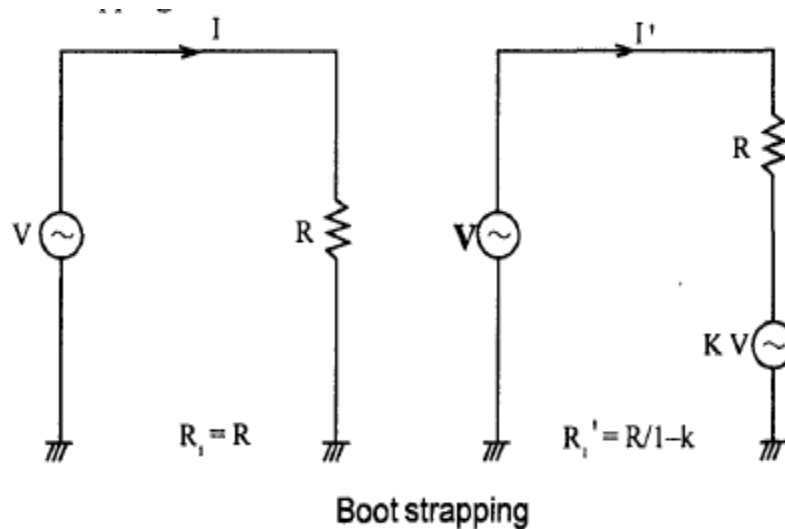
Therefore, for a CASCODE Transistor Configuration, its input Z is equal to that of a single Common Emitter Transistor (h_{ie})' Its Current Gain is equal to that of a single Common Base Transistor (h_{fe}). Its output resistance is equal to that of a single Common Base Transistor (h_{ob})' the reverse voltage gain is very small, i.e., there is no link between V_1 (input voltage) and V_2 (output voltage). In other words, there is negligible internal feedback in the case of, a CASCODE Transistor Circuit, acts like a single stage C.E. Transistor (Since h_{ie} and h_{fe} are same) with negligible internal feedback ($\therefore h_{re}$ is very small) and very small output conductance, ($= h_{ob}$) or large output resistance ($= 2 \text{ M}\Omega$ equal to that of a Common Base Stage). The above values are correct, if we make the assumption that $h_{ob} R_L < 0.1$ or R_L is $< 200 \text{ K}$.

CASCODE Amplifier will have

1. Very Large Voltage Gain.
2. Large Current Gain
3. Very High Output Resistance.

Boot-strap emitter follower

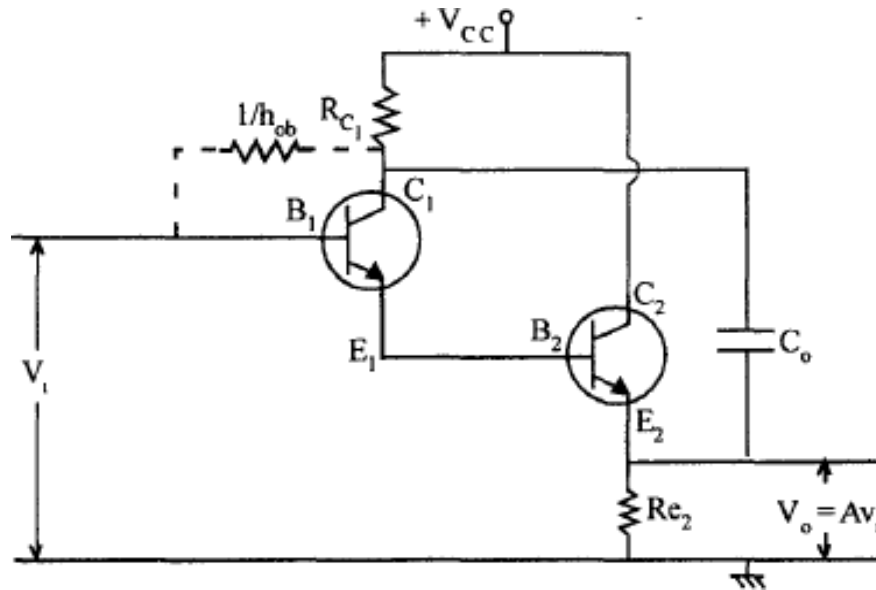
The maximum input resistance of a practical Darlington Circuit is only $2\text{ M}\Omega$. Higher input resistance cannot be achieved because of the biasing resistors R_1 , R_2 etc. They come in parallel with R_i of the transistors and thus reduce the value of R_i . The maximum value of R_i is only $1/h_{ob}$ since, h_{ob} is resistance between base and collector. The input resistance can be increased greatly by boot strapping, the Darlington Circuit through the addition of C_o between the first collector C_1 and emitter B_2 .



In Fig, V is an AC signal generator, supplying current I to R . Therefore, the input resistance of V seen by the generator is $R_i = V/I = R$ itself. Now suppose, the bottom end of R is not at ground potential but at higher potential i.e. another voltage source of KV ($K < 1$) is connected between the bottom end of R and ground. Now the input resistance of the circuit is

$$R_i' = \frac{V}{I'} \quad I' = \frac{(V - KV)}{R}$$

$$R_i' = \frac{VR}{V(1-K)} = \frac{R}{1-K}$$

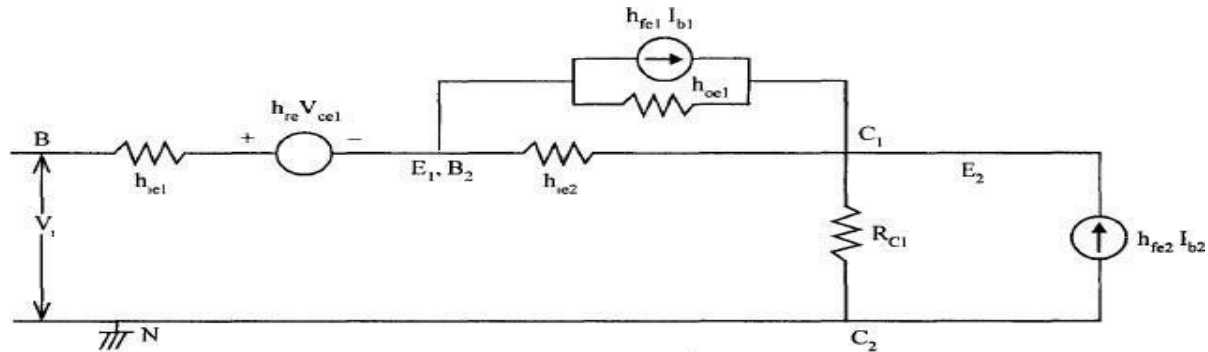


I can be increased by increasing V . When V increases KV also increases. K is constant. Therefore the potential at the two ends of R will increase by the same amount, K is less than 1, therefore $R_i > R$. Now if $K = 1$, there is no current flowing through R (So $V = KV$ there is no potential difference). So the input resistance $R_i = \infty$. Both the top and bottom of the resistor terminals are at the same potential. This is called as the Bootstrapping method which increases the input resistance of a circuit. If the potential at one end of the resistance changes, the other end of R also moves through the same potential difference. It is as if R is pulling itself up by its boot straps. For CC amplifiers $A_v < 1 = 0.95$. So R_i can be made very large by this technique. $K = A_v = 1$. If we pull the boot with both the edges of the strap (wire) the boot lifts up. Here also, if the potential at one end of R is changed, the voltage at the other end also changes or the potential level of R_3 rises, as if it is being pulled up from both the ends.

$$R_i = \frac{h_{ie}}{1 - A_v}; \quad A_v \approx 1.$$

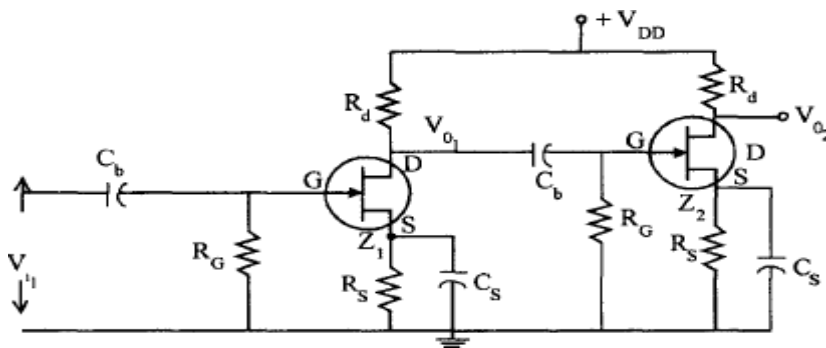
$$R_i = \frac{R}{1 - K}$$

AC Equivalent circuit



Two Stage RC Coupled JFET amplifier (in Common Source (CS) configuration)

The circuit for two stages of RC coupled amplifier in CS configuration is as shown in fig.



The output V_o of I Stage is coupled to the input V_i of II Stage through a blocking capacitor C_b . It blocks the DC components present in the output of I Stage from reaching the input of the I stage which will alter the biasing already fixed for the active device. Resistor R_g is connected between gate and ground resistor R_o is connected between drain and V_{DD} supply. C_s is the bypass capacitor used to prevent loss of gain due to negative feedback. The active device is assumed to operate in the linear region. So the small signal model of the device is valid. Frequency Roll-off is the term used for the decrease in gain with frequency in the upper cut-off region. It is expressed as db/octave or db/decade.

The purpose of multistage amplifiers is to get large gain. So with BJTs, Common Emitter Configuration is used. If JFETs are employed, common source configuration is used.

UNIT III

FET Biasing AND FET Amplifiers

FET-Biasing and FET Amplifiers: FET biasing: fixed bias and self bias. FET Amplifiers: Analysis of Common source (C.S), Common Drain (C.D) JFET Amplifiers, comparison of performance with BJT Amplifiers,

BIASING FET:-

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region. The Q point should be independent of device parameter variations and ambient temperature variations.

This can be achieved by suitably selecting the gate-to-source voltage V_{GS} and drain current I_D which is referred to as biasing.

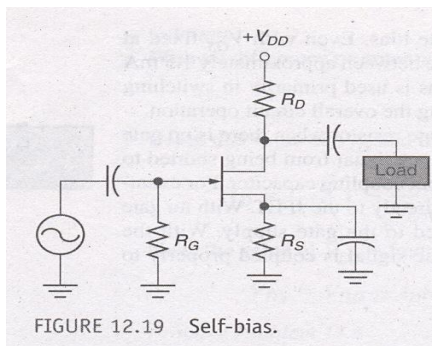
JFET biasing circuits are very similar to BJT biasing circuits. The main difference between JFET circuits and BJT circuits is the operation of the active components themselves.

There are mainly two types of biasing circuits:

- 1) Self bias
- 2) Voltage divider-bias.

SELFBIAS

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate. A self bias circuit is shown in the fig. Self bias is the most common type of JFET bias. This JFET must be operated such that gate-source junction is always reverse biased. This condition requires a negative V_{GS} for an N channel JFET and a positive V_{GS} for P channel JFET. This can be achieved using the self bias arrangement as shown in Fig. The gate resistor R_G doesn't affect the bias because it has essentially no voltage drop across it, and the gate remains at 0V. R_G is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor R_S makes gate-source junction reverse biased.



For the dc analysis coupling capacitors are open circuits. For
the N channel FET in Fig (a)

I_S produces a voltage drop across R_S and makes the source positive w.r.t ground. In any JFET circuit all the source current passes through the device to the drain circuit. This is due to the fact that there is no significant gate current.

We can define source current as $I_S = I_D$

($V_G = 0$ because there is no gate current flowing in R_G so V_G across R_G is zero) $V_G = 0$

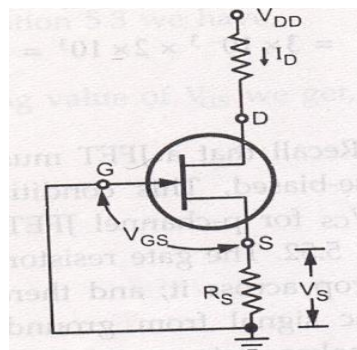
$$\text{then } V_S = I_S R_S = I_D R_S$$

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

DC analysis of self Bias:-

In the following DC analysis, the N channel JFET shown in the fig. is used for illustration.

For DC analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent. $\therefore I_G = 0$. The relation between I_D and V_{GS} is given by



$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2$$

V_{GS} for N channel JFET is $= -I_D R_S$

Substituting this value in the above equation

$$I_D = I_{DSS} \left[1 - \frac{(-I_D R_S)}{V_{GS(off)}} \right]^2$$

$$I_D = I_{DSS} \left[1 + \frac{(I_D R_S)}{V_{GS(off)}} \right]^2$$

For the N-channel FET in the above figure

I_s produces a voltage drop across R_s and makes the source positive w.r.t ground in any JFET circuit all the source current passes through the device to drain circuit this is due to the fact that there is no significant gate current. Therefore we can define source current as $I_s = I_d$ and $V_g = 0$ then

$$V_s = I_s R_s = I_d R_s$$

$$V_{gs} = V_g - V_s = 0 - I_d R_s = -I_d R_s$$

Drawing the self bias line:-

Typical transfer characteristics for a self biased JFET are shown in the fig.

The maximum drain current is 5 mA and the gate source cutoff voltage is -3V. This means the gate voltage has to be between 0 and -3V.

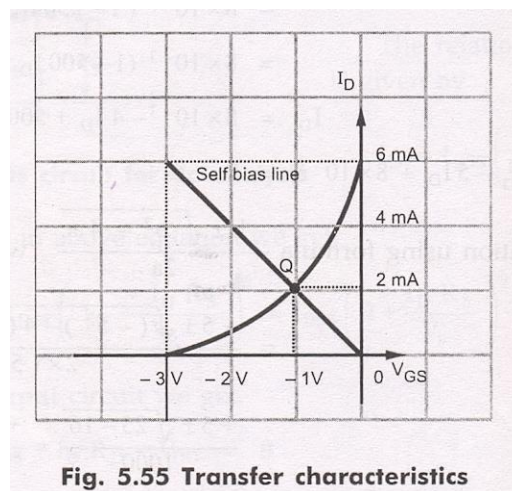


Fig. 5.55 Transfer characteristics

Now using the equation $V_{GS} = -I_D R_s$ and assuming R_s of any suitable value we can draw the self bias line.

Let us assume $R_s = 500 \Omega$

With this R_s , we can plot two points corresponding to $I_D = 0$ and $I_D = I_{DSS}$ for $I_D = 0$

$$V_{GS} = -I_D R_s$$

$$V_{GS} = 0 \times (500 \Omega) = 0 \text{ V}$$

So the first point is (0,0)

$$(I_d, V_{GS})$$

For $I_D = I_{DSS} = 5\text{mA}$

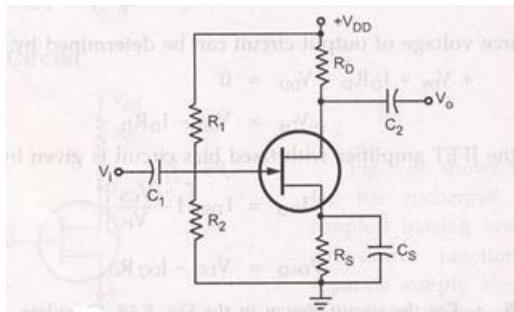
$$V_{GS} = (-5\text{mA})(500\Omega) = -3\text{V}$$

So the 2nd Point will be (5mA, -3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line. The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point, the I_D is slightly > than 2mA and V_{GS} is slightly > -1V. The Q point for the self bias JFET depends on the value of R_S . If R_S is large, Q point far down on the transconductance curve, I_D is small, when R_S is small Q point is far up on the curve, I_D is large.

VOLTAGE DIVIDER BIAS:-



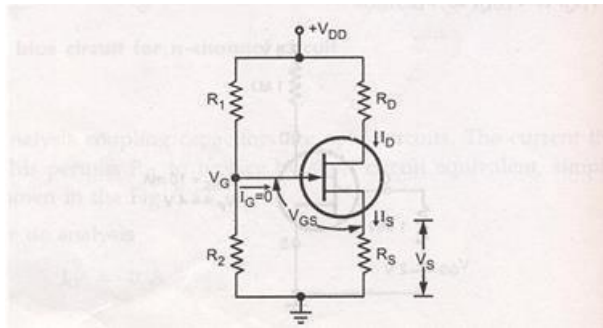
The fig. shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate to source junction reverse biased. The source voltage is

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage divider formula.

$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD}$$

For dc analysis



Applying KVL to the input circuit

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$$

$$V_{GS} = V_G - I_D R_S \quad \therefore I_S = I_D$$

Applying KVL to the output circuit we get

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

The Q-point of a JFET amplifier, using the voltage divider bias is $I_{DQ} =$

$$I_{DSS} [1 - V_{GS} / V_P]^2$$

$$V_{DSQ} = V_{DD} - I_{DQ} (R_D + R_S)$$

COMPARISON OF MOSFET WITH JFET

- In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel.
- In the JFET the transverse electric field across the reverse-biased PN junction controls the conductivity of the channel.

- c. The gate leakage current in a MOSFET is of the order of 10^{-12} A. Hence the input resistance of a MOSFET is very high in the order of 10^{10} to 10^{15} Ω . The gate leakage current of a JFET is of the order of 10^{-9} A, and its input resistance is of the order of $10^8 \Omega$.
- d. The output characteristics of the JFET are flatter than those of the MOSFET, and hence the drain resistance of a JFET (0.1 to $1 M\Omega$) is much higher than that of a MOSFET (1 to $50 k\Omega$).
- e. JFETs are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.
- f. Comparing to JFET, MOSFETs are easier to fabricate.
- g. Special digital CMOS circuits are available which involve near zero power dissipation and very low voltage and current requirements. This makes them suitable for portable systems.

FET AMPLIFIERS

INTRODUCTION

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain and high input impedance. Because of high input impedance and other characteristics of JFETs they are preferred over BJTs for certain types of applications.

There are 3 basic FET circuit configurations:

- i) Common Source
- ii) Common Drain
- iii) Common Gate

Similar to BJT CE, CC and CB circuits, only difference is in BJT large output collector current is controlled by small input base current whereas FET controls output current by means of small input voltage. In both the cases output current is controlled variable.

FET amplifier circuits use voltage controlled nature of the JFET. In Pinch off region, I_D depends only on V_{GS} .

Common Source (CS) Amplifier

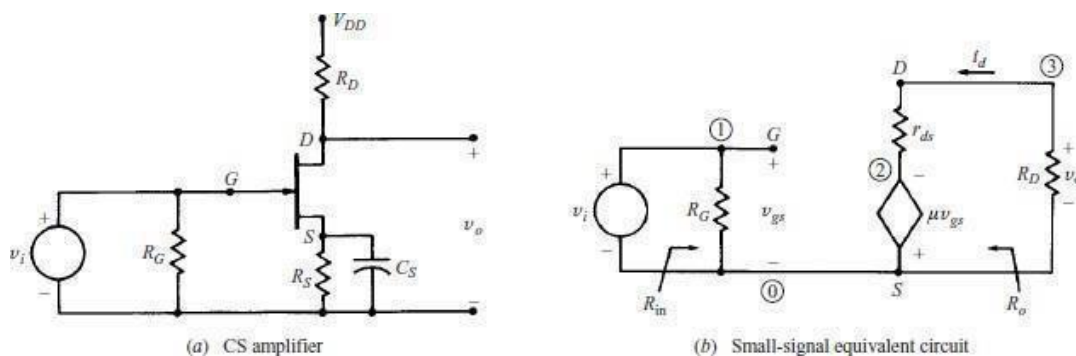


Fig.5.1(a) CS Amplifier (b) Small-signal equivalent circuit

A simple Common Source amplifier is shown in Fig. 5.1(a) and associated small signal equivalent circuit using voltage-source model of FET is shown in Fig. 5.1(b)

Voltage Gain

Source resistance (R_S) is used to set the Q-Point but is bypassed by C_S for mid-frequency operation.

From the small signal equivalent circuit, the output voltage $V_o = -$

$$R_D \mu V_{gs} (R_D + r_d)$$

Where $V_{gs} = V_i$, the input voltage, Hence,

the voltage gain,

$$A_v = V_o / V_i = -R_D \mu (R_D + r_d)$$

Input Impedance

From Fig. 5.1(b) Input Impedance is $Z_i =$

$$R_G$$

For voltage divider bias as in CE Amplifiers of BJT

$$R_G = R_1 \parallel R_2$$

Output Impedance

Output impedance is the impedance measured at the output terminals with the input voltage $V_i = 0$

From the Fig. 5.1(b) when the input voltage $V_i = 0$, $V_{gs} = 0$ and hence

$$\mu V_{gs} = 0$$

The equivalent circuit for calculating output impedance is given in Fig. 5.2. Output

impedance $Z_o = r_d \parallel R_D$

Normally r_d will be far greater than R_D . Hence $Z_o \approx R_D$

Common Drain Amplifier

A simple common drain amplifier is shown in Fig. 5.2(a) and associated small signal equivalent circuit using the voltage source model of FET is shown in Fig. 5.2(b). Since voltage V_{gd} is more easily determined than V_{gs} , the voltage source in the output circuit is expressed in terms of V_{gs} and Thevenin's theorem.

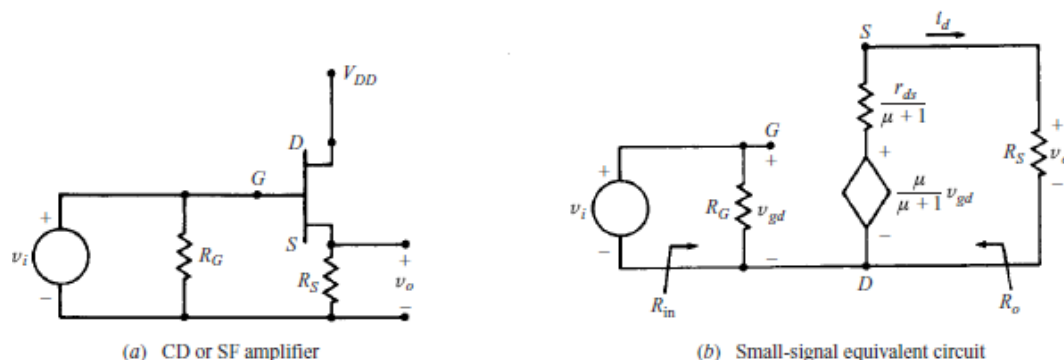


Fig.5.2(a) CD Amplifier (b) Small-signal equivalent circuit

Voltage Gain

The output voltage,

$$V_O = R_S \mu V_{gd} / (\mu + 1) R_S +$$

r_d Where $V_{gd} = V_i$ the input voltage.

Hence, the voltage gain,

$$A_v = V_O / V_i = R_S \mu / (\mu + 1) R_S + r_d$$

Input Impedance

From Fig. 5.2(b), Input Impedance $Z_i = R_G$

Output Impedance

From Fig. 5.2(b), Output impedance measured at the output terminals with input voltage $V_i = 0$ can be calculated from the following equivalent circuit.

As $V_i = 0$: $V_{gd} = 0$: $\mu v_{gd} / (\mu + 1) = 0$ Output

Impedance

$$Z_O = r_d / (\mu + 1) \parallel R_S$$

When $\mu \gg 1$

$$Z_O = (r_d / \mu) \parallel R_S = (1 / g_m) \parallel R_S$$

BIASING FET

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region. The Q point should be independent of device parameter variations and ambient temperature variations.

This can be achieved by suitably selecting the gate-to-source voltage V_{GS} and drain current I_D which is referred to as biasing.

JFET biasing circuits are very similar to BJT biasing circuits. The main difference between JFET circuits and BJT circuits is the operation of the active components themselves.

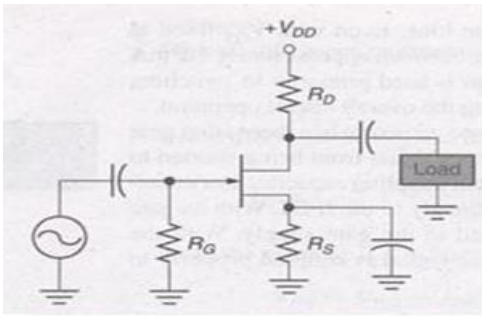
There are mainly two types of Biasing circuits

1. Self bias
2. Voltage divider bias.

5.13.1. SELF BIAS:-

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate.

A self bias circuit is shown in the fig 5.3



Self bias is the most common type of JFET bias.

This JFET must be operated such that the gate-source junction is always reverse biased.

This condition requires a negative V_{GS} for an N-channel JFET and a positive V_{GS} for a P-channel JFET. This can be achieved using the self bias arrangement as shown in Fig 5.3.

The gate resistor R_G doesn't affect the bias because it has essentially no voltage drop across it, and the gate remains at 0V. R_G is necessary only to isolate an AC signal from ground in amplifier applications. The voltage drop across resistor R_S makes the gate-source junction reverse biased.

DC analysis of self Bias:-

In the following DC analysis, the N-channel JFET shown in the fig 5.4 is used for illustration.

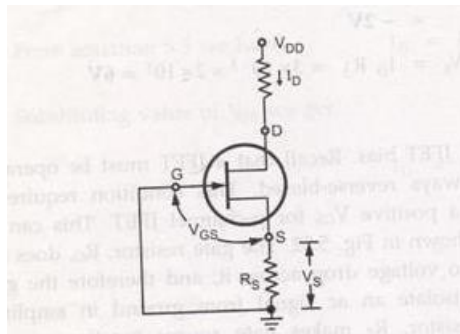
For DC analysis we can replace coupling capacitors by open circuits and resistor R_G by a short circuit equivalent.

we can also replace the

$$\therefore I_G = 0$$

The relation between I_D and V_{GS} is given by

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$



V_{GS} for N channel JFET is $= -I_D R_S$

Substituting this value in the above equation

$$I_D = I_{DSS} \left[1 - \frac{(-I_D R_S)}{V_P} \right]^2$$

$$I_D = I_{DSS} \left[1 + \frac{(I_D R_S)}{V_P} \right]^2$$

For the N-channel JFET in the above figure

I_S produces a voltage drop across R_S and makes the source positive w.r.t. ground

In any JFET circuit all the source current passes through the device to drain circuit. This is due to the fact that there is no significant gate current.

Therefore we can define source current as $I_S = I_D$ and $V_G = 0$ then $V_S = I_S R_S$

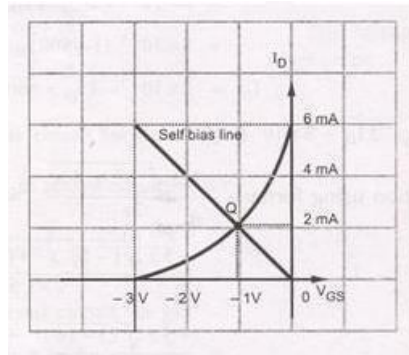
$$R_S = I_D R_S$$

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

Drawing the self bias line:-

Typical transfer characteristics for a self-biased JFET are shown in the figure 5.5 below:

The maximum drain current is 6 mA and the gate-source cutoff voltage is -3V. This means the gate voltage has to be between 0 and -3V.



Now using the equation $V_{GS} = -I_D R_S$ and assuming R_S of any suitable value we can draw the self-bias line.

Let us assume $R_S = 500 \Omega$

With this R_S , we can plot two points corresponding to $I_D = 0$ and $I_D = I_{DSS}$ for

$$I_D = 0$$

$$V_{GS} = -I_D R_S$$

$$V_{GS} = 0 \times (500 \Omega) = 0V$$

So the first point is (0,0)

(I_d, V_{GS})

For $I_D = I_{DSS} = 6\text{mA}$

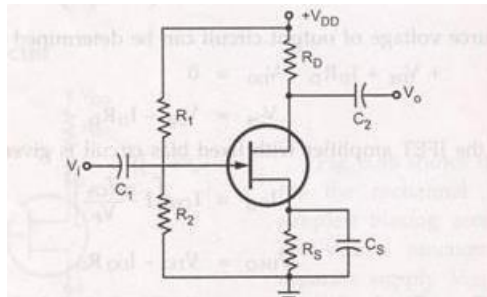
$V_{GS} = (-6\text{mA})(500\Omega) = -3\text{V}$

So the 2nd point will be (6mA, -3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line. The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point, the I_D is slightly > than 2mA and V_{GS} is slightly > -1V. The Q point for the self bias JFET depends on the value of R_S . If R_S is large, Q point far down on the transconductance curve, I_D is small, when R_S is small Q point is far up on the curve, I_D is large.

5.13.2 VOLTAGE DIVIDER BIAS:-



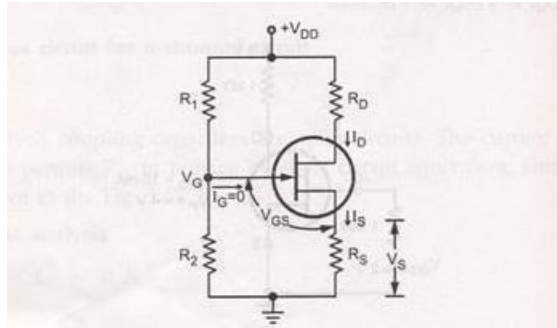
The fig 5.6 shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate-to-source junction reverse biased. The source voltage is

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage divider formula.

$$V_G = V_{DD} \left(\frac{R_2}{R_1 + R_2} \right)$$

Fordcanalysisfig5.5



ApplyingKVLtotheinputcircuit

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$$

$$V_{GS} = V_G - I_D R_S \quad \therefore I_S = I_D$$

ApplyingKVLtotheinputcircuitweget

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

The Q point of a JFET amplifier, using the voltage divider bias is $I_{DQ} = I_{DSS} [1 - V_{GS}/V_P]^2$

$$V_{DSQ} = V_{DD} - I_{DQ} (R_D + R_S)$$

UNIT IV

FEEDBACK AMPLIFIERS

Concept of Feedback and types, Effects of negative feedback on amplifiers characteristics, voltage series, current series, current shunt, and voltage shunt feedback amplifiers.

A practical amplifier has a gain of nearly one million *i.e.* its output is one million times the input. Consequently, even a casual disturbance at the input will appear in the amplified form in the output. There is a strong tendency in amplifiers to introduce *hum* due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output. The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible. The noise level in amplifiers can be reduced considerably by the use of *negative feedback* *i.e.* by injecting a fraction of output in phase opposition to the input signal. The object of this chapter is to consider the effects and methods of providing negative feedback in transistor amplifiers.

Ideally an amplifier should reproduce the input signal, with change in magnitude and without change in phase. But some of the shortcomings of the amplifier circuit are

1. Change in the value of the gain due to variation in supplying voltage, temperature or due to components.
2. Distortion in wave-form due to nonlinearities in the operating characters of the Amplifying device.
3. The amplifier may introduce noise (undesired signals)

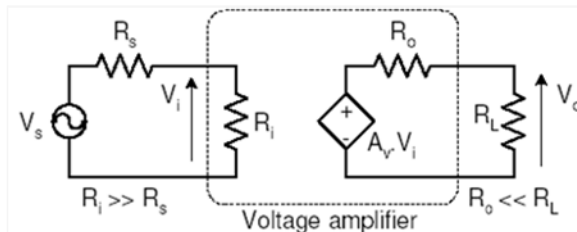
The above drawbacks can be minimized if we introduce feedback.

CLASSIFICATION OF AMPLIFIERS

Amplifiers can be classified broadly as:

1. Voltage amplifiers.
2. Current amplifiers.
3. Transconductance amplifiers.
4. Transresistance amplifiers.

1.1 Voltage amplifier



if $R_i \gg R_s$

then $V_i \approx V_s$

and if $R_o \ll R_L$

then

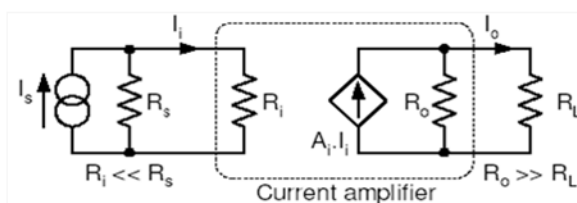
$$V_o \approx A_v V_i \approx A_v V_s$$

hence $A_v \equiv \frac{V_o}{V_i}$

with $R_L = \infty$

represent the open circuit voltage gain.

1.2 Current amplifier



if $R_i \ll R_s$

then $I_i \approx I_s$

and if $R_o \gg R_L$

then

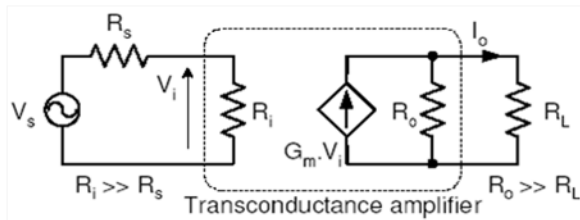
$$I_o \approx A_i I_i \approx A_i I_s$$

hence $A_i \equiv \frac{I_o}{I_i}$

with $R_L = 0$

represent the short circuit current gain.

1.3 Transconductance amplifier



if $R_i \gg R_s$

then $V_i \approx V_s$

and if $R_o \gg R_L$

then

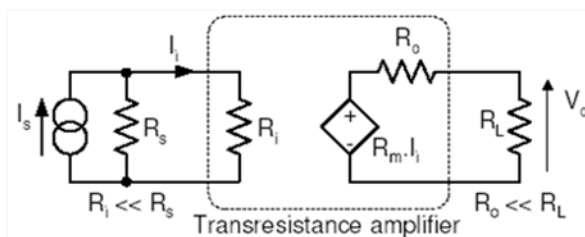
$$I_o \approx G_m V_i \approx G_m V_s$$

hence $G_m \equiv \frac{I_o}{V_i}$

with $R_L = 0$

represent the short circuit mutual or transfer conductance

1.4 Transresistance amplifier



if $R_i \ll R_s$

then $I_i \approx I_s$

and if $R_o \ll R_L$

then

$$V_o \approx R_m I_i \approx R_m I_s$$

hence $R_m \equiv \frac{V_o}{I_i}$

with $R_L = \infty$

represent the open circuit mutual or transfer resistance.

Concept of Feedback

An amplifier circuit simply increases the signal strength. But while amplifying, it just increases the strength of its input signal whether it contains information or some noise along with information. This noise or some disturbance is introduced in the amplifiers because of their strong tendency to introduce hum due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output, which is very undesirable.

The noise level in the amplifier circuits can be considerably reduced by using negative feedback done by injecting a fraction of output in phase opposition to the input signal.

Principle of Feedback Amplifier

A feedback amplifier generally consists of two parts. They are the amplifier and the feedback circuit. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure.

From the above figure, the gain of the amplifier is represented as A . the gain of the amplifier is the ratio of output voltage V_o to the input voltage V_i . the feedback network extracts a voltage $V_f = \beta V_o$ from the output V_o of the amplifier.

This voltage is added for positive feedback and subtracted for negative feedback, from the signal voltage V_s . Now,

$$V_i = V_s + V_f = V_s + \beta V_o$$

$$V_i = V_s - V_f = V_s - \beta V_o$$

The quantity $\beta = V_f / V_o$ is called as feedback ratio or feedback fraction.

Let us consider the case of negative feedback. The output V_o must be equal to the input voltage $(V_s - \beta V_o)$ multiplied by the gain A of the amplifier.

Hence,

$$(V_s - \beta V_o)A = V_o$$

Or

$$AV_s - A\beta V_o = V_o$$

Or

$$AV_s = V_o(1 + A\beta)$$

Therefore,

$$\frac{V_o}{V_s} = \frac{A}{1 + A\beta}$$

Let A_f be the overall gain (gain with the feedback) of the amplifier. This is defined as the ratio of output voltage V_o to the applied signal voltage V_s , i.e.,

$$A_f = \frac{A}{1 + A\beta}$$

The equation of gain of the feedback amplifier, with positive feedback is given by

$$A_f = \frac{A}{1 - A\beta}$$

These are the standard equations to calculate the gain of feedback amplifiers.

Types of Feedbacks

The process of injecting a fraction of output energy of some device back to the input is known as Feedback. It has been found that feedback is very useful in reducing noise and making the amplifier operation stable.

Depending upon whether the feedback signal aids or opposes the input signal, there are two types of feedbacks used.

Positive Feedback

The feedback in which the feedback energy, i.e., either voltage or current is in phase with the input signal and thus aids it is called as Positive feedback.

Both the input signal and feedback signal introduce a phase shift of 180° thus making a 360° resultant phase shift around the loop, to be finally in phase with the input signal.

Though the positive feedback increases the gain of the amplifier, it has the disadvantages such as

- Increasing distortion
- Instability

It is because of these disadvantages the positive feedback is not recommended for the amplifiers. If the positive feedback is sufficiently large, it leads to oscillations, by which oscillator circuits are formed.

Negative Feedback

The feedback in which the feedback energy i.e., either voltage or current is out of phase with the input and thus opposes it, is called as negative feedback.

In negative feedback, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is designed that it produces no phase shift or zero phase shift. Thus the resultant feedback voltage V_f is 180° out of phase with the input signal V_{in} .

Though the gain of negative feedback amplifier is reduced, there are many advantages of negative feedback such as

- Stability of gain is improved
- Reduction in distortion
- Reduction in noise
- Increase in input impedance
- Decrease in output impedance
- Increase in the range of uniform application

It is because of these advantages negative feedback is frequently employed in amplifiers.

Negative feedback in an amplifier is the method of feeding a portion of the amplified output to the input but in opposite phase. The phase opposition occurs as the amplifier provides 180° phase shift whereas the feedback network doesn't.

While the output energy is being applied to the input, for the voltage energy to be taken as feedback, the output is taken in shunt connection and for the current energy to be taken as feedback, the output is taken in series connection.

There are two main types of negative feedback circuits. They are–

- Negative Voltage Feedback
- Negative Current Feedback

Negative Voltage Feedback

In this method, the voltage feedback to the input of amplifier is proportional to the output voltage. This is further classified into two types –

- Voltage-series feedback
- Voltage-shunt feedback

Negative Current Feedback

In this method, the voltage feedback to the input of amplifier is proportional to the output current. This is further classified into two types.

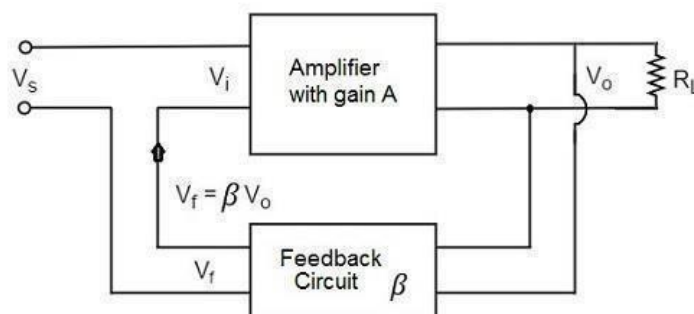
- Current-series feedback
- Current-shunt feedback

Let us have a brief idea on all of them.

Voltage-Series Feedback

In the voltage series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as shunt-driven series-fed feedback, i.e., a parallel-series circuit.

The following figure shows the block diagram of voltage series feedback, by which it is evident that the feedback circuit is placed in shunt with the output but in series with the input.

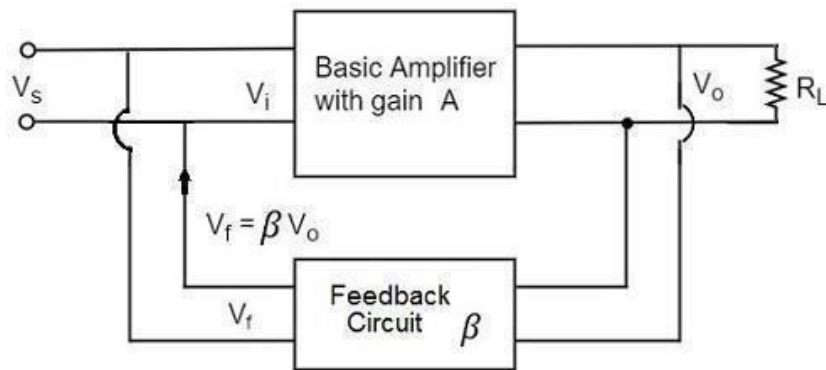


As the feedback circuit is connected in shunt with the output, the output impedance is decreased and due to the series connection with the input, the input impedance is increased.

Voltage-Shunt Feedback

In the voltage shunt feedback circuit, a fraction of the output voltage is applied in parallel with the input voltage through the feedback network. This is also known as shunt-driven shunt-fed feedback i.e., a parallel-parallel proto type.

The below figure shows the block diagram of voltage shunt feedback, by which it is evident that the feedback circuit is placed in shunt with the output and also with the input.

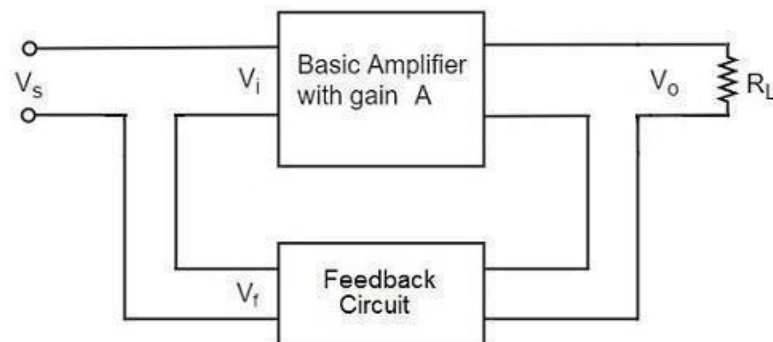


As the feedback circuit is connected in shunt with the output and the input as well, both the output impedance and the input impedance are decreased.

Current-Series Feedback

In the current series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as series-driven series-fed feedback i.e., a series-series circuit.

The following figure shows the block diagram of current series feedback, by which it is evident that the feedback circuit is placed in series with the output and also with the input.



As the feedback circuit is connected in series with the output and the input as well, both the output impedance and the input impedance are increased.

UNIT –V

OSCILLATORS:

Classification of oscillators, Barkhausen criterion, RC phase shift oscillator, Wein-bridge oscillator, LC oscillators- Hartley and Colpitts oscillator.

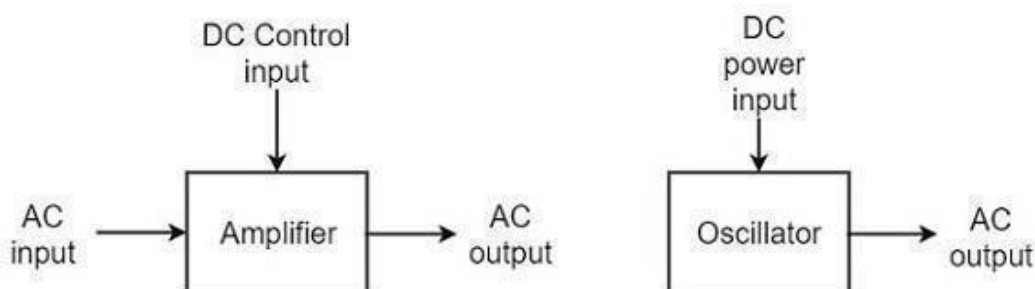
Oscillators:

An **oscillator** generates output without any ac input signal. An electronic oscillator is a circuit which converts dc energy into ac at a very high frequency. An amplifier with a positive feedback can be understood as an oscillator.

Amplifier vs. Oscillator

An **amplifier** increases the signal strength of the input signal applied, whereas an **oscillator** generates a signal without that input signal, but it requires dc for its operation. This is the main difference between an amplifier and an oscillator.

Take a look at the following illustration. It clearly shows how an amplifier takes energy from d.c. power source and converts it into a.c. energy at signal frequency. An oscillator produces an oscillating a.c. signal on its own.



The frequency, waveform, and magnitude of a.c. power generated by an amplifier, is controlled by the a.c. signal voltage applied at the input, whereas those for an oscillator are controlled by the components in the circuit itself, which means no external controlling voltage is required.

Alternator vs. Oscillator

An **alternator** is a mechanical device that produces sinusoidal waves without any input. This a.c. generating machine is used to generate frequencies up to 1000 Hz. The output frequency depends on the number of poles and the speed of rotation of the armature.

The following points highlight the differences between an alternator and an oscillator–

- An alternator converts mechanical energy to a.c. energy, whereas the oscillator converts d.c. energy into a.c. energy.
- An oscillator can produce higher frequencies of several MHz whereas an alternator cannot.
- An alternator has rotating parts, whereas an electronic oscillator doesn't.
- It is easy to change the frequency of oscillations in an oscillator than in an alternator.

Oscillators can also be considered as opposites to rectifiers that convert a.c. to d.c. as these convert d.c. to a.c.

Classification of Oscillators

Electronic oscillators are classified mainly into the following two categories–

- **Sinusoidal Oscillators** – The oscillators that produce an output having a sine waveform are called **sinusoidal** or **harmonic oscillators**. Such oscillators can provide output at frequencies ranging from 20 Hz to 1 GHz.
- **Non-sinusoidal Oscillators** – The oscillators that produce an output having a square, rectangular or saw-tooth waveform are called **non-sinusoidal** or **relaxation oscillators**. Such oscillators can provide output at frequencies ranging from 0 Hz to 20 MHz.

Sinusoidal Oscillators

Sinusoidal oscillators can be classified in the following categories–

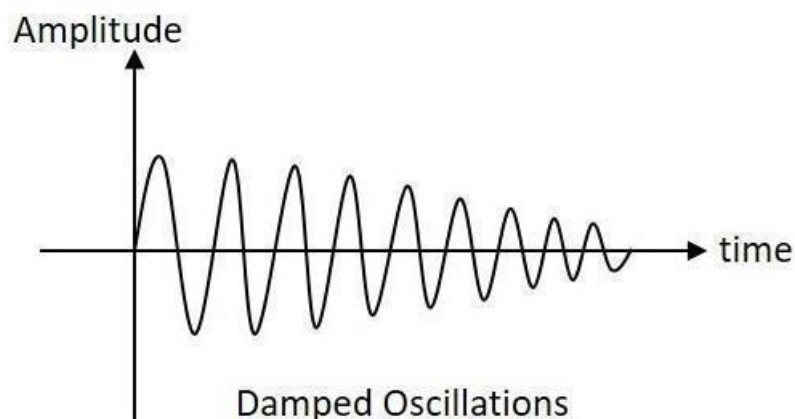
- **Tuned Circuit Oscillators** – These oscillators use a tuned-circuit consisting of inductors (L) and capacitors (C) and are used to generate high-frequency signals. Thus they are also known as radio frequency R.F. oscillators. Such oscillators are Hartley, Colpitts, Clapp-oscillators etc.
- **RC Oscillators** – These oscillators use resistors and capacitors and are used to generate low or audio-frequency signals. Thus they are also known as audio-frequency (A.F.) oscillators. Such oscillators are Phase –shift and Wein-bridge oscillators.
- **Crystal Oscillators** – These oscillators use quartz crystals and are used to generate highly stabilized output signal with frequencies up to 10MHz. The Piezo oscillator is an example of a crystal oscillator.
- **Negative-resistance Oscillator** – These oscillators use negative-resistance characteristic of the devices such as tunnel devices. A tuned diode oscillator is an example of a negative-resistance oscillator.

Nature of Sinusoidal Oscillations

The nature of oscillations in a sinusoidal wave is generally of two types. They are **damped** and **undamped oscillations**.

Damped Oscillations

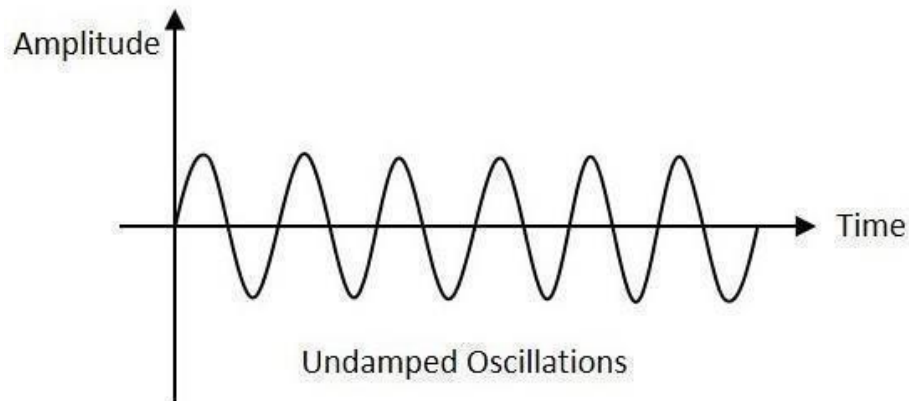
The electrical oscillations whose amplitude goes on decreasing with time are recalled as **Damped Oscillations**. The frequency of the damped oscillations may remain constant depending upon the circuit parameters.



Damped oscillations are generally produced by the oscillatory circuits that produce power losses and doesn't compensate if required.

Undamped Oscillations

The electrical oscillations whose amplitude remains constant with time are called as **Undamped Oscillations**. The frequency of the undamped oscillations remains constant.



Undamped oscillations are generally produced by the oscillatory circuits that produce no power losses and follow compensation techniques if any power losses occur.

An amplifier with positive feedback produces its output to be in phase with the input and increases the strength of the signal. Positive feedback is also called as **degenerative feedback** or **direct feedback**. This kind of feedback makes a feedback amplifier, an oscillator.

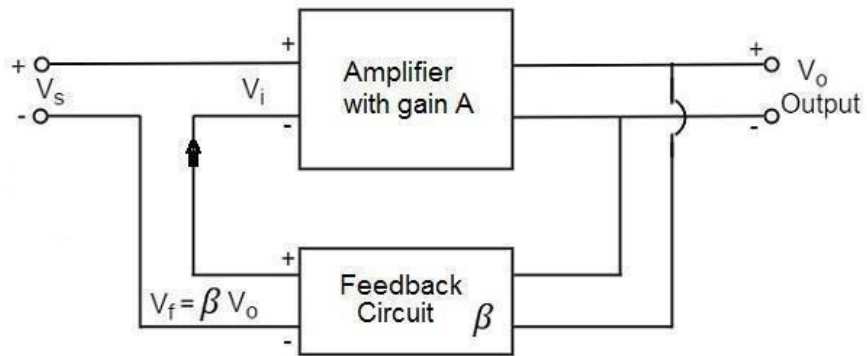
The use of positive feedback results in a feedback amplifier having closed-loop gain greater than the open-loop gain. It results in **instability** and operates as an oscillatory circuit. An oscillatory circuit provides a constantly varying amplified output signal of any desired frequency.

The Barkhausen Criterion

With the knowledge we have till now, we understood that a practical oscillator circuit consists of a tank circuit, a transistor amplifier circuit, and a feedback circuit. So, let us now try to brush up the concept of feedback amplifiers, to derive the gain of the feedback amplifiers.

Principle of Feedback Amplifier

A feedback amplifier generally consists of two parts. They are the **amplifier** and the **feedback circuit**. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure below.



From the above figure, the gain of the amplifier is represented as A . The gain of the amplifier is the ratio of output voltage V_o to the input voltage V_i . The feedback network extracts a voltage $V_f = \beta V_o$ from the output V_o of the amplifier.

This voltage is added for positive feedback and subtracted for negative feedback, from the signal voltage V_s .

So, for a positive feedback,

$$V_i = V_s + V_f = V_s + \beta V_o$$

The quantity $\beta = V_f/V_o$ is called as feedback ratio or feedback fraction.

The output V_o must be equal to the input voltage $(V_s + \beta V_o)$ multiplied by the gain A of the amplifier.

Hence,

$$(V_s + \beta V_o)A = V_o$$

Or

$$AV_s + A\beta V_o = V_o$$

Or

$$AV_s = V_o(1 - A\beta)$$

Therefore

$$\frac{V_o}{V_s} = \frac{A}{(1 - A\beta)}$$

Let A_f be the overall gain (gain with the feedback) of the amplifier. This is defined as the ratio of output voltage V_o to the applied signal voltage V_s , i.e.,

$$A_f = \frac{V_o}{V_s}$$

from the above two equations, we can understand that, the equation of gain of the feedback amplifier A with positive feedback is given by

$$A_f = \frac{A}{1 - A\beta}$$

Where $A\beta$ is the feedback factor or the loop gain.

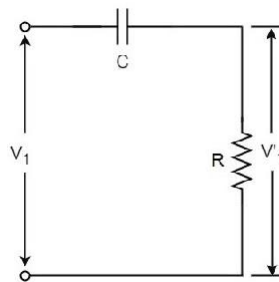
If $A\beta = 1$, $A_f = \infty$. Thus the gain becomes infinity, i.e., there is output without any input. In other words, the amplifier works as an Oscillator.

The condition $A\beta = 1$ is called as **Barkhausen Criterion of oscillations**. This is a very important factor to be always kept in mind, in the concept of Oscillators

RC-Phase-shift Oscillators

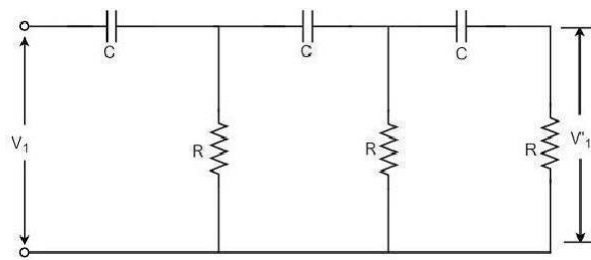
Principle of Phase-shift oscillators

We know that the output voltage of an RC circuit for a sinewave input leads the input voltage. The phase angle by which it leads is determined by the value of RC components used in the circuit. The following circuit diagram shows a single section of an RC network.



The output voltage V_1' across the resistor R leads the input voltage applied input V_1 by some phase angle ϕ° . If R were reduced to zero, V_1' will lead the V_1 by 90° i.e., $\phi^\circ = 90^\circ$.

However, adjusting R to zero would be impracticable, because it would lead to no voltage across R . Therefore, in practice, R is varied to such a value that makes V_1' to lead V_1 by 60° . The following circuit diagram shows the three sections of the RC network.



Each section produces a phase shift of 60° . Consequently, a total phase shift of 180° is produced, i.e., voltage V_2 leads the voltage V_1 by 180° .

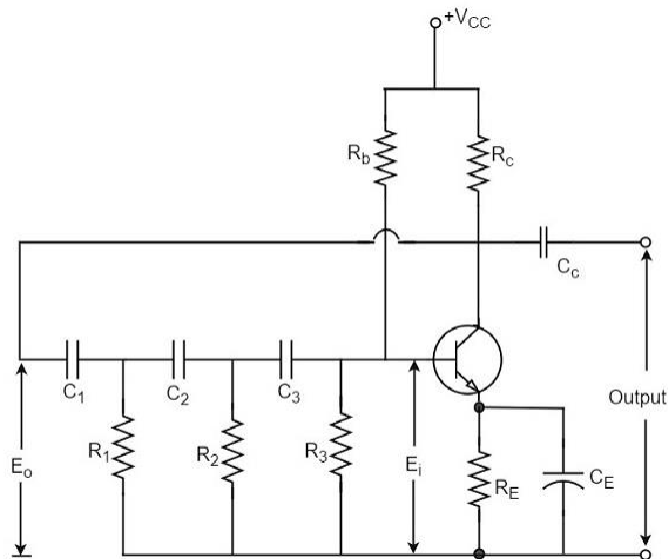
Phase-shift Oscillator Circuit

The oscillator circuit that produces a sine wave using a phase-shift network is called as a Phase-shift oscillator circuit. The constructional details and operation of a phase-shift oscillator circuit are as given below.

Construction

The phase-shift oscillator circuit consists of a single transistor amplifier section and a RC phase-shift network. The phase shift network in this circuit, consists of three RC sections. At the resonant frequency f_o , the phase shift in each RC section is 60° so that the total phase shift produced by RC network is 180° .

The following circuit diagram shows the arrangement of an RC phase-shift oscillator.



The frequency of oscillations is given by

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

Where

$$R_1 = R_2 = R_3 = R$$

$$C_1 = C_2 = C_3 = C$$

Operation

The circuit when switched ON oscillates at the resonant frequency f_o . The output E_o of the amplifier is fed back to RC feedback network. This network produces a phase shift of 180° and a voltage E_i appears at its output. This voltage is applied to the transistor amplifier.

The feedback applied will be

$$m = E_i/E_o$$

The feedback is in correct phase, whereas the transistor amplifier, which is in CE configuration, produces a 180° phase shift. The phase shift produced by network and the transistor add to form a phase shift around the entire loop which is 360° .

Advantages

The advantages of RC phase shift oscillator are as follows–

- It does not require transformers or inductors.
- It can be used to produce very low frequencies.
- The circuit provides good frequency stability.

Disadvantages

The disadvantages of RC phase shift oscillator are as follows–

- Starting the oscillations is difficult as the feedback is small.
- The output produced is small.

Another type of popular audio frequency oscillator is the Wien bridge oscillator circuit. This is mostly used because of its important features. This circuit is free from the **circuit fluctuations** and the **ambient temperature**.

The main advantage of this oscillator is that the frequency can be varied in the range of 10 Hz to about 1 MHz whereas in RC oscillators, the frequency is not varied.

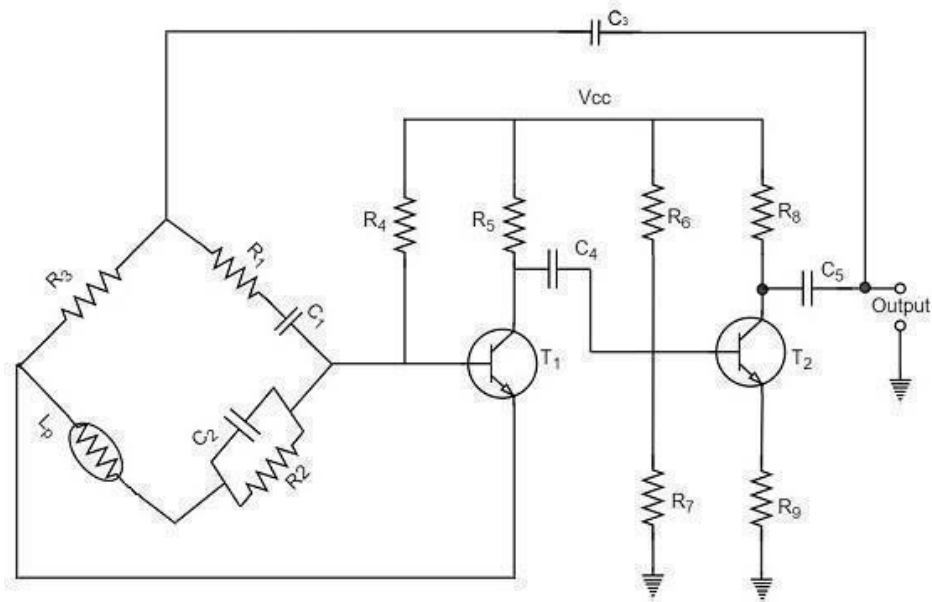
Wien bridge

oscillator

Construction

The circuit construction of Wien bridge oscillator can be explained as below. It is a two-stage amplifier with RC bridge circuit. The bridge circuit has the arms R_1C_1 , R_3 , R_2C_2 and the tungsten lamp L_p . Resistance R_3 and the lamp L_p are used to stabilize the amplitude of the output.

The following circuit diagram shows the arrangement of a Wien bridge oscillator.



The transistor T_1 serves as an oscillator and an amplifier while the other transistor T_2 serves as an inverter. The inverter operation provides a phase shift of 180° . This circuit provides positive feedback through R_1C_1 , C_2R_2 to the transistor T_1 and negative feedback through the voltage divider to the input of transistor T_2 .

The frequency of oscillations is determined by the series element R_1C_1 and parallel element R_2C_2 of the bridge.

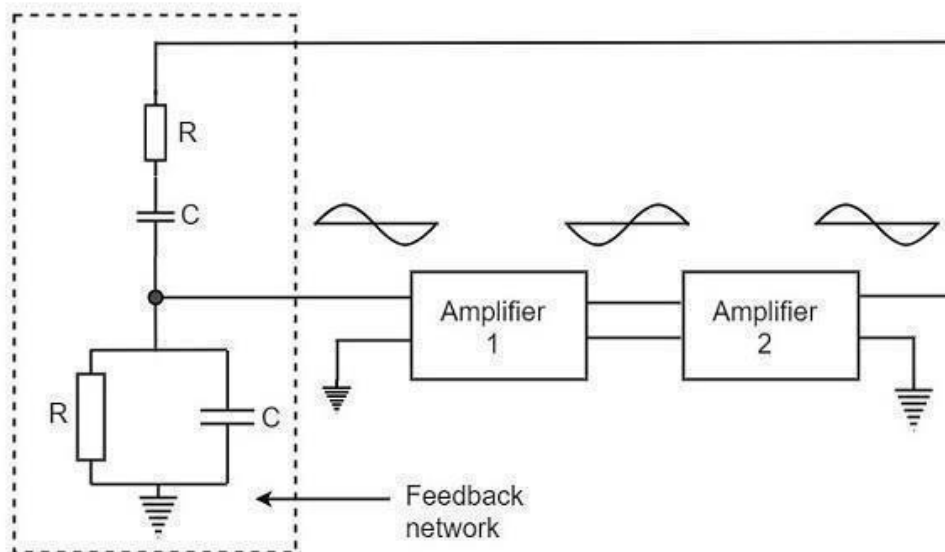
$$f = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

If $R_1=R_2$ and $C_1=C_2=C$

Then,

$$f = \frac{1}{2\pi RC}$$

Now, we can simplify the above circuit as follows–



The oscillator consists of two stages of RC coupled amplifier and a feedback network. The voltage across the parallel combination of R and C is fed to the input of amplifier 1. The net phase shift through the two amplifiers is zero.

The usual idea of connecting the output of amplifier 2 to amplifier 1 to provide signal regeneration for oscillator is not applicable here as the amplifier 1 will amplify signals over a wide range of frequencies and hence direct coupling would result in poor frequency stability. By adding Wien bridge feedback network, the oscillator becomes sensitive to a particular frequency and hence frequency stability is achieved.

Operation

When the circuit is switched ON, the bridge circuit produces oscillations of the frequency stated above. The two transistors produce a total phase shift of 360° so that proper positive feedback is ensured. The negative feedback in the circuit ensures constant output. This is achieved by temperature sensitive tungsten lamp L_p . Its resistance increases with current.

If the amplitude of the output increases, more current is produced and more negative feedback is achieved. Due to this, the output would return to the original value. Whereas, if the output tends to decrease, reverse action would take place.

Advantages

The advantages of Wien bridge oscillator are as follows–

- The circuit provides good frequency stability.

- It provides constant output.
- The operation of circuit is quite easy.
- The overall gain is high because of two transistors.
- The frequency of oscillations can be changed easily.
- The amplitude stability of the output voltage can be maintained more accurately, by replacing R_2 with a thermistor.

Disadvantages

The disadvantages of Wien bridge oscillator are as follows–

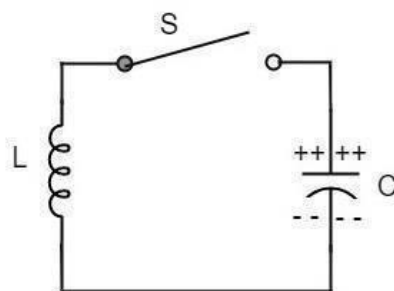
- The circuit cannot generate very high frequencies.
- Two transistors and number of components are required for the circuit construction.

LC Oscillators

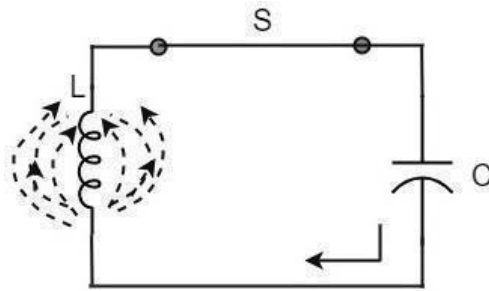
An oscillatory circuit produces electrical oscillations of a desired frequency. They are also known as **tank circuits**.

A simple tank circuit comprises of an inductor L and a capacitor C both of which together determine the oscillatory frequency of the circuit.

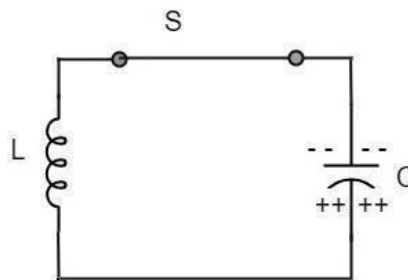
To understand the concept of oscillatory circuit, let us consider the following circuit. The capacitor in this circuit is already charged using a dc source. In this situation, the upper plate of the capacitor has excess of electrons whereas the lower plate has deficit of electrons. The capacitor holds some electrostatic energy and there is a voltage across the capacitor.



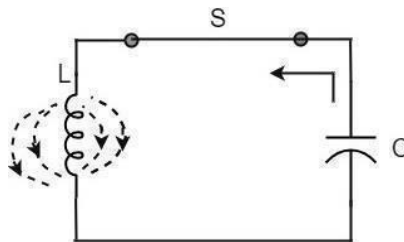
When the switch S is closed, the capacitor discharges and the current flows through the inductor. Due to the inductive effect, the current builds up slowly towards a maximum value. Once the capacitor discharges completely, the magnetic field around the coil is maximum.



Now, let us move on to the next stage. Once the capacitor is discharged completely, the magnetic field begins to collapse and produces a counter EMF according to Lenz's law. The capacitor is now charged with positive charge on the upper plate and negative charge on the lower plate.



Once the capacitor is fully charged, it starts to discharge to build up a magnetic field around the coil, as shown in the following circuit diagram.



This continuation of charging and discharging results in alternating motion of electrons or an **oscillatory current**. The interchange of energy between L and C produce continuous **oscillations**.

In an ideal circuit, where there are no losses, the oscillations would continue indefinitely. In a practical tank circuit, there occur losses such as **resistive** and **radiation losses** in the coil and **dielectric losses** in the capacitor. These losses result in damped oscillations.

Frequency of Oscillations

The frequency of the oscillations produced by the tank circuit are determined by the components of the tank circuit, **the L** and **the C**. The actual frequency of oscillations is the **resonant frequency** (or natural frequency) of the tank circuit which is given by

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Capacitance of the capacitor

The frequency of oscillation f_o is inversely proportional to the square root of the capacitance of a capacitor. So, if the value of the capacitor used is large, the charge and discharge time periods will be large. Hence the frequency will be lower.

Mathematically, the frequency,

$$f_o \propto \frac{1}{\sqrt{C}}$$

Self-Inductance of the coil

The frequency of the oscillation f_o is proportional to the square root of the self-inductance of the coil. If the value of the inductance is large, the opposition to change of current flow is greater and hence the time required to complete each cycle will be longer, which means time period will be longer and frequency will be lower.

Mathematically, the frequency,

$$f_o \propto \frac{1}{\sqrt{L}}$$

Combining both the above equations,

$$f_o \propto \frac{1}{\sqrt{LC}}$$

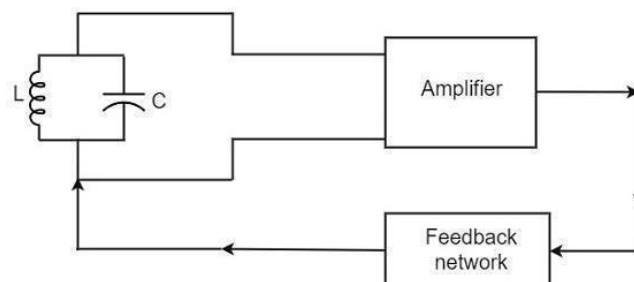
$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

The above equation, though indicates the output frequency, matches the **natural frequency** or **resonance frequency** of the tank circuit.

An Oscillator circuit is a complete set of all the parts of circuit which helps to produce the oscillations. These oscillations should sustain and should be undamped as just discussed before. Let us try to analyze a practical Oscillator circuit to have a better understanding on how an Oscillator circuit works.

Practical Oscillator Circuit

A Practical Oscillator circuit consists of a tank circuit, a transistor amplifier, and a feedback circuit. The following circuit diagram shows the arrangement of a practical oscillator.



Let us now discuss the parts of this practical oscillator circuit.

Tank Circuit – The tank circuit consists of an inductance L connected in parallel with capacitor C . The values of these two components determine the frequency of the oscillator circuit and hence this is called as **Frequency determining circuit**.

- **Transistor Amplifier** – The output of the tank circuit is connected to the amplifier circuit so that the oscillations produced by the tank circuit are amplified here. Hence the output of these oscillations are increased by the amplifier.
- **Feedback Circuit** – The function of feedback circuit is to transfer a part of the output energy to LC circuit in proper phase. This feedback is positive in oscillators while negative in amplifiers.

Frequency Stability of an Oscillator

The frequency stability of an oscillator is a measure of its ability to maintain a constant frequency, over a long time interval. When operated over a longer period of time, the oscillator frequency may have a drift from the previously set value either by increasing or by decreasing.

The change in oscillator frequency may arise due to the following factors –

- Operating point of the active devices such as BJT or FET used should lie in the linear region of the amplifier. Its deviation will affect the oscillator frequency.
- The temperature dependency of the performance of circuit components affects the oscillator frequency.
- The changes in d.c. supply voltage applied to the active device, shift the oscillator frequency. This can be avoided if a regulated power supply is used.
- A change in output load may cause a change in the Q -factor of the tank circuit, thereby causing a change in oscillator output frequency.
- The presence of interelement capacitances and stray capacitances affects the oscillator output frequency and thus frequency stability.

Tuned circuit oscillators are the circuits that produce oscillations with the help of tuning circuits. The tuning circuit consists of an inductance L and a capacitor C . These are also known as **LC oscillators, resonant circuit oscillators or tank circuit oscillators**.

The tuned circuit oscillators are used to produce an output with frequencies ranging from 1 MHz to 500 MHz. Hence these are also known as **R.F. Oscillators**. A BJT or a FET is used as an amplifier with tuned circuit oscillators. With an amplifier and an LC tank circuit, we can feedback a signal with right amplitude and phase to maintain oscillations.

Types of Tuned Circuit Oscillators

Most of the oscillators used in radio transmitters and receivers are of LC oscillators type. Depending upon the way the feedback is used in the circuit, the LC oscillators are divided as the following types.

- **Hartley Oscillator**—It uses inductive feedback.
- **Colpitts Oscillator**—It uses capacitive feedback.
- **Clapp Oscillator**—It uses capacitive feedback.

Hartley Oscillator

A very popular **local oscillator** circuit that is mostly used in **radio receivers** is the **Hartley Oscillator** circuit. The constructional details and operation of a Hartley oscillator are discussed below.

Construction

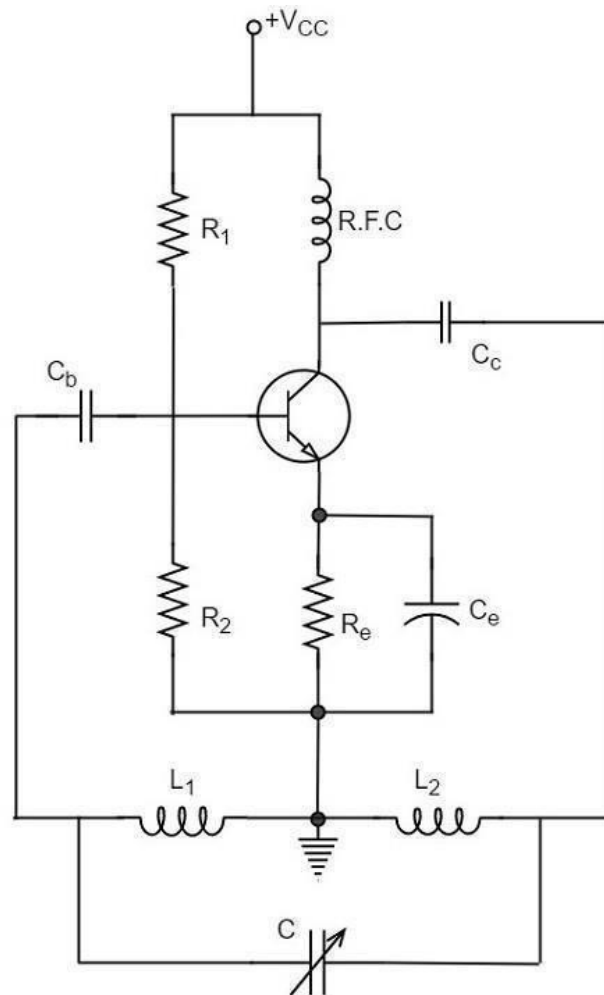
In the circuit diagram of a Hartley oscillator shown below, the resistors R_1 , R_2 and R_e provide necessary bias condition for the circuit. The capacitor C_e provides a.c. ground thereby providing any signal degeneration. This also provides temperature stabilization.

The capacitors C_c and C_b are employed to block d.c. and to provide an a.c. path. The radio frequency choke (R.F.C) offers very high impedance to high frequency currents which means it shorts for d.c. and opens for a.c. Hence it provides d.c. load for collector and keeps a.c. currents out of d.c. supply source.

Tank Circuit

The frequency determining network is a parallel resonant circuit which consists of the inductors L_1 and L_2 along with a variable capacitor C . The junction of L_1 and L_2 are earthed. The coil L_1 has its one end connected to base via C_c and the other to emitter via C_e . So, L_2 is in the output circuit. Both the coils L_1 and L_2 are inductively coupled and together form an **Auto-transformer**.

The following circuit diagram shows the arrangement of a Hartley oscillator. The tank circuit is **shunt fed** in this circuit. It can also be a **series-fed**.



Operation

When the collector supply is given, a transient current is produced in the oscillatory or tank circuit. The oscillatory current in the tank circuit produces a.c. voltage across L_1 .

The **auto-transformer** made by the inductive coupling of L_1 and L_2 helps in determining the frequency and establishes the feedback. As the CE configured transistor provides 180° phase shift, another 180° phase shift is provided by the transformer, which makes 360° phase shift between the input and output voltages.

This makes the feedback positive which is essential for the condition of oscillations. When the **loop gain $|\beta A|$ of the amplifier is greater than one**, oscillations are sustained in the circuit.

Frequency

The equation for frequency of Hartley oscillator is given as

$$f = \frac{1}{2\pi\sqrt{L_T C}}$$

$$L_T = L_1 + L_2 + 2M$$

Here, L_T is the total cumulatively coupled inductance; L_1 and L_2 represent inductances of 1st and 2nd coils; and M represents mutual inductance.

Mutual inductance is calculated when two windings are considered.

Advantages

The advantages of Hartley oscillator are

- Instead of using a large transformer, a single coil can be used as an auto-transformer.
- Frequency can be varied by employing either a variable capacitor or a variable inductor.
- Less number of components are sufficient.
- The amplitude of the output remains constant over a fixed frequency range.

Disadvantages

The disadvantages of Hartley oscillator are

- It cannot be a low frequency oscillator.
- Harmonic distortions are present.

Applications

The applications of Hartley oscillator are

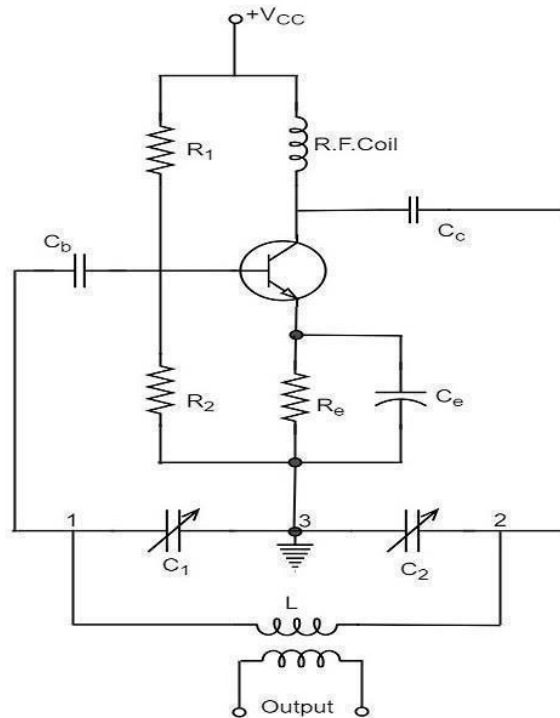
- It is used to produce a sine wave of desired frequency.
- Mostly used as a local oscillator in radio receivers.
- It is also used as R.F. Oscillator.

Colpitts oscillator

A Colpitts oscillator looks just like the Hartley oscillator but the inductors and capacitors are replaced with each other in the tank circuit. The constructional details and operation of a Colpitts oscillator are as discussed below.

Construction

Let us first take a look at the circuit diagram of a Colpitts oscillator.



The resistors R_1 , R_2 and R_e provide necessary bias condition for the circuit. The capacitor C_e provides a.c. ground thereby providing any signal degeneration. This also provides temperature stabilization.

The capacitors C_c and C_b are employed to block d.c. and to provide an a.c. path. The radio frequency choke (R.F.C) offers very high impedance to high frequency currents which means it shorts for d.c. and opens for a.c. Hence it provides d.c. load for collector and keeps a.c. currents out of d.c. supply source.

Tank Circuit

The frequency determining network is a parallel resonant circuit which consists of variable capacitors C_1 and C_2 along with an inductor L . The junction of C_1 and C_2 are earthed. The capacitor C_1 has its one end connected to base via C_c and the other to emitter via C_e . The voltage developed across C_1 provides the regenerative feedback required for the sustained oscillations.

Operation

When the collector supply is given, a transient current is produced in the oscillatory or tank circuit. The oscillatory current in the tank circuit produces a.c. voltage across C_1 which are

applied to the base-emitter junction and appear in the amplified form in the collector circuit and supply losses to the tank circuit.

If terminal 1 is at positive potential with respect to terminal 3 at any instant, then terminal 2 will be at negative potential with respect to 3 at that instant because terminal 3 is grounded. Therefore, points 1 and 2 are out of phase by 180° .

As the CE configured transistor provides 180° phase shift, it makes 360° phase shift between the input and output voltages. Hence, feedback is properly phased to produce continuous undamped oscillations. When the **loop gain $|\beta A|$ of the amplifier is greater than one, oscillations are sustained** in the circuit.

Frequency

The equation for frequency of Colpitts oscillator is given as

$$f = \frac{1}{2\pi\sqrt{LC_T}}$$

C_T is the total capacitance of C_1 and C_2 connected in series.

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$C_T = \frac{C_1 \times C_2}{C_1 + C_2}$$

Advantages

The advantages of Colpitts oscillator are as follows—

- Colpitts oscillator can generate sinusoidal signals of very high frequencies.
- It can withstand high and low temperatures.
- The frequency stability is high.
- Frequency can be varied by using both the variable capacitors.
- Less number of components are sufficient.
- The amplitude of the output remains constant over a fixed frequency range.

The Colpitts oscillator is designed to eliminate the disadvantages of Hartley oscillator and is known to have no specific disadvantages. Hence there are many applications of a Colpitts oscillator.

The operation of Clapp oscillator circuit is in the same way as that of Colpitts oscillator. The frequency of oscillator is given by the relation,

$$f_o = \frac{1}{2\pi\sqrt{L \cdot C}}$$

Where, $\frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}$

Usually, the value of C_3 is much smaller than C_1 and C_2 . As a result of this, C is approximately equal to C_3 . Therefore, the frequency of oscillation,

$$f_o = \frac{1}{2\pi\sqrt{L \cdot C_3}}$$

It is understood that the Clapp oscillator is similar to the Colpitts oscillator, however they differ in the way the inductances and capacitances are arranged. The frequency stability though is good, can be variable in a Clapp oscillator.

A Clapp oscillator is sometimes preferred over a Colpitts oscillator for constructing a variable frequency oscillator. The Clapp oscillators are used in receiver tuning circuits as a frequency oscillator.

One of the important features of an oscillator is that the feedback energy applied should be in correct phase to the tank circuit. The oscillator circuits discussed so far have employed inductor (L) and capacitor (C) combination in the tank circuit or frequency determining circuit.

We have observed that the LC combination in oscillators provides 180° phase shift and transistor in CE configuration provides 180° phase shift to make a total of 360° phase shift so that it would make a zero difference in phase.

Drawbacks of LC circuits

Though they have few applications, the LC circuits have few drawbacks such as

- Frequency instability
- Waveform is poor
- Cannot be used for low frequencies
- Inductors are bulky and expensive

Whenever an oscillator is under continuous operation, its **frequency stability** gets affected. There occur changes in its frequency. The main factors that affect the frequency of an oscillator are

- Powersupplyvariations
- Changesintemperature
- Changesinloadoroutputresistance

In RC and LC oscillators the values of resistance, capacitance and inductance vary with temperature and hence the frequency gets affected. In order to avoid this problem, the piezo electric crystals are being used in oscillators.