ANALOG CIRCUITS

LECTURE NOTES

B.TECH
(II YEAR – II SEM)
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(Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – ‘A’ Grade - ISO 9001:2015 Certified)
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MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

II Year B.Tech. ECE-II Sem  L  T/P/D  C
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(R18A0405) ANALOG CIRCUITS

OBJECTIVE
The main objectives of the course are:
1. Study about Wave shaping concepts of both linear and non-linear circuits.
2. Study about the designing of multivibrators.
3. Study about Time Base Generator, understanding sampling gates and Logic Gates.
4. Analysis of basic transistor amplifier circuits and their frequency response

UNIT – I BJT Amplifiers- Frequency Response: Frequency response of an amplifier, Analysis at low and High Frequencies, Hybrid-pi (π) common emitter transistor model, validity of hybrid- π model, variation of hybrid – π parameters, Millers theorem and its dual, the CE short circuit current gain, current gain with resistive load, gain-bandwidth product.

MULTISTAGE AMPLIFIERS: Distortion in amplifiers, Analysis of cascaded BJT amplifier, Darlington pair, Coupling schemes-RC coupled amplifier, transformer coupled amplifier, Direct coupled Amplifier.

UNIT - II FEEDBACK AMPLIFIERS: Concept of Feedback and types, Effects of negative feedback on amplifiers characteristics, voltage series, current series, current shunt, and voltage shunt feedback amplifiers.

OSCILLATORS: Classification of oscillators, Barkhausen criterion, RC phase shift oscillator, Wein-bridge oscillator, LC oscillators- Hartley and Colpitts oscillator.

UNIT - III LARGE SIGNAL AMPLIFIERS: Classification, Distortion in amplifiers, class A large signal amplifiers, efficiency of class A amplifier, class B power amplifier, efficiency of class B amplifier, class B push pull amplifier, Complementary symmetry class B push pull amplifiers, class AB push pull amplifier, Single tuned amplifier, Principles of Staggered tuning.


UNIT –V TIME BASE GENERATORS: General features of a Time Base Signal, Methods of Generating Time Base Wave forms, Basic Principles of Transistor Miller and Bootstrap Time Base Generator, Current Time Base Generator.

TEXT BOOKS:
REFERENCE BOOKS:


COURSE OUTCOMES:

At the end of the course, the student will be able to;

1. Understand the concepts of wave shaping circuits
2. Design of multivibrators for various applications,
3. Understand the concepts of Time Base Generators, sampling gates and logic gates
4. Analyzed the different types of amplifiers and oscillators
UNIT-I
BJT Amplifiers- Frequency Response

FREQUENCY RESPONSE OF AMPLIFIERS

For any electronic circuit, the behavior of amplifiers is affected by the frequency of the signal on their input terminal. This characteristic is known as the frequency response.

Frequency response is one of the most important properties of amplifiers. In the frequency range that amplifiers have been designed for, they must deliver a constant and acceptable level of gain. The frequency response depends directly on the components and the architecture chosen for the design of the amplifier.

Before defining in detail the frequency response, we need to present the unit of decibel (dB) and the logarithmic scale related to it. When studying the frequency response, it is indeed more suitable to convert either the power or voltage gain into dB and to represent the frequency scale in a logarithmic (log) scale.

If we consider an amplifier with power gain $A_P$ and voltage gain $A_V$, the power and voltage gain in dB are defined by:

$$A_P(dB) = 10 \log(A_P)$$
$$A_V(dB) = 20 \log(A_V)$$

While the gains in linear scale are always positive ($A_P, A_V \geq 0$), their equivalent in dB can either be positive if an amplification is being realized ($A_P, A_V > 1$) or negative if the input signal is attenuated ($A_P, A_V < 1$).

Often, it is not the gain $A_V(dB)$ that is investigated but rather a normalized ratio $A_V/A_{V,mid}(dB)=20\log(A_V/A_{V,mid})$. Where $A_{V,mid}$ is called the midrange gain and represents the maximum gain of the amplifier in its frequency working range, for example 20 Hz – 20 kHz for an audio amplifier.

Therefore, when $A_V=A_{V,mid}$, the normalized gain (written indifferently $A_V$) is $A_V(dB)=0$. This sets a 0 dB reference when the gain is maximum. It is important to note that when the power is divided by two, we observe that $A_P(dB)=10\log(0.5)=-3$ dB.

The frequency at which the power drops to 50% of its midrange value is known as the cutoff frequency and noted $f_c$. Each time that the power is halved, a reduction of 3 dB of the normalized gain is observed. Therefore $A_P=-3$ dB corresponds to $A_{V,mid}/2$, $A_P=-6$ dB corresponds to $A_{V,mid}/4$ and so on ...

For this same frequency, the voltage (or current) is multiplied by a factor $\sqrt{2}=0.7$. Halving the voltage signal corresponds to a reduction of 6 dB and follows the same pattern as presented for the power gain.
The most common tool used to represent the frequency response of any system is the **Bode plot**. It consists of the normalized gain $A_V$(dB) as a function of the frequency in log scale. A simplified Bode graph of an amplifier is shown in the **Figure 1** below:

Fig 1 : Typical Bode graph of an amplifier

The light blue curve is called the asymptotic representation while the dark blue curve is the real frequency response of the circuit. In **Figure 1**, two different cutoff frequencies can be distinguished: $f_c$ for “low cutoff” and $f_h$ for “high cutoff”. The quantity $f_h-f_c$ is called the **bandwidth** and represents the frequency range where the gain is above the -3 dB.

**EFFECT OF THE CAPACITORS:**

Let us consider a Common Emitter Amplifier (CEA) which configuration is shown in **Figure 2**. The structure around the BJT transistor consists of a voltage divider network ($R_1$ and $R_2$), a load ($R_l$), coupling capacitors ($C_1$ and $C_3$) and a bypass capacitor $C_2$.

As capacitors have a property called **reactance** that is an equivalent of the resistance. The reactance ($X_C$) of capacitors depends on the frequency and the value of the capacitor, as in the below equation

$$X_C = \frac{1}{2\pi f C}$$
When the frequency is low, $X_C$ tends to be high. Near DC signals, capacitors behave therefore as open circuits. On the other hand, when the frequency increases $X_C$ tends to zero and capacitors act as short circuits.

At low input frequencies, the coupling capacitors will more likely block the signal, since $X_{C1}$ and $X_{C3}$ are higher, more voltage drop will be observed across $C_1$ and $C_3$. This results in a lower voltage gain.

At high input frequencies the bypass capacitor $C_2$ shortens the emitter branch to the ground and the voltage gain of the amplifier is $A_V = \frac{R_C / R_l}{r_e}$ with $r_e$ being the small diode emitter resistance. When the frequencies are lower, the resistance between the emitter and the ground is no longer only $r_e$ but $R_E + r_e$ and therefore the voltage gain decreases to $A_V = \frac{R_C / R_l}{(R_E + r_e)}$.

There is another type of capacitors that affect the frequency response of the amplifier and is not represented in Figure 2. They are known as internal transistor capacitors and represented in Figure 3 below:
Whereas the coupling and bypass capacitors act as **high-pass filter** (they block low frequencies), these internal capacitors behave differently. Indeed, if the frequency is low, \( C_{BC} \) and \( C_{BE} \) act as an open circuit and the transistor is not affected at all. However, if the frequency increases, more signal passes through them instead of going in the base branch of the transistor, therefore decreasing the voltage gain. The cutoff frequency of a RC filter:

\[
 f_c = \frac{1}{2\pi RC} 
\]

**ANALYSIS AT LOW FREQUENCY**

First of all we consider the input high-pass filter \( R_{in}C_1 \). Where \( R_{in} \) is the total input impedance of the amplifier which can be expressed as:

\[
 R_{in} = R_S + (R_1 \parallel R_2 \parallel \beta R_e) 
\]

The low cutoff frequency of the input will therefore be:

\[
 f_{cl,in} = \frac{1}{2\pi R_{in}C_1} 
\]

The same procedure can be done for the output where the output resistance is

\[
 R_{out} = R_C \parallel R_L 
\]

The low cutoff frequency of the output filter is:

\[
 f_{cl,out} = \frac{1}{2\pi R_{out}C_3} 
\]

Finally, for the bypass capacitor, the resistance formula is more complex and given by

\[
 R_{bypass} = R_e \parallel \left( R_e + \frac{(R_S \parallel \beta R_e)}{\beta} \right) 
\]

The low cutoff frequency of the bypass structure is thus:

\[
 f_{cl,bypass} = \frac{1}{2\pi R_{bypass}C_2} 
\]

One last thing we need to understand before plotting the Bode graph is about the slope out of the midrange values. The decrease of \( A_{V,mid} \) with the frequency is called **roll-off** and its value for each simple RC filter is -20 dB/decade (dB/dec). This value means for high-pass filters (resp. low-pass filters) that each time the frequency is divided by 10 (resp. multiplied by 10), a decrease of -20 dB is observed for the gain of the amplifier.

When multiple filters are blocking the same range of frequencies, the roll-off is enhanced. In our example three filters are simultaneously blocking the frequencies below 35 Hz, the roll-off is therefore 3*(-20 dB/dec)=-60 dB/dec.
As stated previously, it is the internal transistor capacitors that will limit the gain at high frequencies acting as low-pass filters. It can be shown that the equivalent circuit of Figure 2 at high frequency can be drawn such as presented in Figure 5:

We can note that the coupling capacitors are not represented since they behave as short circuits at high frequencies. Moreover, the emitter branch is shorten to the ground for the same reason applying to the bypass capacitor.

The internal capacitor $C_{BC}$ is converted via Miller’s theorem into the equivalent $C_{in}$ and $C_{out}$ capacitors. Moreover, this theorem states that
\[C_{in} = C_{BC}(A_{V,mid} + 1)\] and
\[C_{out} = C_{BC}(A_{V,mid} + 1)/A_{V,mid}.

The total input capacitance of this circuit is
\[C_{in} = C_{BE} + C_{in};\]

The total input resistance is
\[R_{IN} = R_S//R_1//R_2//\beta_r.

The numerical application to our example gives
\[A_{V,mid} = (R_C//R_t)/r_e = 108, C_{IN} = 575 \text{ pF} \text{ and } R_{IN} = 409 \Omega.\]

The high cutoff frequency of the input is therefore
\[f_{hc,in} = 1/(2\pi R_{IN} C_{IN}) = 677 \text{ kHz}.\]

From the output point of view, the high cutoff frequency is simply given by the filter
\[(R_C//R_t)C_{out} \text{ with } C_{out} = 5.3 \text{ pF} ; f_{hc,out} = 1/(2\pi (R_C//R_t) C_{out}) = 1.1 \text{ MHz}.\]

The information given here is summarized in a Bode plot representing the high frequency response of the CEA in asymptotic representation:

Fig 6: High frequency response of the CEA

By merging the two Bode graphs obtained for the low and high frequency responses in Figure 4 and 6, we can now plot the overall frequency response of the CEA configuration:

Fig 7: Total frequency response of the CEA
Hybrid-pi (π) common emitter transistor model

For amplifier circuits Common Emitter configuration is preferred Because for Common Collector (hrc < 1). For Common Collector Configuration, voltage gain $A_v < 1$. So even by cascading you can't increase voltage gain. For Common Base, current gain $h_{ib} < 1$. So overall voltage gain is < 1. But for Common Emitter, $h_{re} > 1$. Therefore Voltage gain can be increased by cascading Common Emitter stage. So Common Emitter configuration is widely used.

Under reverse bias condition the capacitance at the junction is called transition or space charge capacitance. Under forward bias condition the capacitance is called diffusion or storage capacitance. At high frequencies, BJT cannot be analysed by h-parameters.

Giacolletto model - hybrid π equivalent circuit

Desirable features of hybrid π equivalent circuit are:
1. The value of components in the equivalent circuit are independent of frequencies.
2. The values of all the resistive components in the equivalent circuit can be determined from the known or specified values of h-parameters at low frequencies.
3. The results obtained by using this equivalent circuit agrees with the experimental result.

The components of the equivalent circuit exist in the form of π hence the name.

For small signal behaviour the transistor at its input port behaves as a resistor.

The output port is a dependent current source.
Because the base (B) is lightly doped all the depletion region lies entirely in the Base region. So, when the collector voltage is increased the depletion region in the base increases.

\[
r_{bc} \rightarrow \text{This resistance is added to compensate for the change in IC due to change in VCE.}
\]

The *Hybrid-\( \pi \) or Giacoletto Model* for the Common Emitter amplifier circuit (single stage) is as shown:

\[
r_{bc}' = \frac{1}{g_{bc}}
\]

**Fig 8 : Hybrid-\( \pi \) CE BJT Model**
Analysis of this circuit gives satisfactory results at all frequencies not only at high frequencies but also at low frequencies. All the parameters are assumed to be independent of frequency.

Circuit Components

B' is the internal node of the base of the Transconductance amplifier. It is not physically accessible.
The base spreading resistance $r_{b'b}$ is represented as a lumped parameter between base B and internal node B'. $(g_m, V_{b'e})$ is a current generator. Vb'e is the input voltage across the emitter junction. If $V_{b'e}$ increases, more carriers are injected into the base of the transistor. So the increase in the number of carriers is $\alpha V_{b'e}$. This results in small signal current (since we are taking into account changes in $V_{b'e}$). This effect is represented by the current generator $g_m V_{b'e}$. This represents the current that results because of changes in $V_{b'e}$ when C is shorted to E.

When the number of carriers injected into the base increase, base recombination also increases. So this effect is taken care of by $g_{b'e}$. As recombination increases, base current increases. Minority carrier storage in the base is represented by $c_e$ the diffusion capacitance.

According to Early Effect, the change in voltage between Collector and Emitter changes the base width. So base width will be modulated according to the voltage between Collector and Emitter. When base width changes, the minority carrier concentration in base changes. Hence the current which is proportional to carrier concentration also changes. So $I_E$ changes and hence $I_C$ changes. This feedback effect [$I_E$ on input side, $I_C$ on output side] is taken into account by connecting $g_{b'c}$ between B', and C. The conductance between Collector and Base is $g_{ce}$. $C_c$ represents the collector junction barrier capacitance.

The High frequency model parameters of a BJT in terms of low frequency hybrid parameters is given below
- Tran conductance $g_m = I_C/V_T$
- Internal Base node to emitter resistance $r_{b'e} = h_{fe}/g_m = (h_{fe} V_T)/I_C$
- Internal Base node to collector resistance $r_{b'c} = (h_{re} r_{b'e}) / (1-h_{re})$ assuming $h_{re} << 1$ it reduces to $r_{b'c} = (h_{re} r_{b'e})$
- Base spreading resistance $r_{bb'} = h_{ie} - r_{b'e} = h_{ie} - (h_{fe} V_T)/I_C$
- Collector to emitter resistance $r_{ce} = 1 / (h_{oe} - (1+h_{fe})/r_{b'c})$

Variation of Hybrid Parameters with $|I_C|$, $|V_{CE}|$ and T

1) Transconductance Amplifier or Mutual Conductance ($g_m$):

$$g_m = I_C/V_T$$

$g_m$ is independent of $V_{CE}$

$$V_T = T/11,600$$

Therefore $g_m \propto 1/T$

$g_m$ is independent of $V_{CE}$

Since in the active region of the transconductance, $I_C$ is independent of $V_{CE}$
2) **Base Emitter Resistance** \( (r_{b'e}) \)

\[
 r_{b'e} = \frac{h_{fe}}{g_m} = (h_{fe}V_T)/I_C
\]

Therefore 
\[
 r_{b'e} \propto \frac{1}{I_C}
\]

\( r_{b'e} \) increases as \( T \) increases since \( r_{b'e} \propto V_T \).

3) **Base Spread Resistance** \( (r_{bb'}) \)

\( r_{bb'} \) decreases with increase in \( I_C \)

Since as \( I_C \) increases, conductivity increases. So \( r_{bb'} \) decreases, because of conductivity modulation. But \( r_{bb'} \) increases with increase in Temperature. Because as \( T \) increases, mobility of the carriers decreases. So conductivity decreases. So \( r_{bb'} \) increases.

**Miller’s Theorem**

Fig. 9(a) shows an amplifier with a capacitor between input and output terminals. It is called as feedback capacitor. When the gain \( K \) is large, the feedback will change the input \( Z \) and output \( Z \) of the circuit.

![Fig. 9 (a) Feedback Capacitor](image)

A circuit as shown above is difficult to analyze, because of capacitor. So according to the Miller’s theorem, the feedback capacitor can be split into two values, one as connected in the input side and the other on the output side, as shown in Fig. 9 (b).

![Fig. 9 (b) Splitting of feedback capacitor using Miller’s Theorem](image)

**Mathematical Proof of Miller’s Theorem:**

The AC current passing through capacitor \( (C) \) in Fig. 9 (a) is

\[
 I_C = \frac{V_{in}-V_{out}}{(\frac{1}{j\omega C})} = \frac{(V_{in}-V_{out})}{-jX_C}
\]
\[ V_{\text{out}} = K V_{\text{in}} \]

Therefore
\[ I_C = \frac{(V_{\text{in}} - K V_{\text{in}})}{-jX_C} = \frac{V_{\text{in}}(1-K)}{-jX_C} \]

\[ V_{\text{in}} \frac{V_{\text{in}}}{I_C} = Z_{\text{in}} = \frac{V_{\text{in}}}{-jX_C} = -jX_C \frac{1}{(1-K)} \]

\[ = -j \frac{1}{2\pi f C(1-K)} \quad \text{since } X_C = \frac{1}{2\pi f C} \]

\[ \frac{V_{\text{in}}}{I_C} \text{ is the input } Z \text{ as seen from the input terminals.} \]

Therefore
\[ Z_{\text{in}} = -j \frac{1}{2\pi f C(1-K)} \]

Therefore
\[ C_{\text{in}} = C (1-K) \]

Similarly output capacitance can be derived as follows:

Current in the capacitor,
\[ I_C = \frac{V_{\text{out}} - V_{\text{in}}}{-jX_C} = \frac{V_{\text{out}}}{-jX_C} \left(1 - \frac{V_{\text{in}}}{V_{\text{out}}}\right) \]

\[ I_C = \frac{V_{\text{out}}}{-jX_C} \left(1 - \frac{1}{K}\right) \]

Rearranging the terms we get,
\[ Z_{\text{out}} = \frac{-jX_C}{\left(1 - \frac{1}{K}\right)} = \frac{-jX_C}{\left(K - 1\right)} \]

\[ = -j \frac{1}{2\pi f C\left(K - 1\right)} \]

Therefore
\[ C_{\text{out}} (\text{Miller}) = C \left(\frac{K - 1}{K}\right) \]

**Miller’s Theorem**

It states that if an impedance \( Z \) is connected between the input and output terminals, of a network, between which there is voltage gain, \( K \), the same effect can be had by removing \( Z \) and connecting an impedance \( Z_i \) at the input = \( \frac{Z}{(1-K)} \) and \( Z_o \) across the output = \( \frac{ZK}{(K-1)} \).
Fig 10: High Frequency equivalent circuit with resistive load

\[ C_{b'c} = C_c \]

\( r_{b'c} \) and \( C_c \) are between the input termed \( B' \) and output termed \( C \). The voltage gain of the amplifier \( \frac{V_{ce}}{V_{b'e}} = K (>> 1) \). Therefore by Miller’s theorem, \( C_c \) and \( r_{b'c} \) can be connected between \( B' \) and \( E \) (input side) with values \( \frac{C_c}{1-K} \) and \( r_{b'c} (1-K) \) respectively. On the output side between Collector and emitter as \( C_c \left( \frac{K-1}{K} \right) \) and \( r_{b'c} \left( \frac{K}{K-1} \right) \) resting.

Therefore high frequency equivalent circuit using Miller’s theorem reduces to, (neglecting \( r_{bb} \),)

\[ K = \frac{V_{ce}}{V_{b'e}} \]

\[ V_{ce} = -I_C \cdot R_L \cdot \text{Negative is used since current direction is opposite} \]

Fig 11: Circuit after applying Millers Theorem

\[ K = -\frac{I_C \cdot R_L}{V_{b'e}} \]

But \( \frac{I_C}{V_{b'e}} = g_m \)

Therefore \( K = -g_m \cdot R_L \)
The CE Short Circuit Current gain (Ai)

This is the circuit of transistor amplifier in common emitter configuration

The approximate equivalent circuit at high frequencies, with output shorted is

$r_{b'e}$ is assumed to be very large. So it is open circuit.
$r_{ce}$ disappears since it is in shunt with short circuited output.

$I_L = -g_m V_{b'e}$

Negative sign taking the direction of current into account. $I_L$ is contributed by the current source only.

$V_{b'e} = I x Z = I X \frac{1}{Y}$

$V_{b'e} = \frac{I_L X_1}{g_{b'e} + j\omega_C e}$
Therefore

\[ I_L = \frac{-g_m l_i}{g_{b'e} + j\omega C_e} \]

Conductances in parallel get added

![Fig.14 Conductances in parallel](image)

Therefore current gain under short circuit conditions is,

\[ A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega C_e} \]

But

\[ g_{b'e} = \frac{g_m}{h_{fe}} \]

\[ C_e = \frac{g_m}{2\pi f_T} \]

Therefore by substituting all these terms in the above equation, we get

\[ A_i = \frac{I_L}{I_i} = \frac{-g_m}{\frac{g_m}{h_{fe}} + j\omega \frac{g_m}{h_{fe}} 2\pi f_T} \]

\[ = \frac{-1}{h_{fe} + j\omega \frac{1}{2\pi f_T}} = \frac{-h_{fe}}{1 + j \frac{h_{fe} \cdot f_T}{f_T}} \]

Since

\[ f_r h_{fe} = f_{\beta} \]

Therefore

\[ A_i = \frac{-h_{fe}}{1 + j \left( \frac{f}{f_{\beta}} \right)} \]
When $f = f_\beta$, $A_i$ falls by $\frac{1}{\sqrt{2}}$, or by 3db. The frequency range $f_\beta$ is called Bandwidth of the amplifiers.

$f_\beta$ : Is the frequency at which the short circuit gain in common emitter configuration falls by 3 db.
$f_T$: This is defined as the frequency at which the common emitter shunt circuit current gain becomes 1.

Let $f = f_T$, $A_i = 1$

Therefore $1 = \frac{h_fe}{\sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}}$

$1 + \left(\frac{f_T}{f_\beta}\right)^2 = h_fe^2$

$\left(\frac{f_T}{f_\beta}\right)^2 = h_fe^2 - 1 = h_fe^2$ since $h_fe >> 1$

Therefore $f_T = f_\beta \cdot h_fe$

Where $f_\beta$ - is the Bandwidth of the transistor
$h_fe$ - is the current gain
$f_T$ - is the current gain, Bandwidth product

In Common Emitter configurations, $A_i >> 1$. But as frequency increases $A_i$ decreases. $f_T$ depends on the operating point of the transistor. The graph of $f_T$ versus $I_C$ for a transistor is as shown,

![Graph](image)

Fig.15 Variation of $I_C$ with frequency

For a typical transistor, $f_T = 80$ MHz
$f_\beta = 1.6$ MHz
Current gain with resistive load

\[ f_T = f_\beta \cdot h_{fe} = \frac{g_m}{2\pi(C_e + C_c)} \]

Considering the load resistance \( R_L \),
\( V_{b'e} \) is the input voltage and is equal to \( V_1 \)
\( V_{Ce} \) is the output voltage and is equal to \( V_2 \)

\[ K_2 = \frac{V_{Ce}}{V_{b'e}} \]

The equivalent circuit is as shown below:

![Equivalent circuit taking Load resistance into account](image)

This circuit is still complicated for analysis.

Because, there are two time constants associated with the input and the other associated with the output. The output time constant will be much smaller than the input time constant. So it can be neglected.

\[ K = \text{Voltage gain. It will be } \gg 1 \]

Therefore

\[ g_{b'c} \left( \frac{K-1}{K} \right) = g_{b'c} \]

\[ g_{b'c} < g_{Ce} \quad \text{since } r_{b'c} = 4 \text{ MΩ}, \quad r_{Ce} = 80 \text{ K (typical values)} \]

So \( g_{b'c} \) can be neglected in the equivalent circuit.

In a wide band amplifier \( R_L \) will not exceed 2KΩ, since \( f_H \propto \frac{1}{R_L} \). If \( R_L \) is small, \( f_H \) is large.

\[ f_H = \frac{1}{2\pi C_S(R_C || R_L)} \]

Therefore \( g_{Ce} \) can be neglected compared with \( R_L \).

Therefore the output circuit consists of current generator \( g_m \) \( V_{b'e} \) feeding the load \( R_L \) so the Circuit simplifies as shown in Fig. 17
\[ K = \frac{V_{Ce}}{V_{b'e}} = -g_m R_L \quad ; \quad g_m = 50 \text{ mA/V}, \quad R_L = 2\text{K}\Omega \text{ (typical values)} \]

\[ K = -100 \]

So the maximum value is \( g_{b'c} \cdot (1-K) = 0.02595 \). So this can be neglected compared to \( g_{b'c} = 1\text{mA/V} \).

\( R_L \) should not exceed 2KΩ, therefore if \( R_L > 2\text{K}\Omega \), \( C_C (1 + g_m R_L) \) becomes very large and so band pass becomes very small.

\[ C_C \left( \frac{K-1}{K} \right) = C_C \]

When \( R_L = 2\text{K}\Omega \),

The output time constant is,

\[ R_L \cdot C_C = 2 \times 10^3 \times 3 \times 10^{-12} = 6 \times 10^{-9} \text{ s (typical value)} \]

Input time constant is,

\[ r_{b'e} \left[ C_e + C_C \left[ 1 + g_m R_L \right] \right] = 403 \times 10^{-6} \text{ s} \]

So the band pass of the amplifier will be determined by the time constant of the input circuit.

The 3db frequency \( f_M = \frac{1}{2\pi r_{b'e} C} = \frac{g_{b'e}}{2\pi C} \)

Where \( C = \left[ C_e + C_C \left[ 1 + g_m R_L \right] \right] \)

**Bandwidth of a multistage amplifier**

The range of frequencies which are amplified without much variation in gain is called bandwidth of amplifiers. Human ears are insensitive to the variation of power gain of about 3dB. Hence, frequency range from lower 3dB to upper 3dB is considered as bandwidth of single stage amplifier. Bandwidth of single stage amplifier.
Bandwidth (BW) = \( f_H - f_L \) ~ \( f_H \)

**Lower 3dB frequency of multistage amplifier**

The lower 3db frequency of \( n \) identical cascaded stages as \( f_L(n) \). It is the frequency for which the overall gain falls to \( \frac{1}{\sqrt{2}} \) (3 db) of its midband value.

\[
\left[ \frac{1}{\sqrt{1 + \left( \frac{f_L}{f_L(n)} \right)^2}} \right]^n = \frac{1}{\sqrt{2}}
\]

\[
\left[ \sqrt{1 + \left( \frac{f_L}{f_L(n)} \right)^2} \right]^n = \sqrt{2}
\]

Squaring on both sides we get

\[
\left[ 1 + \left( \frac{f_L}{f_L(n)} \right)^2 \right]^n = 2
\]

Taking \( n \)th root on both sides

\[
1 + \left( \frac{f_L}{f_L(n)} \right)^2 = 2^{\frac{1}{n}}
\]

\[
\left( \frac{f_L}{f_L(n)} \right)^2 = 2^{\frac{1}{n}} - 1
\]
Taking square root on both sides

\[
\frac{f_L}{f_L(n)} = \sqrt{\frac{1}{2\pi} - 1}
\]

\[
f_L(n) = \frac{f_L}{\sqrt{\frac{1}{2\pi} - 1}}
\]

**Higher 3dB frequency of multistage amplifier**

The higher 3db frequency of \(n\) identical cascaded stages as \(f_H(n)\). It is the frequency for which the overall gain falls to \(\frac{1}{\sqrt{2}}\) (3 db) of its midband value.

\[
\left[ \frac{1}{\sqrt{1 + \left( \frac{f_H(n)}{f_H} \right)^2}} \right]^n = \frac{1}{\sqrt{2}}
\]

\[
\left[ \sqrt{1 + \left( \frac{f_H(n)}{f_H} \right)^2} \right]^n = \sqrt{2}
\]

Squaring on both sides we get

\[
\left[ 1 + \left( \frac{f_H(n)}{f_H} \right)^2 \right]^n = 2
\]

Taking \(n\)th root on both sides

\[
1 + \left( \frac{f_H(n)}{f_H} \right)^2 = 2^{\frac{1}{n}}
\]

\[
\left( \frac{f_H(n)}{f_H} \right)^2 = 2^{\frac{1}{n}} - 1
\]

Taking square root on both sides

\[
\left( \frac{f_H(n)}{f_H} \right) = \sqrt{2^{\frac{1}{n}} - 1}
\]

\[
f_H(n) = f_H \sqrt{2^{\frac{1}{n}} - 1}
\]
Multi-stage amplifiers

In practical applications, the output of a single state amplifier is usually insufficient, though it is a voltage or power amplifier. Hence they are replaced by Multi-stage transistor amplifiers.

In Multi-stage amplifiers, the output of first stage is coupled to the input of next stage using a coupling device. These coupling devices can usually be a capacitor or a transformer. This process of joining two amplifier stages using a coupling device can be called as **Cascading**.

The following figure shows a two-stage amplifier connected in cascade.

The overall gain is the product of voltage gain of individual stages.

\[
A_V = A_{V1} \times A_{V2} = \frac{V_2}{V_1} \times \frac{V_o}{V_2} = \frac{V_o}{V_1}
\]

Where \(A_V\) = Overall gain,
\(A_{V1}\) = Voltage gain of 1\(^{st}\) stage, and \(A_{V2}\) = Voltage gain of 2\(^{nd}\) stage.

If there is \(n\) number of stages, the product of voltage gains of those \(n\) stages will be the overall gain of that multistage amplifier circuit.

**Purpose of coupling device**

The basic purposes of a coupling device are

- To transfer the AC from the output of one stage to the input of next stage.
- To block the DC to pass from the output of one stage to the input of next stage, which means to isolate the DC conditions.

**Types of Coupling**

Joining one amplifier stage with the other in cascade, using coupling devices form a Multi-stage amplifier circuit. There are **four** basic methods of coupling, using these coupling devices such as resistors, capacitors, transformers etc. Let us have an idea about them.

**Resistance-Capacitance Coupling**

This is the mostly used method of coupling, formed using simple **resistor-capacitor** combination. The capacitor which allows AC and blocks DC is the main coupling element used here.
The coupling capacitor passes the AC from the output of one stage to the input of its next stage. While blocking the DC components from DC bias voltages to effect the next stage. Let us get into the details of this method of coupling in the coming chapters.

**Impedance Coupling**

The coupling network that uses inductance and capacitance as coupling elements can be called as Impedance coupling network. In this impedance coupling method, the impedance of coupling coil depends on its inductance and signal frequency which is \( jwL \). This method is not so popular and is seldom employed.

**Transformer Coupling**

The coupling method that uses a transformer as the coupling device can be called as Transformer coupling. There is no capacitor used in this method of coupling because the transformer itself conveys the AC component directly to the base of second stage.

The secondary winding of the transformer provides a base return path and hence there is no need of base resistance. This coupling is popular for its efficiency and its impedance matching and hence it is mostly used.

**Direct Coupling**

If the previous amplifier stage is connected to the next amplifier stage directly, it is called as direct coupling. The individual amplifier stage bias conditions are so designed that the stages can be directly connected without DC isolation.

The direct coupling method is mostly used when the load is connected in series, with the output terminal of the active circuit element. For example, head-phones, loud speakers etc.

**Role of Capacitors in Amplifiers**

Other than the coupling purpose, there are other purposes for which few capacitors are especially employed in amplifiers. To understand this, let us know about the role of capacitors in Amplifiers.

**The Input Capacitor Cin**

The input capacitor \( C_{in} \) present at the initial stage of the amplifier, couples AC signal to the base of the transistor. This capacitor \( C_{in} \) if not present, the signal source will be in parallel to resistor \( R_2 \) and the bias voltage of the transistor base will be changed.

Hence \( C_{in} \) allows, the AC signal from source to flow into input circuit, without affecting the bias conditions.
The Emitter By-pass Capacitor $C_e$

The emitter by-pass capacitor $C_e$ is connected in parallel to the emitter resistor. It offers a low reactance path to the amplified AC signal.

In the absence of this capacitor, the voltage developed across $R_E$ will feedback to the input side thereby reducing the output voltage. Thus in the presence of $C_e$ the amplified AC will pass through this.

Coupling Capacitor $C_C$

The capacitor $C_C$ is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the operating point from shifting. This is also called as blocking capacitor because it does not allow the DC voltage to pass through it.

In the absence of this capacitor, $R_C$ will come in parallel with the resistance $R_1$ of the biasing network of the next stage and thereby changing the biasing conditions of the next stage.

Amplifier Consideration

For an amplifier circuit, the overall gain of the amplifier is an important consideration. To achieve maximum voltage gain, let us find the most suitable transistor configuration for cascading.

CC Amplifier

- Its voltage gain is less than unity.
- It is not suitable for intermediate stages.

CB Amplifier

- Its voltage gain is less than unity.
- Hence not suitable for cascading.

CE Amplifier

- Its voltage gain is greater than unity.
- Voltage gain is further increased by cascading.

The characteristics of CE amplifier are such that, this configuration is very suitable for cascading in amplifier circuits. Hence most of the amplifier circuits use CE configuration.
Two Stage CE-CE Cascade Amplifier

The impact of input and output loading can be minimized by cascading two amplifiers with appropriate input and output characteristics. Multistage cascading can be used to create amplifiers with high input resistance, low output resistance and large gains.

The complication in calculating the gain of cascaded stages comes from the non-ideal coupling between stages due to loading. Two cascaded common emitter stages are shown in below figure. Because the input resistance of the second stage (resistors $R_1$ and $R_2$) forms a voltage divider with the output resistance ($R_{C1}$) of the first stage, the total gain is not simply the product of the gain for the individual (separated) stages.
Cascode Amplifier

AC equivalent circuit

h-parameter equivalent circuit
Darlington pair

Darlington pair 1- Two emitter follower stages in cascade with infinite emitter resistance in the first stage constitute a Darlington circuit.

Second Stage
Let us assume, $h_{oe}R_L<0.1$
Also $h_{fe}>>1$

$$A_{i2} = \frac{I_o}{I_2} = 1 + h_{fe} \approx h_{fe} - - - - - - (1)$$

$$R_{i2} = h_{ie} + (1 + h_{fe}) R_L \sim h_{ie} + h_{fe} R_L h_{fe} R_L \quad \text{(2)}$$

$$R_{i1} = R_{i2} = h_{fe} R_L \quad \text{(3)}$$

First Stage
$h_{oe}R_L = h_{oe}h_{fe}R_L < 0.1$. If this inequality is satisfied, then we can use simplified equivalent ckt in the first stage. Using exact solution

$$A_{i1} = \frac{-h_{fe}}{1 + h_{oe}R_{i1}}$$

$$A_{i1} = \frac{1 + h_{fe}}{1 + h_{oe}h_{fe}R_L} - - - - - - - - (4)$$

$$R_{i1} = h_{ie} + h_{re} A_{i1} R_{i1}$$
For emitter follower
\[ R_i = h_{ie} + (1+h_{fe}) R_L \]
\[ = h_{ie} + h_{ie} R_L \]

Overall current gain
\[ A_I = A_1 A_2 = \frac{h_{fe}^2}{1+h_{fe} R_L} \]

Emitter follower, \[ A_V = \frac{1-h_{ie}}{R_L} \] \hspace{1cm} (1)

Darlington ckt, \[ A_V = A_{V1} A_{V2} \]
\[ = \frac{1-h_{ie}}{R_L} \left( 2+h_{fe} R_L \right) \] \hspace{1cm} (2)

Effect of biasing network on the input resistance of emitter follower or Darlington ckt.
Effective input resistance \( R_i = R_1 \parallel R_2 \parallel R_i' \) where \( R_i' \) is a large input resistance of emitter follower or Darlington ckt.

\[
R_i = R_B \parallel R_i'
\]

\( \sim R_B \)

**Emitter follower with Boot Strap Biasing**

The reactance offered by the capacitor is very low for all frequencies.

\[
A_V = \frac{V_o}{V_i}
\]

\[\therefore \quad V_o = A_V V_i \approx V_i\]

\( R_3 \) can be replaced by Miller’s theorem

\[
R_{2i} = \frac{R_3}{1 - A_V} = \infty
\]

\[
R_{3o} = \frac{R_2}{1 - 1/A_V} = \frac{R_2 A_V}{A_V - 1}
\]

Effective output resistance

\[
R_L = R_o \parallel R_{3o} \parallel R_B
\]

\( \approx R_o \)
Coupling Schemes

Two-stage RC Coupled Amplifier

The resistance-capacitance coupling is, in short termed as RC coupling. This is the mostly used coupling technique in amplifiers.

Construction of a Two-stage RC Coupled Amplifier

The constructional details of a two-stage RC coupled transistor amplifier circuit are as follows. The two stage amplifier circuit has two transistors, connected in CE configuration and a common power supply $V_{CC}$ is used. The potential divider network $R_1$ and $R_2$ and the resistor $R_e$ form the biasing and stabilization network. The emitter by-pass capacitor $C_e$ offers a low reactance path to the signal.

The resistor $R_i$ is used as a load impedance. The input capacitor $C_{in}$ present at the initial stage of the amplifier couples AC signal to the base of the transistor. The capacitor $C_C$ is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the shift of operating point. The figure below shows the circuit diagram of RC coupled amplifier.

![Circuit Diagram of RC Coupled Amplifier](image)

Operation of RC Coupled Amplifier

When an AC input signal is applied to the base of first transistor, it gets amplified and appears at the collector load $R_L$ which is then passed through the coupling capacitor $C_C$ to the next stage. This becomes the input of the next stage, whose amplified output again appears across its collector load. Thus the signal is amplified in stage by stage action.

The important point that has to be noted here is that the total gain is less than the product of the gains of individual stages. This is because when a second stage is made to follow the first stage, the effective load resistance of the first stage is reduced due to the shunting
effect of the input resistance of the second stage. Hence, in a multistage amplifier, only the gain of the last stage remains unchanged.

As we consider a two stage amplifier here, the output phase is same as input. Because the phase reversal is done two times by the two stage CE configured amplifier circuit.

**Frequency Response of RC Coupled Amplifier**

Frequency response curve is a graph that indicates the relationship between voltage gain and function of frequency. The frequency response of a RC coupled amplifier is as shown in the following graph.

![Frequency Response Graph](image)

From the above graph, it is understood that the frequency rolls off or decreases for the frequencies below 50Hz and for the frequencies above 20 KHz. whereas the voltage gain for the range of frequencies between 50Hz and 20 KHz is constant.

We know that,

\[ X_C = \frac{1}{2\pi f_C} \]

It means that the capacitive reactance is inversely proportional to the frequency.

**At Low frequencies (i.e. below 50 Hz)**

The capacitive reactance is inversely proportional to the frequency. At low frequencies, the reactance is quite high. The reactance of input capacitor \( C_{in} \) and the coupling capacitor \( C_C \) are so high that only small part of the input signal is allowed. The reactance of the emitter by pass capacitor \( C_E \) is also very high during low frequencies. Hence it cannot shunt the emitter resistance effectively. With all these factors, the voltage gain rolls off at low frequencies.

**At High frequencies (i.e. above 20 KHz):** Again considering the same point, we know that the capacitive reactance is low at high frequencies. So, a capacitor behaves as a short
circuit, at high frequencies. As a result of this, the loading effect of the next stage increases, which reduces the voltage gain. Along with this, as the capacitance of emitter diode decreases, it increases the base current of the transistor due to which the current gain (β) reduces. Hence the voltage gain rolls off at high frequencies.

**At Mid-frequencies (i.e. 50 Hz to 20 KHz)**

The voltage gain of the capacitors is maintained constant in this range of frequencies, as shown in figure. If the frequency increases, the reactance of the capacitor \( C_c \) decreases which tends to increase the gain. But this lower capacitance reactive increases the loading effect of the next stage by which there is a reduction in gain.

Due to these two factors, the gain is maintained constant.

**Advantages of RC Coupled Amplifier**

The following are the advantages of RC coupled amplifier.

- The frequency response of RC amplifier provides constant gain over a wide frequency range, hence most suitable for audio applications.
- The circuit is simple and has lower cost because it employs resistors and capacitors which are cheap.
- It becomes more compact with the upgrading technology.

**Disadvantages of RC Coupled Amplifier**

The following are the disadvantages of RC coupled amplifier.

- The voltage and power gain are low because of the effective load resistance.
- They become noisy with age.
- Due to poor impedance matching, power transfer will be low.

**Applications of RC Coupled Amplifier**

The following are the applications of RC coupled amplifier.

- They have excellent audio fidelity over a wide range of frequency.
- Widely used as Voltage amplifiers
- Due to poor impedance matching, RC coupling is rarely used in the final stages.
We have observed that the main drawback of RC coupled amplifier is that the effective load resistance gets reduced. This is because, the input impedance of an amplifier is low, while its output impedance is high.

When they are coupled to make a multistage amplifier, the high output impedance of one stage comes in parallel with the low input impedance of next stage. Hence, effective load resistance is decreased. This problem can be overcome by a transformer coupled amplifier.

In a transformer-coupled amplifier, the stages of amplifier are coupled using a transformer. Let us go into the constructional and operational details of a transformer coupled amplifier.

**Construction of Transformer Coupled Amplifier**

The amplifier circuit in which, the previous stage is connected to the next stage using a coupling transformer, is called as Transformer coupled amplifier.

The coupling transformer T₁ is used to feed the output of 1st stage to the input of 2nd stage. The collector load is replaced by the primary winding of the transformer. The secondary winding is connected between the potential divider and the base of 2nd stage, which provides the input to the 2nd stage. Instead of coupling capacitor like in RC coupled amplifier, a transformer is used for coupling any two stages, in the transformer coupled amplifier circuit.

The figure below shows the circuit diagram of transformer coupled amplifier.

![Transformer Coupled Amplifier Circuit Diagram](image)

The potential divider network R₁ and R₂ and the resistor Rₑ together form the biasing and stabilization network. The emitter by-pass capacitor Cₑ offers a low reactance path to the signal. The resistor Rₗ is used as a load impedance. The input capacitor Cᵢₗ present at the initial stage of the amplifier couples AC signal to the base of the transistor. The capacitor
$C_C$ is the coupling capacitor that connects two stages and prevents DC interference between the stages and controls the shift of operating point.

**Operation of Transformer Coupled Amplifier**

When an AC signal is applied to the input of the base of the first transistor then it gets amplified by the transistor and appears at the collector to which the primary of the transformer is connected.

The transformer which is used as a coupling device in this circuit has the property of impedance changing, which means the low resistance of a stage (or load) can be reflected as a high load resistance to the previous stage. Hence the voltage at the primary is transferred according to the turns ratio of the secondary winding of the transformer.

This transformer coupling provides good impedance matching between the stages of amplifier. The transformer coupled amplifier is generally used for power amplification.

**Frequency Response of Transformer Coupled Amplifier**

The figure below shows the frequency response of a transformer coupled amplifier. The gain of the amplifier is constant only for a small range of frequencies. The output voltage is equal to the collector current multiplied by the reactance of primary.

At low frequencies, the reactance of primary begins to fall, resulting in decreased gain. At high frequencies, the capacitance between turns of windings acts as a bypass condenser to reduce the output voltage and hence gain.

So, the amplification of audio signals will not be proportionate and some distortion will also get introduced, which is called as **Frequency distortion**.

**Advantages of Transformer Coupled Amplifier**

- An excellent impedance matching is provided.
- Gain achieved is higher.
- There will be no power loss in collector and base resistors.
- Efficient in operation.
Disadvantages of Transformer Coupled Amplifier

The following are the disadvantages of a transformer coupled amplifier −

- Though the gain is high, it varies considerably with frequency. Hence a poor frequency response.
- Frequency distortion is higher.
- Transformers tend to produce hum noise.
- Transformers are bulky and costly.

Applications

The following are the applications of a transformer coupled amplifier −

- Mostly used for impedance matching purposes.
- Used for Power amplification.
- Used in applications where maximum power transfer is needed.

The other type of coupling amplifier is the direct coupled amplifier, which is especially used to amplify lower frequencies, such as amplifying photo-electric current or thermo-couple current or so.

Direct Coupled Amplifier

As no coupling devices are used, the coupling of the amplifier stages is done directly and hence called as **Direct coupled amplifier**.

Construction

The figure below indicates the three stage direct coupled transistor amplifier. The output of first stage transistor $T_1$ is connected to the input of second stage transistor $T_2$. 

![Diagram of Direct Coupled Amplifier]
The transistor in the first stage will be an NPN transistor, while the transistor in the next stage will be a PNP transistor and so on. This is because; the variations in one transistor tend to cancel the variations in the other. The rise in the collector current and the variation in $\beta$ of one transistor gets cancelled by the decrease in the other.

**Operation**

The input signal when applied at the base of transistor $T_1$, it gets amplified due to the transistor action and the amplified output appears at the collector resistor $R_c$ of transistor $T_1$. This output is applied to the base of transistor $T_2$ which further amplifies the signal. In this way, a signal is amplified in a direct coupled amplifier circuit.

**Advantages**

The advantages of direct coupled amplifier are as follows.

- The circuit arrangement is simple because of minimum use of resistors.
- The circuit is of low cost because of the absence of expensive coupling devices.

**Disadvantages**

The disadvantages of direct coupled amplifier are as follows.

- It cannot be used for amplifying high frequencies.
- The operating point is shifted due to temperature variations.

**Applications**

- Low frequency amplifications.
- Low current amplifications.

**Comparisons**

<table>
<thead>
<tr>
<th>S.No</th>
<th>Particular</th>
<th>RC Coupling</th>
<th>Transformer</th>
<th>Direct Coupling</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Frequency</td>
<td>Excellent in audio</td>
<td>Poor</td>
<td>Best</td>
</tr>
<tr>
<td>2</td>
<td>Cost</td>
<td>Less</td>
<td>More</td>
<td>Least</td>
</tr>
<tr>
<td>3</td>
<td>Space</td>
<td>Less</td>
<td>More</td>
<td>Least</td>
</tr>
<tr>
<td>4</td>
<td>Impedance</td>
<td>Not good</td>
<td>Excellent</td>
<td>Good</td>
</tr>
<tr>
<td>5</td>
<td>Use</td>
<td>For voltage</td>
<td>For power</td>
<td>For amplification</td>
</tr>
</tbody>
</table>
UNIT-II  
Feedback Amplifier & Oscillator

Feedback Amplifier

A practical amplifier has a gain of nearly one million \( i.e. \) its output is one million times the input. Consequently, even a casual disturbance at the input will appear in the amplified form in the output. There is a strong tendency in amplifiers to introduce \textit{hum} due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output. The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible. The noise level in amplifiers can be reduced considerably by the use of \textit{negative feedback} \( i.e. \) by injecting a fraction of output in phase opposition to the input signal. The object of this chapter is to consider the effects and methods of providing negative feedback in transistor amplifiers.

Ideally an amplifier should reproduce the input signal, with change in magnitude and with or without change in phase. But some of the shortcomings of the amplifier circuit are:

1. Change in the value of the gain due to variation in supplying voltage, temperature or due to components.
2. Distortion in wave-form due to non-linearities in the operating characters of the Amplifying device.
3. The amplifier may introduce noise (undesired signals)

The above drawbacks can be minimizing if we introduce feedback.

CLASSIFICATION OF AMPLIFIERS

Amplifiers can be classified broadly as:

1. Voltage amplifiers.
2. Current amplifiers.
3. Tran conductance amplifiers.
4. Tran resistance amplifiers.
1.1 Voltage amplifier

\[
\text{if } R_i \gg R_s \Rightarrow V_i \approx V_s
\]

and if \( R_o \ll R_L \) then

\[
V_o \approx A_v V_i \approx A_v V_s
\]

hence 
\[
A_v = \frac{V_o}{V_i}
\]

with \( R_L = \infty \)

represent the open circuit voltage gain.

1.2 Current amplifier

\[
\text{if } R_i \ll R_s \Rightarrow I_i \approx I_s
\]

and if \( R_o \gg R_L \) then

\[
I_o \approx A_i I_i \approx A_i I_s
\]

hence 
\[
A_i = \frac{I_o}{I_i}
\]

with \( R_L = 0 \)

represent the short circuit current gain.
1.3 Transconductance amplifier

\[
\text{if } R_i \gg R_s \\
\text{then } V_i \approx V_s \\
\text{and if } R_o \gg R_L \\
\text{then } I_o \approx G_m V_i \approx G_m V_s \\
\text{hence } G_m = \frac{I_o}{V_i} \\
\text{with } R_s = 0
\]

represent the short circuit mutual or transfer conductance

1.4 Transresistance amplifier

\[
\text{if } R_i \ll R_s \\
\text{then } I_i \approx I_s \\
\text{and if } R_o \ll R_L \\
\text{then } V_o \approx R_m I_i \approx R_m I_s \\
\text{hence } R_m = \frac{V_o}{I_i} \\
\text{with } R_s = \infty
\]

represent the open circuit mutual or transfer resistance.
Concept of Feedback

An amplifier circuit simply increases the signal strength. But while amplifying, it just increases the strength of its input signal whether it contains information or some noise along with information. This noise or some disturbance is introduced in the amplifiers because of their strong tendency to introduce hum due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output, which is very undesirable.

The noise level in the amplifier circuits can be considerably reduced by using negative feedback done by injecting a fraction of output in phase opposition to the input signal.

Principle of Feedback Amplifier

A feedback amplifier generally consists of two parts. They are the amplifier and the feedback circuit. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure.

![Feedback Amplifier Diagram](image)

From the above figure, the gain of the amplifier is represented as \( A \). the gain of the amplifier is the ratio of output voltage \( V_o \) to the input voltage \( V_i \). the feedback network extracts a voltage \( V_f = \beta V_o \) from the output \( V_o \) of the amplifier.

This voltage is added for positive feedback and subtracted for negative feedback, from the signal voltage \( V_s \). Now,

\[
V_i = V_s + V_f = V_s + \beta V_o \\
V_i = V_s - V_f = V_s - \beta V_o
\]

The quantity \( \beta = V_f/V_o \) is called as feedback ratio or feedback fraction.

Let us consider the case of negative feedback. The output \( V_o \) must be equal to the input voltage \( (V_s - \beta V_o) \) multiplied by the gain \( A \) of the amplifier.
Hence,

\[(V_s - \beta V_o)A = V_o\]

Or

\[AV_s - A\beta V_o = V_o\]

Or

\[AV_s = V_o(1 + A\beta)\]

Therefore,

\[\frac{V_o}{V_s} = \frac{A}{1 + A\beta}\]

Let \(A_f\) be the overall gain (gain with the feedback) of the amplifier. This is defined as the ratio of output voltage \(V_o\) to the applied signal voltage \(V_s\), i.e.,

\[A_f = \frac{A}{1 + A\beta}\]

The equation of gain of the feedback amplifier, with positive feedback is given by

\[A_f = \frac{A}{1 - A\beta}\]

These are the standard equations to calculate the gain of feedback amplifiers.

**Types of Feedbacks**

The process of injecting a fraction of output energy of some device back to the input is known as Feedback. It has been found that feedback is very useful in reducing noise and making the amplifier operation stable.

Depending upon whether the feedback signal aids or opposes the input signal, there are two types of feedbacks used.

**Positive Feedback**

The feedback in which the feedback energy i.e., either voltage or current is in phase with the input signal and thus aids it is called as Positive feedback.

Both the input signal and feedback signal introduces a phase shift of 180° thus making a 360° resultant phase shift around the loop, to be finally in phase with the input signal.

Though the positive feedback increases the gain of the amplifier, it has the disadvantages such as
• Increasing distortion
• Instability

It is because of these disadvantages the positive feedback is not recommended for the amplifiers. If the positive feedback is sufficiently large, it leads to oscillations, by which oscillator circuits are formed.

**Negative Feedback**

The feedback in which the feedback energy i.e., either voltage or current is out of phase with the input and thus opposes it, is called as negative feedback.

In negative feedback, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it produces no phase shift or zero phase shift. Thus the resultant feedback voltage \( V_f \) is 180° out of phase with the input signal \( V_{in} \).

Though the gain of negative feedback amplifier is reduced, there are many advantages of negative feedback such as

• Stability of gain is improved
• Reduction in distortion
• Reduction in noise
• Increase in input impedance
• Decrease in output impedance
• Increase in the range of uniform application

It is because of these advantages negative feedback is frequently employed in amplifiers.

Negative feedback in an amplifier is the method of feeding a portion of the amplified output to the input but in opposite phase. The phase opposition occurs as the amplifier provides 180° phase shift whereas the feedback network doesn’t.

While the output energy is being applied to the input, for the voltage energy to be taken as feedback, the output is taken in shunt connection and for the current energy to be taken as feedback, the output is taken in series connection.

There are two main types of negative feedback circuits. They are –

• Negative Voltage Feedback
• Negative Current Feedback
Negative Voltage Feedback

In this method, the voltage feedback to the input of amplifier is proportional to the output voltage. This is further classified into two types –

- Voltage-series feedback
- Voltage-shunt feedback

Negative Current Feedback

In this method, the voltage feedback to the input of amplifier is proportional to the output current. This is further classified into two types.

- Current-series feedback
- Current-shunt feedback

Let us have a brief idea on all of them.

Voltage-Series Feedback

In the voltage series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as shunt-driven series-fed feedback, i.e., a parallel-series circuit.

The following figure shows the block diagram of voltage series feedback, by which it is evident that the feedback circuit is placed in shunt with the output but in series with the input.

![Block Diagram of Voltage Series Feedback](image)

As the feedback circuit is connected in shunt with the output, the output impedance is decreased and due to the series connection with the input, the input impedance is increased.
Voltage-Shunt Feedback

In the voltage shunt feedback circuit, a fraction of the output voltage is applied in parallel with the input voltage through the feedback network. This is also known as shunt-driven shunt-fed feedback i.e., a parallel-parallel prototype.

The below figure shows the block diagram of voltage shunt feedback, by which it is evident that the feedback circuit is placed in shunt with the output and also with the input.

As the feedback circuit is connected in shunt with the output and the input as well, both the output impedance and the input impedance are decreased.

Current-Series Feedback

In the current series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as series-driven series-fed feedback i.e., a series-series circuit.

The following figure shows the block diagram of current series feedback, by which it is evident that the feedback circuit is placed in series with the output and also with the input.

As the feedback circuit is connected in series with the output and the input as well, both the output impedance and the input impedance are increased.
Current-Shunt Feedback

In the current shunt feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as series-driven shunt-fed feedback i.e., a series-parallel circuit.

The below figure shows the block diagram of current shunt feedback, by which it is evident that the feedback circuit is placed in series with the output but in parallel with the input.

![Current Shunt Feedback Diagram](image)

As the feedback circuit is connected in series with the output, the output impedance is increased and due to the parallel connection with the input, the input impedance is decreased.

Let us now tabulate the amplifier characteristics that get affected by different types of negative feedbacks.

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Advantages of Negative Feedback

1. Stabilization of gain
   - Make the gain less sensitive to changes in circuit components e.g. due to changes in temperature.

2. Reduce non-linear distortion
   - Make the output proportional to the input, keeping the gain constant, independent of signal level.

3. Reduce the effect of noise
   - Minimize the contribution to the output of unwanted signals generated in circuit components or extraneous interference.

4. Extend the bandwidth of the amplifier
   - Reduce the gain and increase the bandwidth

5. Modification the input and output impedances
   - Raise or lower the input and output impedances by selection of the appropriate feedback topology.

Oscillators

An oscillator generates output without any ac input signal. An electronic oscillator is a circuit which converts dc energy into ac at a very high frequency. An amplifier with a positive feedback can be understood as an oscillator.

Amplifier vs. Oscillator

An amplifier increases the signal strength of the input signal applied, whereas an oscillator generates a signal without that input signal, but it requires dc for its operation. This is the main difference between an amplifier and an oscillator.

Take a look at the following illustration. It clearly shows how an amplifier takes energy from d.c. power source and converts it into a.c. energy at signal frequency. An oscillator produces an oscillating a.c. signal on its own.
The frequency, waveform, and magnitude of a.c. power generated by an amplifier, is controlled by the a.c. signal voltage applied at the input, whereas those for an oscillator are controlled by the components in the circuit itself, which means no external controlling voltage is required.

**Alternator vs. Oscillator**

An alternator is a mechanical device that produces sinusoidal waves without any input. This a.c. generating machine is used to generate frequencies up to 1000Hz. The output frequency depends on the number of poles and the speed of rotation of the armature.

The following points highlight the differences between an alternator and an oscillator –

- An alternator converts mechanical energy to a.c. energy, whereas the oscillator converts d.c. energy into a.c. energy.
- An oscillator can produce higher frequencies of several MHz whereas an alternator cannot.
- An alternator has rotating parts, whereas an electronic oscillator doesn’t.
- It is easy to change the frequency of oscillations in an oscillator than in an alternator.

Oscillators can also be considered as opposite to rectifiers that convert a.c. to d.c. as these convert d.c. to a.c.

**Classification of Oscillators**

Electronic oscillators are classified mainly into the following two categories –

- **Sinusoidal Oscillators** – The oscillators that produce an output having a sine waveform are called sinusoidal or harmonic oscillators. Such oscillators can provide output at frequencies ranging from 20 Hz to 1 GHz.
- **Non-sinusoidal Oscillators** – The oscillators that produce an output having a square, rectangular or saw-tooth waveform are called non-sinusoidal or relaxation oscillators. Such oscillators can provide output at frequencies ranging from 0 Hz to 20 MHz.

**Sinusoidal Oscillators**

Sinusoidal oscillators can be classified in the following categories –
• **Tuned Circuit Oscillators** – These oscillators use a tuned-circuit consisting of inductors (L) and capacitors (C) and are used to generate high-frequency signals. Thus they are also known as radio frequency R.F. oscillators. Such oscillators are Hartley, Colpitts, Clapp-oscillators etc.

• **RC Oscillators** – There oscillators use resistors and capacitors and are used to generate low or audio-frequency signals. Thus they are also known as audio-frequency (A.F.) oscillators. Such oscillators are Phase –shift and Wein-bridge oscillators.

• **Crystal Oscillators** – These oscillators use quartz crystals and are used to generate highly stabilized output signal with frequencies up to 10 MHz. The Piezo oscillator is an example of a crystal oscillator.

• **Negative-resistance Oscillator** – These oscillators use negative-resistance characteristic of the devices such as tunnel devices. A tuned diode oscillator is an example of a negative-resistance oscillator.

**Nature of Sinusoidal Oscillations**

The nature of oscillations in a sinusoidal wave is generally of two types. They are **damped** and **undamped oscillations**.

**Damped Oscillations**

The electrical oscillations whose amplitude goes on decreasing with time are called as **Damped Oscillations**. The frequency of the damped oscillations may remain constant depending upon the circuit parameters.

Damped oscillations are generally produced by the oscillatory circuits that produce power losses and doesn't compensate if required.
Undamped Oscillations

The electrical oscillations whose amplitude remains constant with time are called as Undamped Oscillations. The frequency of the undamped oscillations remains constant.

Undamped oscillations are generally produced by the oscillatory circuits that produce no power losses and follow compensation techniques if any power losses occur.

An amplifier with positive feedback produces its output to be in phase with the input and increases the strength of the signal. Positive feedback is also called as degenerative feedback or direct feedback. This kind of feedback makes a feedback amplifier, an oscillator.

The use of positive feedback results in a feedback amplifier having closed-loop gain greater than the open-loop gain. It results in instability and operates as an oscillatory circuit. An oscillatory circuit provides a constantly varying amplified output signal of any desired frequency.

The Barkhausen Criterion

With the knowledge we have till now, we understood that a practical oscillator circuit consists of a tank circuit, a transistor amplifier circuit and a feedback circuit. So, let us now try to brush up the concept of feedback amplifiers, to derive the gain of the feedback amplifiers.

Principle of Feedback Amplifier

A feedback amplifier generally consists of two parts. They are the amplifier and the feedback circuit. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure below.
From the above figure, the gain of the amplifier is represented as $A$. The gain of the amplifier is the ratio of output voltage $V_o$ to the input voltage $V_i$. The feedback network extracts a voltage $V_f = \beta V_o$ from the output $V_o$ of the amplifier.

This voltage is added for positive feedback and subtracted for negative feedback, from the signal voltage $V_s$.

So, for a positive feedback,

$$V_i = V_s + V_f = V_s + \beta V_o$$

The quantity $\beta = \frac{V_f}{V_o}$ is called as feedback ratio or feedback fraction.

The output $V_o$ must be equal to the input voltage $(V_s + \beta V_o)$ multiplied by the gain $A$ of the amplifier.

Hence,

$$(V_s + \beta V_0)A = V_0$$

Or

$$AV_s + A\beta V_o = V_0$$

Or

$$AV_s = V_o(1 - A\beta)$$

Therefore

$$\frac{V_o}{V_s} = \frac{A}{1 - A\beta}$$

Let $A_f$ be the overall gain (gain with the feedback) of the amplifier. This is defined as the ratio of output voltage $V_o$ to the applied signal voltage $V_s$, i.e.,

$$A_f = \frac{V_o}{V_s}$$
from the above two equations, we can understand that, the equation of gain of the feedback amplifier with positive feedback is given by

\[ A_f = \frac{A}{1 - A\beta} \]

Where \( A\beta \) is the feedback factor or the loop gain.

If \( A\beta = 1, A_I = \infty \). Thus the gain becomes infinity, i.e., there is output without any input. In another words, the amplifier works as an Oscillator.

The condition \( A\beta = 1 \) is called as Barkhausen Criterion of oscillations. This is a very important factor to be always kept in mind, in the concept of Oscillators.

**RC-Phase–shift Oscillators**

**Principle of Phase-shift oscillators**

We know that the output voltage of an RC circuit for a sinewave input leads the input voltage. The phase angle by which it leads is determined by the value of RC components used in the circuit. The following circuit diagram shows a single section of an RC network.

The output voltage \( V_1' \) across the resistor \( R \) leads the input voltage applied input \( V_1 \) by some phase angle \( \phi^o \). If \( R \) were reduced to zero, \( V_1' \) will lead the \( V_1 \) by 90\(^o\) i.e., \( \phi^o = 90^o \).

However, adjusting \( R \) to zero would be impracticable, because it would lead to no voltage across \( R \). Therefore, in practice, \( R \) is varied to such a value that makes \( V_1' \) to lead \( V_1 \) by 60\(^o\). The following circuit diagram shows the three sections of the RC network.

Each section produces a phase shift of 60\(^o\). Consequently, a total phase shift of 180\(^o\) is produced, i.e., voltage \( V_2 \) leads the voltage \( V_1 \) by 180\(^o\).
Phase-shift Oscillator Circuit

The oscillator circuit that produces a sine wave using a phase-shift network is called as a Phase-shift oscillator circuit. The constructional details and operation of a phase-shift oscillator circuit are as given below.

Construction

The phase-shift oscillator circuit consists of a single transistor amplifier section and a RC phase-shift network. The phase shift network in this circuit, consists of three RC sections. At the resonant frequency $f_o$, the phase shift in each RC section is $60^\circ$ so that the total phase shift produced by RC network is $180^\circ$.

The following circuit diagram shows the arrangement of an RC phase-shift oscillator.

![Circuit Diagram]

The frequency of oscillations is given by

$$f_o = \frac{1}{2\pi RC \sqrt{6}}$$

Where

- $R_1 = R_2 = R_3 = R$
- $C_1 = C_2 = C_3 = C$
Operation

The circuit when switched ON oscillates at the resonant frequency $f_0$. The output $E_o$ of the amplifier is fed back to RC feedback network. This network produces a phase shift of $180^\circ$ and a voltage $E_i$ appears at its output. This voltage is applied to the transistor amplifier.

The feedback applied will be

$$m = \frac{E_i}{E_o}$$

The feedback is in correct phase, whereas the transistor amplifier, which is in CE configuration, produces a $180^\circ$ phase shift. The phase shift produced by network and the transistor add to form a phase shift around the entire loop which is $360^\circ$.

Advantages

The advantages of RC phase shift oscillator are as follows –

- It does not require transformers or inductors.
- It can be used to produce very low frequencies.
- The circuit provides good frequency stability.

Disadvantages

The disadvantages of RC phase shift oscillator are as follows –

- Starting the oscillations is difficult as the feedback is small.
- The output produced is small.

Another type of popular audio frequency oscillator is the Wien bridge oscillator circuit. This is mostly used because of its important features. This circuit is free from the circuit fluctuations and the ambient temperature.

The main advantage of this oscillator is that the frequency can be varied in the range of 10Hz to about 1MHz whereas in RC oscillators, the frequency is not varied.

Wien bridge oscillator

Construction

The circuit construction of Wien bridge oscillator can be explained as below. It is a two-stage amplifier with RC bridge circuit. The bridge circuit has the arms $R_1C_1$, $R_3$, $R_2C_2$ and the tungsten lamp $L_p$. Resistance $R_3$ and the lamp $L_p$ are used to stabilize the amplitude of the output.
The following circuit diagram shows the arrangement of a Wien bridge oscillator.

The transistor T₁ serves as an oscillator and an amplifier while the other transistor T₂ serves as an inverter. The inverter operation provides a phase shift of 180°. This circuit provides positive feedback through R₁C₁, C₂R₂ to the transistor T₁ and negative feedback through the voltage divider to the input of transistor T₂.

The frequency of oscillations is determined by the series element R₁C₁ and parallel element R₂C₂ of the bridge.

\[
f = \frac{1}{2\pi \sqrt{R_1 C_1 R_2 C_2}}
\]

If \( R_1 = R_2 \) and \( C_1 = C_2 = C \)

Then,

\[
f = \frac{1}{2\pi RC}
\]
Now, we can simplify the above circuit as follows –

The oscillator consists of two stages of RC coupled amplifier and a feedback network. The voltage across the parallel combination of R and C is fed to the input of amplifier 1. The net phase shift through the two amplifiers is zero.

The usual idea of connecting the output of amplifier 2 to amplifier 1 to provide signal regeneration for oscillator is not applicable here as the amplifier 1 will amplify signals over a wide range of frequencies and hence direct coupling would result in poor frequency stability. By adding Wien bridge feedback network, the oscillator becomes sensitive to a particular frequency and hence frequency stability is achieved.

**Operation**

When the circuit is switched ON, the bridge circuit produces oscillations of the frequency stated above. The two transistors produce a total phase shift of 360° so that proper positive feedback is ensured. The negative feedback in the circuit ensures constant output. This is achieved by temperature sensitive tungsten lamp $L_p$. Its resistance increases with current.

If the amplitude of the output increases, more current is produced and more negative feedback is achieved. Due to this, the output would return to the original value. Whereas, if the output tends to decrease, reverse action would take place.

**Advantages**

The advantages of Wien bridge oscillator are as follows –

- The circuit provides good frequency stability.
- It provides constant output.
- The operation of circuit is quite easy.
- The overall gain is high because of two transistors.
- The frequency of oscillations can be changed easily.
- The amplitude stability of the output voltage can be maintained more accurately, by replacing $R_2$ with a thermistor.

**Disadvantages**

The disadvantages of Wien bridge oscillator are as follows –

- The circuit cannot generate very high frequencies.
- Two transistors and number of components are required for the circuit construction.

**LC Oscillators**

An oscillatory circuit produces electrical oscillations of a desired frequency. They are also known as **tank circuits**.

A simple tank circuit comprises of an inductor $L$ and a capacitor $C$ both of which together determine the oscillatory frequency of the circuit.

To understand the concept of oscillatory circuit, let us consider the following circuit. The capacitor in this circuit is already charged using a dc source. In this situation, the upper plate of the capacitor has excess of electrons whereas the lower plate has deficit of electrons. The capacitor holds some electrostatic energy and there is a voltage across the capacitor.

When the switch $S$ is closed, the capacitor discharges and the current flows through the inductor. Due to the inductive effect, the current builds up slowly towards a maximum value. Once the capacitor discharges completely, the magnetic field around the coil is maximum.
Now, let us move on to the next stage. Once the capacitor is discharged completely, the magnetic field begins to collapse and produces a counter EMF according to Lenz’s law. The capacitor is now charged with positive charge on the upper plate and negative charge on the lower plate.

Once the capacitor is fully charged, it starts to discharge to build up a magnetic field around the coil, as shown in the following circuit diagram.

This continuation of charging and discharging results in alternating motion of electrons or an oscillatory current. The interchange of energy between L and C produce continuous oscillations.

In an ideal circuit, where there are no losses, the oscillations would continue indefinitely. In a practical tank circuit, there occur losses such as resistive and radiation losses in the coil and dielectric losses in the capacitor. These losses result in damped oscillations.

**Frequency of Oscillations**

The frequency of the oscillations produced by the tank circuit are determined by the components of the tank circuit, the L and the C. The actual frequency of oscillations is the resonant frequency (or natural frequency) of the tank circuit which is given by

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Capacitance of the capacitor
The frequency of oscillation \( f_o \) is inversely proportional to the square root of the capacitance of a capacitor. So, if the value of the capacitor used is large, the charge and discharge time periods will be large. Hence the frequency will be lower.

Mathematically, the frequency,
\[
f_o \propto \frac{1}{\sqrt{C}}
\]

**Self-Inductance of the coil**

The frequency of the oscillation \( f_o \) is proportional to the square root of the self-inductance of the coil. If the value of the inductance is large, the opposition to change of current flow is greater and hence the time required to complete each cycle will be longer, which means time period will be longer and frequency will be lower.

Mathematically, the frequency,
\[
f_o \propto \frac{1}{\sqrt{L}}
\]

Combining both the above equations,
\[
f_o \propto \frac{1}{\sqrt{LC}}
\]
\[
f_o = \frac{1}{2\pi\sqrt{LC}}
\]

The above equation, though indicates the output frequency, matches the **natural frequency** or **resonance frequency** of the tank circuit.

An Oscillator circuit is a complete set of all the parts of circuit which helps to produce the oscillations. These oscillations should sustain and should be Undamped as just discussed before. Let us try to analyze a practical Oscillator circuit to have a better understanding on how an Oscillator circuit works.

**Practical Oscillator Circuit**

A Practical Oscillator circuit consists of a tank circuit, a transistor amplifier, and a feedback circuit. The following circuit diagram shows the arrangement of a practical oscillator.
Let us now discuss the parts of this practical oscillator circuit.

**Tank Circuit** – The tank circuit consists of an inductance L connected in parallel with capacitor C. The values of these two components determine the frequency of the oscillator circuit and hence this is called as **Frequency determining circuit**.

- **Transistor Amplifier** – The output of the tank circuit is connected to the amplifier circuit so that the oscillations produced by the tank circuit are amplified here. Hence the output of these oscillations are increased by the amplifier.

- **Feedback Circuit** – The function of feedback circuit is to transfer a part of the output energy to LC circuit in proper phase. This feedback is positive in oscillators while negative in amplifiers.

**Frequency Stability of an Oscillator**

The frequency stability of an oscillator is a measure of its ability to maintain a constant frequency, over a long time interval. When operated over a longer period of time, the oscillator frequency may have a drift from the previously set value either by increasing or by decreasing.

The change in oscillator frequency may arise due to the following factors –

- Operating point of the active device such as BJT or FET used should lie in the linear region of the amplifier. Its deviation will affect the oscillator frequency.

- The temperature dependency of the performance of circuit components affect the oscillator frequency.

- The changes in d.c. supply voltage applied to the active device, shift the oscillator frequency. This can be avoided if a regulated power supply is used.

- A change in output load may cause a change in the Q-factor of the tank circuit, thereby causing a change in oscillator output frequency.

- The presence of inter element capacitances and stray capacitances affect the oscillator output frequency and thus frequency stability.

Tuned circuit oscillators are the circuits that produce oscillations with the help of tuning circuits. The tuning circuits consists of an inductance L and a capacitor C. These are also known as **LC oscillators**, **resonant circuit oscillators** or **tank circuit oscillators**.
The tuned circuit oscillators are used to produce an output with frequencies ranging from 1 MHz to 500 MHz. Hence these are also known as **R.F. Oscillators**. A BJT or a FET is used as an amplifier with tuned circuit oscillators. With an amplifier and an LC tank circuit, we can feedback a signal with right amplitude and phase to maintain oscillations.

**Types of Tuned Circuit Oscillators**

Most of the oscillators used in radio transmitters and receivers are of LC oscillators type. Depending upon the way the feedback is used in the circuit, the LC oscillators are divided as the following types.

- **Hartley Oscillator** – It uses inductive feedback.
- **Colpitts Oscillator** – It uses capacitive feedback.
- **Clapp Oscillator** – It uses capacitive feedback.

**Hartley Oscillator**

A very popular **local oscillator** circuit that is mostly used in **radio receivers** is the **Hartley Oscillator** circuit. The constructional details and operation of a Hartley oscillator are as discussed below.

**Construction**

In the circuit diagram of a Hartley oscillator shown below, the resistors R1, R2 and Re provide necessary bias condition for the circuit. The capacitor Ce provides a.c. ground thereby providing any signal degeneration. This also provides temperature stabilization.

The capacitors Cc andCb are employed to block d.c. and to provide an a.c. path. The radio frequency choke (R.F.C) offers very high impedance to high frequency currents which means it shorts for d.c. and opens for a.c. Hence it provides d.c. load for collector and keeps a.c. currents out of d.c. supply source.

**Tank Circuit**

The frequency determining network is a parallel resonant circuit which consists of the inductors L1 and L2 along with a variable capacitor C. The junction of L1 and L2 are earthed. The coil L1 has its one end connected to base via Cc and the other to emitter via Ce. So, L2 is in the output circuit. Both the coils L1 and L2 are inductively coupled and together form an **Auto-transformer**.

The following circuit diagram shows the arrangement of a Hartley oscillator. The tank circuit is **shunt fed** in this circuit. It can also be a **series-fed**.
**Operation**

When the collector supply is given, a transient current is produced in the oscillatory or tank circuit. The oscillatory current in the tank circuit produces a.c. voltage across \( L_1 \).

The **auto-transformer** made by the inductive coupling of \( L_1 \) and \( L_2 \) helps in determining the frequency and establishes the feedback. As the CE configured transistor provides 180° phase shift, another 180° phase shift is provided by the transformer, which makes 360° phase shift between the input and output voltages.

This makes the feedback positive which is essential for the condition of oscillations. When the **loop gain** \(|\beta A|\) of the amplifier is greater than one, oscillations are sustained in the circuit.

**Frequency**

The equation for **frequency of Hartley oscillator** is given as
\[
    f = \frac{1}{2\pi \sqrt{L_T C}}
\]

\[
    L_T = L_1 + L_2 + 2M
\]

Here, \(L_T\) is the total cumulatively coupled inductance; \(L_1\) and \(L_2\) represent inductances of 1\(^{st}\) and 2\(^{nd}\) coils; and \(M\) represents mutual inductance.

**Mutual inductance** is calculated when two windings are considered.

### Advantages

The advantages of Hartley oscillator are

- Instead of using a large transformer, a single coil can be used as an auto-transformer.
- Frequency can be varied by employing either a variable capacitor or a variable inductor.
- Less number of components are sufficient.
- The amplitude of the output remains constant over a fixed frequency range.

### Disadvantages

The disadvantages of Hartley oscillator are

- It cannot be a low frequency oscillator.
- Harmonic distortions are present.

### Applications

The applications of Hartley oscillator are

- It is used to produce a sine wave of desired frequency.
- Mostly used as a local oscillator in radio receivers.
- It is also used as R.F. Oscillator.

### Colpitts oscillator

A Colpitts oscillator looks just like the Hartley oscillator but the inductors and capacitors are replaced with each other in the tank circuit. The constructional details and operation of a colpitts oscillator are as discussed below.
Construction

Let us first take a look at the circuit diagram of a Colpitts oscillator.

The resistors $R_1$, $R_2$ and $R_e$ provide necessary bias condition for the circuit. The capacitor $C_e$ provides a.c. ground thereby providing any signal degeneration. This also provides temperature stabilization.

The capacitors $C_c$ and $C_b$ are employed to block d.c. and to provide an a.c. path. The radio frequency choke (R.F.C) offers very high impedance to high frequency currents which means it shorts for d.c. and opens for a.c. Hence it provides d.c. load for collector and keeps a.c. currents out of d.c. supply source.

Tank Circuit

The frequency determining network is a parallel resonant circuit which consists of variable capacitors $C_1$ and $C_2$ along with an inductor $L$. The junction of $C_1$ and $C_2$ are earthed. The capacitor $C_1$ has its one end connected to base via $C_c$ and the other to emitter via $C_e$. the voltage developed across $C_1$ provides the regenerative feedback required for the sustained oscillations.

Operation

When the collector supply is given, a transient current is produced in the oscillatory or tank circuit. The oscillatory current in the tank circuit produces a.c. voltage across $C_1$ which are
applied to the base emitter junction and appear in the amplified form in the collector circuit and supply losses to the tank circuit.

If terminal 1 is at positive potential with respect to terminal 3 at any instant, then terminal 2 will be at negative potential with respect to 3 at that instant because terminal 3 is grounded. Therefore, points 1 and 2 are out of phase by 180°.

As the CE configured transistor provides 180° phase shift, it makes 360° phase shift between the input and output voltages. Hence, feedback is properly phased to produce continuous Undamped oscillations. When the loop gain \(|\beta A|\) of the amplifier is greater than one, oscillations are sustained in the circuit.

**Frequency**

The equation for **frequency of Colpitts oscillator** is given as

\[ f = \frac{1}{2\pi \sqrt{LC_T}} \]

\(C_T\) is the total capacitance of \(C_1\) and \(C_2\) connected in series.

\[
\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2}
\]

\[
C_T = \frac{C_1 \times C_2}{C_1 + C_2}
\]

**Advantages**

The advantages of Colpitts oscillator are as follows –

- Colpitts oscillator can generate sinusoidal signals of very high frequencies.
- It can withstand high and low temperatures.
- The frequency stability is high.
- Frequency can be varied by using both the variable capacitors.
- Less number of components are sufficient.
- The amplitude of the output remains constant over a fixed frequency range.

The Colpitts oscillator is designed to eliminate the disadvantages of Hartley oscillator and is known to have no specific disadvantages. Hence there are many applications of a colpitts oscillator.
Applications

The applications of Colpitts oscillator are as follows –

- Colpitts oscillator can be used as High frequency sinewave generator.
- This can be used as a temperature sensor with some associated circuitry.
- Mostly used as a local oscillator in radio receivers.
- It is also used as R.F. Oscillator.
- It is also used in Mobile applications.
- It has got many other commercial applications.

Clapp Oscillator

Another oscillator which is an advanced version of Colpitts oscillator is the Clapp Oscillator. This circuit is designed by making a few changes to the Colpitts oscillator.

The circuit differs from the Colpitts oscillator only in one respect; it contains one additional capacitor \( C_3 \) connected in series with the inductor. The addition of capacitor \( C_3 \) improves the frequency stability and eliminates the effect of transistor parameters and stray capacitances.

The following circuit diagram shows the arrangement of a transistor Clapp oscillator.
The operation of Clapp oscillator circuit is in the same way as that of Colpitts oscillator. The frequency of oscillator is given by the relation,

$$f_o = \frac{1}{2\pi \sqrt{L \cdot C}}$$

Where

$$C = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$

Usually, the value of $C_3$ is much smaller than $C_1$ and $C_2$. As a result of this, $C$ is approximately equal to $C_3$. Therefore, the frequency of oscillation,

$$f_o = \frac{1}{2\pi \sqrt{L \cdot C_3}}$$

It is understood that the Clapp oscillator is similar to the Colpitts oscillator, however they differ in the way the inductances and capacitances are arranged. The frequency stability though is good, can be variable in a Clapp oscillator.

A Clapp oscillator is sometimes preferred over a Colpitts oscillator for constructing a variable frequency oscillator. The Clapp oscillators are used in receiver tuning circuits as a frequency oscillator.

One of the important features of an oscillator is that the feedback energy applied should be in correct phase to the tank circuit. The oscillator circuits discussed so far has employed inductor (L) and capacitor (C) combination, in the tank circuit or frequency determining circuit.

We have observed that the LC combination in oscillators provide 180° phase shift and transistor in CE configuration provide 180° phase shift to make a total of 360° phase shift so that it would make a zero difference in phase.

**Drawbacks of LC circuits**

Though they have few applications, the LC circuits have few drawbacks such as

- Frequency instability
- Waveform is poor
- Cannot be used for low frequencies
- Inductors are bulky and expensive
Whenever an oscillator is under continuous operation, its \textit{frequency stability} gets affected. There occur changes in its frequency. The main factors that affect the frequency of an oscillator are

- Power supply variations
- Changes in temperature
- Changes in load or output resistance

In RC and LC oscillators the values of resistance, capacitance and inductance vary with temperature and hence the frequency gets affected. In order to avoid this problem, the piezo electric crystals are being used in oscillators.

\textbf{Crystal Oscillators}

The use of piezo electric crystals in parallel resonant circuits provide high frequency stability in oscillators. Such oscillators are called as \textit{Crystal Oscillators}.

\textbf{Crystal Oscillators}

The principle of crystal oscillators depends upon the \textit{Piezo electric effect}. The natural shape of a crystal is hexagonal. When a crystal wafer is cut perpendicular to X-axis, it is called as X-cut and when it is cut along Y-axis, it is called as Y-cut.

The crystal used in crystal oscillator exhibits a property called as Piezo electric property. So, let us have an idea on piezo electric effect.

\textbf{Piezo Electric Effect}

The crystal exhibits the property that when a mechanical stress is applied across one of the faces of the crystal, a potential difference is developed across the opposite faces of the crystal. Conversely, when a potential difference is applied across one of the faces, a mechanical stress is produced along the other faces. This is known as \textit{Piezo electric effect}.

Certain crystalline materials like Rochelle salt, quartz and tourmaline exhibit piezo electric effect and such materials are called as \textit{Piezo electric crystals}. Quartz is the most commonly used piezo electric crystal because it is inexpensive and readily available in nature.

When a piezo electric crystal is subjected to a proper alternating potential, it vibrates mechanically. The amplitude of mechanical vibrations becomes maximum when the frequency of alternating voltage is equal to the natural frequency of the crystal.
Working of a Quartz Crystal

In order to make a crystal work in an electronic circuit, the crystal is placed between two metal plates in the form of a capacitor. Quartz is the mostly used type of crystal because of its availability and strong nature while being inexpensive. The ac voltage is applied in parallel to the crystal.

The circuit arrangement of a Quartz Crystal will be as shown below –

If an AC voltage is applied, the crystal starts vibrating at the frequency of the applied voltage. However, if the frequency of the applied voltage is made equal to the natural frequency of the crystal, resonance takes place and crystal vibrations reach a maximum value. This natural frequency is almost constant.

Equivalent circuit of a Crystal

If we try to represent the crystal with an equivalent electric circuit, we have to consider two cases, i.e., when it vibrates and when it doesn’t. The figures below represent the symbol and electrical equivalent circuit of a crystal respectively.

The above equivalent circuit consists of a series R-L-C circuit in parallel with a capacitance $C_m$. When the crystal mounted across the AC source is not vibrating, it is equivalent to the capacitance $C_m$. When the crystal vibrates, it acts like a tuned R-L-C circuit.
Frequency response

The frequency response of a crystal is as shown below. The graph shows the reactance ($X_L$ or $X_C$) versus frequency ($f$). It is evident that the crystal has two closely spaced resonant frequencies.

![Graph showing frequency response of a crystal](image)

The first one is the series resonant frequency ($f_s$), which occurs when reactance of the inductance ($L$) is equal to the reactance of the capacitance $C$. In that case, the impedance of the equivalent circuit is equal to the resistance $R$ and the frequency of oscillation is given by the relation,

$$f = \frac{1}{2\pi \sqrt{L \cdot C}}$$

The second one is the parallel resonant frequency ($f_p$), which occurs when the reactance of $R$-$L$-$C$ branch is equal to the reactance of capacitor $C_m$. At this frequency, the crystal offers a very high impedance to the external circuit and the frequency of oscillation is given by the relation.

$$f_p = \frac{1}{2\pi \sqrt{L \cdot C_T}}$$

Where

$$C_T = \frac{C C_m}{C + C_m}$$

The value of $C_m$ is usually very large as compared to $C$. Therefore, the value of $C_T$ is approximately equal to $C$ and hence the series resonant frequency is approximately equal to the parallel resonant frequency (i.e., $f_s = f_p$).
Crystal Oscillator Circuit

pierce crystal oscillator

A crystal oscillator circuit can be constructed in a number of ways like a Crystal controlled tuned collector oscillator, a Colpitts crystal oscillator, a Clap crystal oscillator etc. But the **transistor pierce crystal oscillator** is the most commonly used one. This is the circuit which is normally referred as a crystal oscillator circuit.

The following circuit diagram shows the arrangement of a transistor pierce crystal oscillator.

![Circuit Diagram](image)

In this circuit, the crystal is connected as a series element in the feedback path from collector to the base. The resistors $R_1$, $R_2$ and $R_E$ provide a voltage-divider stabilized d.c. bias circuit. The capacitor $C_E$ provides a.c. bypass of the emitter resistor and RFC (radio frequency choke) coil provides for d.c. bias while decoupling any a.c. signal on the power lines from affecting the output signal. The coupling capacitor $C$ has negligible impedance at the circuit operating frequency. But it blocks any d.c. between collector and base.

The circuit frequency of oscillation is set by the series resonant frequency of the crystal and its value is given by the relation,

$$f = \frac{1}{2\pi \sqrt{L \cdot C}}$$

It may be noted that the changes in supply voltage, transistor device parameters etc. have no effect on the circuit operating frequency, which is held stabilized by the crystal.
Advantages

The advantages of crystal oscillator are as follows –

- They have a high order of frequency stability.
- The quality factor (Q) of the crystal is very high.

Disadvantages

The disadvantages of crystal oscillator are as follows –

- They are fragile and can be used in low power circuits.
- The frequency of oscillations cannot be changed appreciably.

Frequency Stability of an Oscillator

An Oscillator is expected to maintain its frequency for a longer duration without any variations, so as to have a smoother clear sinewave output for the circuit operation. Hence the term frequency stability really matters a lot, when it comes to oscillators, whether sinusoidal or non-sinusoidal.

The frequency stability of an oscillator is defined as the ability of the oscillator to maintain the required frequency constant over a long time interval as possible. Let us try to discuss the factors that affect this frequency stability.

Change in operating point

We have already come across the transistor parameters and learnt how important an operating point is. The stability of this operating point for the transistor being used in the circuit for amplification (BJT or FET), is of higher consideration.

The operating of the active device used is adjusted to be in the linear portion of its characteristics. This point is shifted due to temperature variations and hence the stability is affected.

Variation in temperature

The tank circuit in the oscillator circuit, contains various frequency determining components such as resistors, capacitors and inductors. All of their parameters are temperature dependent. Due to the change in temperature, their values get affected. This brings the change in frequency of the oscillator circuit.
Due to power supply

The variations in the supplied power will also affect the frequency. The power supply variations lead to the variations in $V_{cc}$. This will affect the frequency of the oscillations produced.

In order to avoid this, the regulated power supply system is implemented. This is in short called as RPS.

Change in output load

The variations in output resistance or output load also affects the frequency of the oscillator. When a load is connected, the effective resistance of the tank circuit is changed. As a result, the Q-factor of LC tuned circuit is changed. This results a change in output frequency of oscillator.

Changes in inter-element capacitances

Inter-element capacitances are the capacitances that develop in PN junction materials such as diodes and transistors. These are developed due to the charge present in them during their operation.

The inter element capacitors undergo change due to various reasons as temperature, voltage etc. This problem can be solved by connecting swamping capacitor across offending inter-element capacitor.

Value of Q

The value of $Q$ (Quality factor) must be high in oscillators. The value of $Q$ in tuned oscillators determine the selectivity. As this $Q$ is directly proportional to the frequency stability of a tuned circuit, the value of $Q$ should be maintained high.

Frequency stability can be mathematically represented as,

$$Sw=d\theta/dw$$

Where $d\theta$ is the phase shift introduced for a small frequency change in nominal frequency $f_r$. The circuit giving the larger value of $(d\theta/dw)$ has more stable oscillatory frequency.
UNIT-III
LARGE SIGNAL AMPLIFIERS

In practice, any amplifier consists of few stages of amplification. If we consider audio amplification, it has several stages of amplification, depending upon our requirement.

Power Amplifier

After the audio signal is converted into electrical signal, it has several voltage amplifications done, after which the power amplification of the amplified signal is done just before the loud speaker stage. This is clearly shown in the below figure.

![Power Amplifier Diagram](image)

While the voltage amplifier raises the voltage level of the signal, the power amplifier raises the power level of the signal. Besides raising the power level, it can also be said that a power amplifier is a device which converts DC power to AC power and whose action is controlled by the input signal.

The DC power is distributed according to the relation, DC

\[ \text{DC power input} = \text{AC power output} + \text{losses} \]

Power Transistor

For such Power amplification, a normal transistor would not do. A transistor that is manufactured to suit the purpose of power amplification is called as a **Power transistor**.

A Power transistor differs from the other transistors, in the following factors.

- It is larger in size, in order to handle large powers.
- The collector region of the transistor is made large and a heat sink is placed at the collector-base junction in order to minimize heat generated.
- The emitter and base regions of a power transistor are heavily doped.
- Due to the low input resistance, it requires low input power.

Hence there is a lot of difference in voltage amplification and power amplification. So, let us now try to get into the details to understand the differences between a voltage amplifier and a power amplifier.

**Difference between Voltage and Power Amplifiers:**

Let us try to differentiate between voltage and power amplifier.

Voltage Amplifier

The function of a voltage amplifier is to raise the voltage level of the signal. A voltage
amplifier is designed to achieve maximum voltage amplification.

The voltage gain of an amplifier is given by

\[ Av = \beta \left( \frac{R_c}{R_{in}} \right) \]

The characteristics of a voltage amplifier are as follows –

- The base of the transistor should be thin and hence the value of \( \beta \) should be greater than 100.
- The resistance of the input resistor \( R_{in} \) should be low when compared to collector load \( R_c \).
- The collector load \( R_c \) should be relatively high. To permit high collector load, the voltage amplifiers are always operated at low collector current.
- The voltage amplifiers are used for small signal voltages.

**Power Amplifier**

The function of a power amplifier is to raise the power level of input signal. It is required to deliver a large amount of power and has to handle large current.

The characteristics of a power amplifier are as follows –

- The base of transistor is made thick to handle large currents. The value of \( \beta \) being (\( \beta > 100 \)) high.
- The size of the transistor is made larger, in order to dissipate more heat, which is produced during transistor operation.
- Transformer coupling is used for impedance matching.
- Collector resistance is made low.

The comparison between voltage and power amplifiers is given below in a tabular form.

<table>
<thead>
<tr>
<th>S.No</th>
<th>Particular</th>
<th>Voltage Amplifier</th>
<th>Power Amplifier</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( \beta )</td>
<td>High (&gt;100)</td>
<td>Low (5 to 20)</td>
</tr>
<tr>
<td>2</td>
<td>( R_c )</td>
<td>High (4-10 K( \Omega ))</td>
<td>Low (5 to 20 ( \Omega ))</td>
</tr>
<tr>
<td>3</td>
<td>Coupling</td>
<td>Usually R-C coupling</td>
<td>Invariably transformer coupling</td>
</tr>
<tr>
<td>4</td>
<td>Input voltage</td>
<td>Low (a few mV)</td>
<td>High (2-4 V)</td>
</tr>
<tr>
<td>5</td>
<td>Collector current</td>
<td>Low (( \approx 1 ) mA)</td>
<td>High (&gt; 100 mA)</td>
</tr>
<tr>
<td>6</td>
<td>Power output</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>7</td>
<td>Output impedance</td>
<td>High (( \approx 12 ) K( \Omega ))</td>
<td>Low (200 ( \Omega ))</td>
</tr>
</tbody>
</table>

The Power amplifiers amplify the power level of the signal. This amplification is done in the last stage in audio applications. The applications related to radio frequencies employ radio power amplifiers. But the **operating point** of a transistor plays a very important role in determining the efficiency of the amplifier. The **main classification** is done based on this mode of operation.
The classification is done based on their frequencies and also based on their mode of operation.

**Classification Based on Frequencies**

Power amplifiers are divided into two categories, based on the frequencies they handle. They are as follows.

- **Audio Power Amplifiers** – The audio power amplifiers raise the power level of signals that have audio frequency range (20 Hz to 20 KHz). They are also known as *small signal power amplifiers*.

- **Radio Power Amplifiers** – Radio Power Amplifiers or tuned power amplifiers raise the power level of signals that have radio frequency range (3 KHz to 300 GHz). They are also known as *large signal power amplifiers*.

**Classification Based on Mode of Operation**

On the basis of the mode of operation, i.e., the portion of the input cycle during which collector current flows, the power amplifiers may be classified as follows.

- **Class A Power amplifier** – When the collector current flows at all times during the full cycle of signal, the power amplifier is known as *class A power amplifier*.

- **Class B Power amplifier** – When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as *class B power amplifier*.

- **Class C Power amplifier** – When the collector current flows for less than half cycle of the input signal, the power amplifier is known as *class C power amplifier*.

There forms another amplifier called Class AB amplifier, if we combine the class A and class B amplifiers so as to utilize the advantages of both. Before going into the details of these amplifiers, let us have a look at the important terms that have to be considered to determine the efficiency of an amplifier.

**Terms Considering Performance**

The primary objective of a power amplifier is to obtain maximum output power. In order to
achieve this, the important factors to be considered are collector efficiency, power dissipation capability and distortion. Let us go through them in detail.

**Collector Efficiency**

This explains how well an amplifier converts DC power to AC power. When the DC supply is given by the battery but no AC signal input is given, the collector output at such a condition is observed as **collector efficiency**.

The collector efficiency is defined as

\[ \eta = \frac{\text{average a.c power output}}{\text{average d.c power input to transistor}} \]

The main aim of a power amplifier is to obtain maximum collector efficiency. Hence the higher the value of collector efficiency, the efficient the amplifier will be.

**Power Dissipation Capacity**

Every transistor gets heated up during its operation. As a power transistor handles large currents, it gets more heated up. This heat increases the temperature of the transistor, which alters the operating point of the transistor. So, in order to maintain the operating point stability, the temperature of the transistor has to be kept in permissible limits. For this, the heat produced has to be dissipated. Such a capacity is called as **Power dissipation capability**.

**Power dissipation capability** can be defined as the ability of a power transistor to dissipate the heat developed in it. Metal cases called heat sinks are used in order to dissipate the heat produced in power transistors.

**Distortion**

A transistor is a non-linear device. When compared with the input, there occur few variations in the output. In voltage amplifiers, this problem is not pre-dominant as small currents are used. But in power amplifiers, as large currents are in use, the problem of distortion certainly arises.
**Distortion** is defined as the change of output wave shape from the input wave shape of the amplifier. An amplifier that has lesser distortion produces a better output and hence considered efficient.

We have already come across the details of transistor biasing, which is very important for the operation of a transistor as an amplifier. Hence to achieve faithful amplification, the biasing of the transistor has to be done such that the amplifier operates over the linear region.

A Class A power amplifier is one in which the output current flows for the entire cycle of the AC input supply. Hence the complete signal present at the input is amplified at the output. The following figure shows the circuit diagram for Class A Power amplifier.

![Circuit Diagram for Class A Power Amplifier](image)

From the above figure, it can be observed that the transformer is present at the collector as a load. The use of transformer permits the impedance matching, resulting in the transference of maximum power to the load e.g. loud speaker.
The operating point of this amplifier is present in the linear region. It is so selected that the current flows for the entire ac input cycle. The below figure explains the selection of operating point.

The output characteristics with operating point Q is shown in the figure above. Here \((I_c)_Q\) and \((V_{ce})_Q\) represent no signal collector current and voltage between collector and emitter respectively. When signal is applied, the Q-point shifts to \(Q_1\) and \(Q_2\). The output current increases to \((I_c)_{\text{max}}\) and decreases to \((I_c)_{\text{min}}\). Similarly, the collector-emitter voltage increases to \((V_{ce})_{\text{max}}\) and decreases to \((V_{ce})_{\text{min}}\).

D.C. Power drawn from collector battery \(V_{cc}\) is given by

\[ P_{in} = \text{voltage} \times \text{current} = V_{cc}(I_c)_Q \]

This power is used in the following two parts –

- Power dissipated in the collector load as heat is given by
  \[ P_{RC} = (current)^2 \times \text{resistance} = (I_c)^2_QR_c \]
- Power given to transistor is given by
  \[ P_{tr} = P_{in} - P_{RC} = V_{cc} -(I_c)^2_QR_c \]

When signal is applied, the power given to transistor is used in the following two parts –

- A.C. Power developed across load resistors RC which constitutes the a.c. power output.
  \[ (P_o)_{ac} = I^2 R_c = V^2 / R_c = (V_m/\sqrt{2})^2 / R_c = V_{m}^2 / 2R_c \]
  - Where \(I\) is the R.M.S. value of a.c. output current through load, \(V\) is the R.M.S. value of a.c. voltage, and \(V_m\) is the maximum value of \(V\).
  - The D.C. power dissipated by the transistor (collector region) in the form of heat, i.e., \((P_{C})_{dc}\)

We have represented the whole power flow in the following diagram.
This class A power amplifier can amplify small signals with least distortion and the output will be an exact replica of the input with increased strength.

Let us now try to draw some expressions to represent efficiencies.

Overall Efficiency
The overall efficiency of the amplifier circuit is given by

\[
\eta_{overall} = \frac{\text{a. c power delivered to the load}}{\text{total power delivered by d. c supply}} = \frac{(P_D)_{ac}}{(P_m)_{dc}}
\]

Collector Efficiency
The collector efficiency of the transistor is defined as

\[
\eta_{collector} = \frac{\text{average a. c power output}}{\text{average d. c power input to transistor}} = \frac{(P_D)_{ac}}{(P_I)_{dc}}
\]

Expression for overall efficiency

\[
(P_D)_{ac} = V_{rms} \times I_{rms}
\]

\[
= \frac{1}{\sqrt{2}} \left[ \frac{(V_{ce})_{max} - (V_{ce})_{min}}{2} \right] \times \frac{1}{\sqrt{2}} \left[ \frac{(I_C)_{max} - (I_C)_{min}}{2} \right]
\]

\[
= \frac{1}{8} [ (V_{ce})_{max} - (V_{ce})_{min} ] \times [ (I_C)_{max} - (I_C)_{min} ]
\]

Advantages of Class A Amplifiers
The advantages of Class A power amplifier are as follows –
- The current flows for complete input cycle
- It can amplify small signals
- The output is same as input
- No distortion is present

Disadvantages of Class A Amplifiers
The advantages of Class A power amplifier are as follows –
- Low power output
- Low collector efficiency

The class A power amplifier as discussed in the previous chapter, is the circuit in which the output current flows for the entire cycle of the AC input supply. We also have learnt about the
disadvantages it has such as low output power and efficiency. In order to minimize those effects, the transformer coupled class A power amplifier has been introduced.

The construction of class A power amplifier can be understood with the help of below figure. This is similar to the normal amplifier circuit but connected with a transformer in the collector load.

Here $R_1$ and $R_2$ provide potential divider arrangement. The resistor $R_e$ provides stabilization, $C_e$ is the bypass capacitor and $R_e$ to prevent a.c. voltage. The transformer used here is a step-down transformer. The high impedance primary of the transformer is connected to the high impedance collector circuit. The low impedance secondary is connected to the load (generally loud speaker).

Transformer Action:

The transformer used in the collector circuit is for impedance matching. $R_L$ is the load connected in the secondary of a transformer. $R_L'$ is the reflected load in the primary of the transformer.

The number of turns in the primary are $n_1$ and the secondary are $n_2$. Let $V_1$ and $V_2$ be the primary and secondary voltages and $I_1$ and $I_2$ be the primary and secondary currents respectively. The below figure shows the transformer clearly.
A power amplifier may be matched by taking proper turn ratio in step down transformer.

**Circuit Operation**

If the peak value of the collector current due to signal is equal to zero signal collector current, then the maximum a.c. power output is obtained. So, in order to achieve complete amplification, the operating point should lie at the center of the load line.

The operating point obviously varies when the signal is applied. The collector voltage varies in opposite phase to the collector current. The variation of collector voltage appears across the primary of the transformer.
Circuit Analysis

The power loss in the primary is assumed to be negligible, as its resistance is very small.

The input power under dc condition will be

\[(P_{in})_{dc} = (P_{in})_{ac} = V_{cc} \times (I_c)_Q\]

Under maximum capacity of class A amplifier, voltage swings from \((V_{ce})_{max}\) to zero and current from \((I_c)_{max}\) to zero.

Hence

\[V_{rms} = \frac{1}{\sqrt{2}} \left[ \frac{(V_{ce})_{max} - (V_{ce})_{min}}{2} \right] = \frac{1}{\sqrt{2}} \left[ \frac{(V_{ce})_{max}}{2} \right] = \frac{2V_{cc}}{2\sqrt{2}} = \frac{V_{cc}}{\sqrt{2}}\]

\[I_{rms} = \frac{1}{\sqrt{2}} \left[ \frac{(I_c)_{max} - (I_c)_{min}}{2} \right] = \frac{1}{\sqrt{2}} \left[ \frac{(I_c)_{max}}{2} \right] = \frac{2(I_c)_Q}{2\sqrt{2}} = \frac{(I_c)_Q}{\sqrt{2}}\]

Therefore,

\[(P_o)_{ac} = V_{rms} \times I_{rms} = \frac{V_{cc}}{\sqrt{2}} \times \frac{(I_c)_Q}{\sqrt{2}} = \frac{V_{cc} \times (I_c)_Q}{2}\]

Therefore,

Collector Efficiency = \(\frac{(P_o)_{ac}}{(P_{in})_{dc}}\)

Or,

\[(\eta)_{collector} = \frac{V_{cc} \times (I_c)_Q}{2 \times V_{cc} \times (I_c)_Q} = \frac{1}{2}\]

\[= \frac{1}{2} \times 100 = 50\%\]

The efficiency of a class A power amplifier is nearly than 30% whereas it has got improved to 50% by using the transformer coupled class A power amplifier.

Advantages

The advantages of transformer coupled class A power amplifier are as follows.
- No loss of signal power in the base or collector resistors.
- Excellent impedance matching is achieved.
- Gain is high.
- DC isolation is provided.

Disadvantages

The disadvantages of transformer coupled class A power amplifier are as follows.
- Low frequency signals are less amplified comparatively.
- Hum noise is introduced by transformers.
- Transformers are bulky and costly.
- Poor frequency response.

**Applications**

The applications of transformer coupled class A power amplifier are as follows.
- This circuit is where impedance matching is the main criterion.
- These are used as driver amplifiers and sometimes as output amplifiers.
- When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as **class B power amplifier**.

**Class B Operation**

The biasing of the transistor in class B operation is in such a way that at zero signal condition, there will be no collector current. The **operating point** is selected to be at collector cut off voltage. So, when the signal is applied, **only the positive half cycle** is amplified at the output.

The figure below shows the input and output waveforms during class B operation.

![Input and Output Waveforms](image)

When the signal is applied, the circuit is forward biased for the positive half cycle of the input and hence the collector current flows. But during the negative half cycle of the input, the circuit is reverse biased and the collector current will be absent. Hence **only the positive half cycle** is amplified at the output.

As the negative half cycle is completely absent, the signal distortion will be high. Also, when the applied signal increases, the power dissipation will be more. But when compared to class A power amplifier, the output efficiency is increased. Well, in order to minimize the disadvantages and achieve low distortion, high efficiency and high output power, the push-pull configuration is used in this class B amplifier.
Class B Push-Pull Amplifier

Though the efficiency of class B power amplifier is higher than class A, as only one half cycle of the input is used, the distortion is high. Also, the input power is not completely utilized. In order to compensate these problems, the push-pull configuration is introduced in class B amplifier.

Construction:

The circuit of a push-pull class B power amplifier consists of two identical transistors $T_1$ and $T_2$ whose bases are connected to the secondary of the center-tapped input transformer $T_{r1}$. The emitters are shorted and the collectors are given the $V_{CC}$ supply through the primary of the output transformer $T_{r2}$.

The circuit arrangement of class B push-pull amplifier, is same as that of class A push-pull amplifier except that the transistors are biased at cut off, instead of using the biasing resistors. The figure below gives the detailing of the construction of a push-pull class B power amplifier.

The circuit operation of class B push pull amplifier is detailed below.

Operation

The circuit of class B push-pull amplifier shown in the above figure clears that both the transformers are center-tapped. When no signal is applied at the input, the transistors $T_1$ and $T_2$ are in cut off condition and hence no collector currents flow. As no current is drawn from $V_{CC}$, no power is wasted.

When input signal is given, it is applied to the input transformer $T_{r1}$ which splits the signal into two signals that are $180^\circ$ out of phase with each other. These two signals are given to the two identical transistors $T_1$ and $T_2$. For the positive half cycle, the base of the transistor $T_1$ becomes positive and collector current flows. At the same time, the transistor $T_2$ has negative half cycle, which throws the transistor $T_2$ into cutoff condition and hence no collector current flows. The waveform is produced as shown in the following figure.
For the next half cycle, the transistor $T_1$ gets into cut off condition and the transistor $T_2$ gets into conduction, to contribute the output. Hence for both the cycles, each transistor conducts alternately. The output transformer $T_{r3}$ serves to join the two currents producing an almost undistorted output waveform.

**Power Efficiency of Class B Push-Pull Amplifier**

The current in each transistor is the average value of half sine loop. For half sine loop, $I_{dc}$ is given by

$$I_{dc} = \frac{(I_C)_{max}}{\pi}$$

Therefore,

$$(P_{in})_{dc} = 2 \times \left[ \frac{(I_C)_{max}}{\pi} \times V_{cc} \right]$$

Here factor 2 is introduced as there are two transistors in push-pull amplifier.

R.M.S. value of collector current = $(I_C)_{max}/\sqrt{2}$

R.M.S. value of output voltage = $V_{cc}/\sqrt{2}$

Under ideal conditions of maximum power

Therefore,

$$(P_o)_{ac} = \frac{(I_C)_{max}}{\sqrt{2}} \times \frac{V_{cc}}{\sqrt{2}} = \frac{(I_C)_{max} \times V_{cc}}{2}$$

Now overall maximum efficiency

$$\eta_{overall} = \frac{(P_o)_{ac}}{(P_{in})_{dc}}$$

$$= \frac{(I_C)_{max} \times V_{cc}}{2} \times \frac{\pi}{2(I_C)_{max} \times V_{cc}} = \frac{\pi}{4} = 0.785 = 78.5\%$$
The collector efficiency would be the same. Hence the class B push-pull amplifier improves the efficiency than the class A push-pull amplifier.

**Complementary Symmetry Push-Pull Class B Amplifier**

The push pull amplifier which was just discussed improves efficiency but the usage of center-tapped transformers makes the circuit bulky, heavy and costly. To make the circuit simple and to improve the efficiency, the transistors used can be complemented, as shown in the following circuit diagram.

The above circuit employs a NPN transistor and a PNP transistor connected in push pull configuration. When the input signal is applied, during the positive half cycle of the input signal, the NPN transistor conducts and the PNP transistor cuts off. During the negative half cycle, the NPN transistor cuts off and the PNP transistor conducts.

In this way, the NPN transistor amplifies during positive half cycle of the input, while PNP transistor amplifies during negative half cycle of the input. As the transistors are both complement to each other, yet act symmetrically while being connected in push pull configuration of class B, this circuit is termed as **Complementary symmetry push pull class B amplifier.**

**Advantages**

The advantages of Complementary symmetry push pull class B amplifier are as follows.

- As there is no need of center tapped transformers, the weight and cost are reduced.
- Equal and opposite input signal voltages are not required.

**Disadvantages**

The disadvantages of Complementary symmetry push pull class B amplifier are as follows.
- It is difficult to get a pair of transistors (NPN and PNP) that have similar characteristics.
- We require both positive and negative supply voltages.

The class A and class B amplifier so far discussed has got few limitations. Let us now try to combine these two to get a new circuit which would have all the advantages of both class A and class B amplifier without their inefficiencies. Before that, let us also go through another important problem, called as **Cross over distortion**, the output of class B encounters with.

**Cross-over Distortion:**

In the push-pull configuration, the two identical transistors get into conduction, one after the other and the output produced will be the combination of both.

When the signal changes or crosses over from one transistor to the other at the zero voltage point, it produces an amount of distortion to the output wave shape. For a transistor in order to conduct, the base emitter junction should cross 0.7v, the cut off voltage. The time taken for a transistor to get ON from OFF or to get OFF from ON state is called the **transition period**.

At the zero voltage point, the transition period of switching over the transistors from one to the other, has its effect which leads to the instances where both the transistors are OFF at a time. Such instances can be called as **Flat spot** or **Dead band** on the output wave shape.

The above figure clearly shows the cross over distortion which is prominent in the output waveform. This is the main disadvantage. This cross over distortion effect also reduces the overall peak to peak value of the output waveform which in turn reduces the maximum power output. This can be more clearly understood through the non-linear characteristic of the waveform as shown below.
It is understood that this cross-over distortion is less pronounced for large input signals, whereas it causes severe disturbance for small input signals. This cross over distortion can be eliminated if the conduction of the amplifier is more than one half cycle, so that both the transistors won’t be OFF at the same time.

This idea leads to the invention of class AB amplifier, which is the combination of both class A and class B amplifiers, as discussed below.

**Class AB Power Amplifier**

As the name implies, class AB is a combination of class A and class B type of amplifiers. As class A has the problem of low efficiency and class B has distortion problem, this class AB is emerged to eliminate these two problems, by utilizing the advantages of both the classes.

The cross over distortion is the problem that occurs when both the transistors are OFF at the same instant, during the transition period. In order to eliminate this, the condition has to be chosen for more than one half cycle. Hence, the other transistor gets into conduction, before the operating transistor switches to cut off state. This is achieved only by using class AB configuration, as shown in the following circuit diagram.
Therefore, in class AB amplifier design, each of the push-pull transistors is conducting for slightly more than the half cycle of conduction in class B, but much less than the full cycle of conduction of class A.

The conduction angle of class AB amplifier is somewhere between 180° to 360° depending upon the operating point selected. This is understood with the help of below figure.

The small bias voltage given using diodes D₁ and D₂, as shown in the above figure, helps the operating point to be above the cutoff point. Hence the output waveform of class AB results as seen in the above figure. The crossover distortion created by class B is overcome by this class AB, as well the inefficiencies of class A and B don’t affect the circuit.

So, the class AB is a good compromise between class A and class B in terms of efficiency and linearity having the efficiency reaching about 50% to 60%. The class A, B and AB amplifiers are called as linear amplifiers because the output signal amplitude and phase are linearly related to the input signal amplitude and phase.
Class C Power Amplifier

When the collector current flows for less than half cycle of the input signal, the power amplifier is known as **class C power amplifier**. The efficiency of class C amplifier is high while linearity is poor. The conduction angle for class C is less than 180°. It is generally around 90°, which means the transistor remains idle for more than half of the input signal. So, the output current will be delivered for less time compared to the application of input signal.

The following figure shows the operating point and output of a class C amplifier.

![Operating curve](image)

This kind of biasing gives a much improved efficiency of around 80% to the amplifier, but introduces heavy distortion in the output signal. Using the class C amplifier, the pulses produced at its output can be converted to complete sine wave of a particular frequency by using LC circuits in its collector circuit.

The types of amplifiers that we have discussed so far cannot work effectively at radio frequencies, even though they are good at audio frequencies. Also, the gain of these amplifiers is such that it will not vary according to the frequency of the signal, over a wide range. This allows the amplification of the signal equally well over a range of frequencies and does not permit the selection of particular desired frequency while rejecting the other frequencies.
Single Tuned Amplifier

An amplifier circuit with a single tuner section being at the collector of the amplifier circuit is called as Single tuner amplifier circuit.

Construction

A simple transistor amplifier circuit consisting of a parallel tuned circuit in its collector load, makes a single tuned amplifier circuit. The values of capacitance and inductance of the tuned circuit are selected such that its resonant frequency is equal to the frequency to be amplified.

The following circuit diagram shows a single tuned amplifier circuit.

![Circuit Diagram]

The output can be obtained from the coupling capacitor \(C_C\) as shown above or from a secondary winding placed at L.

Operation

The high frequency signal that has to be amplified is applied at the input of the amplifier. The resonant frequency of the parallel tuned circuit is made equal to the frequency of the signal applied by altering the capacitance value of the capacitor \(C\), in the tuned circuit. At this stage, the tuned circuit offers high impedance to the signal frequency, which helps to offer high output across the tuned circuit. As high impedance is offered only for the tuned frequency, all the other frequencies which get lower impedance are rejected by the tuned circuit. Hence the tuned amplifier selects and amplifies the desired frequency signal.
**Frequency Response**

The parallel resonance occurs at resonant frequency $f_r$, when the circuit has a high Q. The resonant frequency $f_r$ is given by

$$f_r = \frac{1}{\sqrt{2\pi}LC}$$

The following graph shows the frequency response of a single tuned amplifier circuit.

At resonant frequency $f_r$, the impedance of parallel tuned circuit is very high and is purely resistive. The voltage across $R_L$ is therefore maximum, when the circuit is tuned to resonant frequency. Hence the voltage gain is maximum at resonant frequency and drops off above and below it. The higher the Q, the narrower will the curve be.

**Stagger Tuning**

Tuned amplifiers have large gain, since at resonance, $Z$ is maximum. So $Av$ is maximum. To get this large $Av$ over a wide range of frequencies, stagger tuned amplifiers are employed. This is done by taking two single tuned circuits of a certain Bandwidth, and displacing or staggering their resonance peaks by an amount equal to their Bandwidth. The resultant staggered pair will have a Bandwidth, $\sqrt{2}$ times as great as that of each of individual pairs.
The circuit of stagger tuned amplifier is as shown below:

Stagger Tuned Amplifiers are used to improve the overall frequency response of tuned Amplifiers. Stagger tuned Amplifiers are usually designed so that the overall response exhibits maximal flatness around the centre frequency.

It needs a number of tuned circuit operating in union. The overall frequency response of a Stagger tuned amplifier is obtained by adding the individual response together. Since the resonant Frequencies of different tuned circuits are displaced or staggered, they are referred as Stagger Tuned Amplifier.

The main advantage of stagger tuned amplifier is increased bandwidth. Its Drawback is Reduced Selectivity and critical tuning of many tank circuits. They are used in RF amplifier stage in Radio Receivers.

The stagger tuning in this circuit is achieved by resonating the tuned circuits L1 C1, L2 C2 to slightly different Frequencies.
UNIT IV
MULTIVIBRATORS

TRANSISTOR AS A SWITCH

A transistor can be used as a switch. It has three regions of operation. When both Emitter-to-base and collector-base junctions are reverse biased, the transistor operates in the cut-off region and it acts as an open switch. When the emitter base junction is forward biased and the Collector base junction is reverse biased, it operates in the active region and acts as an amplifier. When both the emitter-base and collector-base junctions are forward biased, it operates in the saturation region and acts as a closed switch. When the transistor is switched from cut-off to saturation and from saturation to cut-off with negligible active region, the transistor is operated as a switch. When the transistor is in saturation, junction voltages are very small but the operating currents are large. When the transistor is in cut-off, the currents are zero (except small leakage current) but the junction voltages are large.

In Below Figure the transistor Q can be used to connect and disconnect the load $RL$ from the source $Vcc$. When Q is saturated it is like a closed switch from collector to emitter and when Q is cutoff it is like an open switch from collector to emitter.

![Transistor Circuit Diagram](image)

$$I_C = \frac{V_{CC} - V_{CE}}{R_L} \quad \text{and} \quad I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

Referring to the output characteristics shown in Figure (b), the region below the $IB = 0$ curve is the cut-off region. The intersection of the load line with $IB = 0$ curve is the cut-off point. At this point, the base current is zero and the collector current is negligible. The emitter diode comes out of forward bias and the normal transistor action is lost, i.e, $V_{CE}(\text{cut-off}) = Vcc$. The transistor appears like an open switch.
The intersection of the load line with the $IB = IB(sat)$ curve is called the saturation point. At this point, the base current is $IB(sat)$ and the collector current is maximum. At saturation, the collector diode comes out of cut-off and again the normal transistor action is lost, i.e. $Ic(sat) = \frac{Vcc}{RL}$. $IB(sat)$ represents the minimum base current required to bring the transistor into saturation. For $0 < IB < IB(sat)$, the transistor operates in the active region. If the base current is greater than $IB(sat)$, the collector current approximately equals $\frac{Vcc}{RL}$ and the transistor appears like a closed switch.

TRANSISTOR SWITCHING TIMES

When the transistor acts as a switch, it is either in cut-off or in saturation. To consider the behaviour of the transistor as it makes transition from one state to the other, consider the circuit shown in below figure (a) driven by the pulse waveform shown in Figure (b). The pulse waveform makes transitions between the voltage levels $V2$ and $V1$. At $V2$ the transistor is at cutoff and at $V$ the transistor is in saturation. The input waveform $v_i$ is applied between the base and the emitter through a resistor $RB$.

![Figure a) Transistor as a Switch  b) input waveform  c) the response of collector current versus time](image)

The response of the collector current $ic$ to the input waveform, together with its time relationship to the waveform is shown in Figure (c). The collector current does not immediately respond to the input signal. Instead there is a delay, and the time that elapses during this delay, together with the time required for the current to rise to 10% of its maximum (saturation) value ($Ics = \frac{Vcc}{RL}$) is called the delay time $td$. The current waveform has a nonzero rise time $tr$, which
is the rise time required for the current to rise from 10% to 90% of $I_{cs}$. The total turn-on time TON is the sum of the delay time and the rise time, i.e. $TON = td + tr$.

When the input signal returns to its initial state, the collector current again fails to respond immediately. The interval which elapses between the transition of the input waveform and the time when $I_c$ has dropped to 90% of $I_{cs}$ is called the storage time $ts$. The storage interval is followed by the fall time $tf$, which is the time required for $I_c$ to fall from 90% to 10% of $I_{cs}$. The turn-off time $t_{OFF}$ is defined as the sum of the storage and fall times, i.e. $TOFF = tr + tf$. We shall now consider the physical reasons for the existence of each of these times.

**The delay time**

There are three factors that contribute to the delay time. First there is a delay which results from the fact that, when the driving signal is applied to the transistor input, a non-zero time is required to charge up the junction capacitance so that the transistor may be brought, from cut-off to the active region. Second, even when the transistor has been brought to the point where minority carriers have begun to cross the emitter junction into the base, a nonzero time is required before these carriers can cross the base region to the collector junction and be recorded as collector current. Finally, a nonzero time is required before the collector current can rise to 10% of its maximum value. Rise time and fall time. The rise time and fall time are due to the fact that, if a base current step is used to saturate the transistor or to return it from saturation into cutoff, the collector current must traverse the active region. The collector current increases or decreases along an exponential curve. Storage time The failure of the transistor to respond to the trailing edge of the driving pulse for the time interval $ts$, results from the fact that a transistor in saturation has a saturation charge of excess minority carriers stored in the base. The transistor cannot respond until the saturation excess charge has been removed.

**MULTIVIBRATORS**

Multi means many; vibrator means oscillator. A circuit which can oscillate at a number of frequencies is called a multivibrator. Basically there are three types of multivibrators:

1. Bistable multivibrator
2. Monostable multivibrator
3. Astable multivibrator

Each of these multivibrators has two states. As the names indicate, a bistable multivibrator has got two stable states, a monostable multivibrator has got only one stable state (the other state being quasi stable) and the astable multivibrator has got no stable state (both the
states being quasi stable). The stable state of a multivibrator is the state in which the device can stay permanently. Only when a proper external triggering signal is applied, it will change its state. Quasi stable state means temporarily stable state. The device cannot stay permanently in this state. After a predetermined time, the device will automatically come out of the quasi stable state.

Multivibrators find applications in a variety of systems where square waves or timed intervals are required. For example, before the advent of low-cost integrated circuits, chains of multivibrators found use as frequency dividers. A free-running multivibrator with a frequency of one-half to one-tenth of the reference frequency would accurately lock to the reference frequency. This technique was used in early electronic organs, to keep notes of different octaves accurately in tune. Other applications included early television systems, where the various line and frame frequencies were kept synchronized by pulses included in the video signal.

**BISTABLE MULTIVIBRATOR**

A bistable multivibrator is a multivibrator which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. In a bistable multivibrator both the coupling elements are resistors (dc coupling). The bistable multivibrator is also called a multi, Eccles-Jordan circuit (after its inventors), trigger circuit, scale-of-two toggle circuit, flip-flop, and binary. There are two types of bistable multivibrators:

1. Collector coupled bistable multivibrator
2. Emitter coupled bistable multivibrator

There are two types of collector-coupled bistable multivibrators:

1. Fixed-bias bistable multivibrator
2. Self-bias bistable multivibrator

**A FIXED-BIAS BISTABLE MULTIVIBRATOR**

The Figure below shows the circuit diagram of a fixed-bias bistable multivibrator using transistors (inverters). Note, that the output of each amplifier is direct coupled to the input of the other amplifier.
In one of the stable states, transistor Q1 is ON (i.e. in saturation) and Q2 is OFF (i.e. in cut-off), and in the other stable state Qj is OFF and Q2 is ON. Even though the circuit is symmetrical, it is not possible for the circuit to remain in a stable state with both the transistors conducting (i.e. both operating in the active region) simultaneously and carrying equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents $I_1$ and $I_2$ and suppose there is a minute fluctuation in the current $I_1$—let us say it increases by a small amount—then the voltage at the collector of Q1 decreases. This will result in a decrease in voltage at the base of Q2. So Q2 conducts less and $I_2$ decreases and hence the potential at the collector of Q2 increases. This results in an increase in the base potential of Q1. So, Q1 conducts still more and $I_1$ is further increased and the potential at the collector of Q1 is further reduced, and so on. So, the current $I_1$ keeps on increasing and the current $I_2$ keeps on decreasing till Q1 goes into saturation and Q2 goes into cut-off. This action takes place because of the regenerative feedback incorporated into the circuit and will occur only if the loop gain is greater than one. A stable state of a binary is one in which the voltages and currents satisfy the Kirchhoff’s laws and are consistent with the device characteristics and in which, in addition, the condition of the loop gain being less than unity is satisfied.

The condition with respect to loop gain will certainly be satisfied, if either of the two devices is below cut-off or if either device is in saturation. But normally the circuit is designed such that in a stable state one transistor is in saturation and the other one is in cut-off, because if one transistor is biased to be in cut-off and the other one to be in active region, as the temperature changes or the devices age and the device parameters vary, the quiescent point changes and the quiescent output voltage may also change appreciably. Sometimes the drift may
be so much that the device operating in the active region may go into cut-off, and with both the devices in cut-off the circuit will be useless.

**Selection of components in the fixed-bias bistable multivibrator**

In the fixed-bias binary shown in Figure 4.1., nearly the full supply voltage \( V_{cc} \) will appear across the transistor that is OFF. Since this supply voltage \( V_{cc} \) is to be reasonably smaller than the collector breakdown voltage \( V_{ce} \). \( V_{cc} \) restricted to a maximum of a few tens of volts. Under saturation conditions the collector current \( I_c \) is maximum. Hence \( RC \) must be chosen so that this value of \( C (= V_{cc}/^\infty G) \) does not exceed the maximum permissible limit. The values of \( R_1, R_2 \) and \( V_{BB} \) must be selected such that in one state the base current is large enough to drive the transistor into saturation whereas in the second stable state the emitter junction must be below cut-off. The signal at a collector called the output swing \( V_w \) is the change in collector voltage resulting from a transistor going from one state to the other, i.e. \( V_w = V_{Ci} - I_{C2} \). If the loading caused by \( R_l \) can be neglected, then the collector voltage of the OFF transistor is \( V_{cc} \). Since the collector saturation voltage is few tenths of a volt, then the swing \( V_w = V_{cc} \), independently of \( R_C \). The component values, the supply voltages and the values of \( /CBO, h^\infty, VBE(sat), \) and \( VCE(sat) \) are sufficient for the analysis of transistor binary circuits.

**Loading**

The bistable multivibrator may be used to drive other circuits and hence at one or both the collectors there are shunting loads, which are not shown in Figure 4.1. These loads reduce the magnitude of the collector voltage \( V_{C1} \) of the OFF transistor. This will result in reduction of the output voltage swing. A reduced \( V_{C1} \) will decrease \( V_{B2} \) and it is possible that \( Q_2 \) may not be driven into saturation. Hence the flip-flop circuit components must be chosen such that under the heaviest load, which the binary drives, one-transistor remains in saturation while the other is in cut-off. Since the resistor \( R_l \) also loads the OFF transistor, to reduce loading, the value of \( R_l \) should be as large as possible compared to the value of \( R_C \). But to ensure a loop gain in excess of unity during the transition between the states, \( R^\infty \) should be selected such that For some applications, the loading varies with the operation being performed. In such cases, the extent to which a transistor is driven into saturation is variable. A constant output swing \( V\sqrt{v} = V \), and a constant base saturation current \( I_{B2} \) can be obtained by clamping the collectors to an auxiliary voltage \( V < V_{cc} \) through the diodes \( D_l \) and \( D_2 \) as indicated in Figure 4.2. As \( Q_1 \) cuts OFF, its collector voltage rises and when it reaches \( V \), the "collector catching diode" \( D_l \) conducts and clamps the output to \( V \).
Standard specifications

In the cut-off region, i.e., for the OFF state

\[ V_{BE} \text{ (cut-off)} : \leq 0 \text{ V for silicon transistor} \]
\[ \leq -0.1 \text{ V for germanium transistor} \]

In the saturation region, i.e., for the ON state

\[ V_{BE} \text{ (sat)} : 0.7 \text{ V for silicon transistor} \]
\[ 0.3 \text{ V for germanium transistor} \]
\[ V_{CE} \text{ (sat)} : 0.3 \text{ V for silicon transistor} \]
\[ 0.1 \text{ V for germanium transistor} \]

The above values hold good for n-p-n transistors. For p-n-p transistors the above values with opposite sign are to be taken.

Test for saturation

To test whether a transistor is really in saturation or not evaluate the collector current \( i_C \) and the base current \( i_B \) independently.

If \( i_B > i_B \text{ (min)} \), where \( i_B \text{ (min)} = i_C / h_{BE} \text{ (min)} \) the transistor is really in saturation.

If \( i_B \leq i_B \text{ (min)} \), the transistor is not in saturation.

Test for cut-off

To test whether a transistor is really cut-off or not, find its base-to-emitter voltage. If \( V_{BE} \) is negative for an n-p-n transistor or positive for a p-n-p transistor, the transistor is really cut-off.
MONOSTABLE MULTIVIBRATOR

Monostable Multivibrators have only one stable state (hence their name: "Mono"), and produce a single output pulse when it is triggered externally. Monostable multivibrators only return back to their first original and stable state after a period of time determined by the time constant of the RC coupled circuit.

Monostable multivibrators or "One-Shot Multivibrators" as they are also called, are used to generate a single output pulse of a specified width, either "HIGH" or "LOW" when a suitable external trigger signal or pulse T is applied. This trigger signal initiates a timing cycle which causes the output of the monostable to change its state at the start of the timing cycle and will remain in this second state, which is determined by the time constant of the timing capacitor, CT and the resistor, RT until it resets or returns itself back to its original (stable) state. It will then remain in this original stable state indefinitely until another input pulse or trigger signal is received. Then, Monostable Multivibrators have only ONE stable state and go through a full cycle in response to a single triggering input pulse.

THE COLLECTOR COUPLED MONOSTABLE MULTIVIBRATOR

The below Figure shows the circuit diagram of a collector-to-base coupled (simply called collectorcoupled) monostable multivibrator using n-p-n transistors. The collector of Q2 is coupled to the base of Qi by a resistor R1 (dc coupling) and the collector of Qt is coupled to the base of Q2 by a capacitor C (ac coupling). C1 is the commutating capacitor introduced to increase the speed of operation. The base of Qi is connected to -VBB through a resistor R2, to ensure that Q! is cut off under quiescent conditions. The base of Q2 is connected to VCC through R to ensure that Q2 is ON under quiescent conditions. In fact, R may be returned to even a small positive voltage but connecting it to VCC is advantageous. The circuit parameters are selected such that under quiescent conditions, the monostable multivibrator finds itself in its permanent stable state with Q2ON (i.e. in saturation) and Q! OFF (i.e. in cut-off)- The multivibrator may be induced to make a transition out of its stable state by the application of a negative trigger at the base of Q2 or at the collector of Qi. Since the triggering signal is applied to only one device and not to both the devices simultaneously, unsymmetrical triggering is employed. When a negative signal is applied at the base of Q2 at t ~ 0, due to regenerative action Q2 goes to OFF state and Qi goes to ON state. When Q, is ON, a current i flows through its Rc and hence its collector voltage drops suddenly by i\|RC This drop will be instantaneously
transmitted through the coupling capacitor $C$ to the base of $Q_2$. So at $t = 0^+$, the base voltage of $Q_2$ is

$$V_{BE(sat)} - I_1 R_C.$$ 

The circuit cannot remain in this state for a long time (it stays in this state only for a finite time $T$) because when $Q_t$ conducts, the coupling capacitor $C$ charges from $V_{cc}$ through the conducting transistor $Q_i$ and hence the potential at the base of $Q_2$ rises exponentially with a time constant

$$\frac{(R + R_O)C}{RC} = RC,$$

where $R_O$ is the conducting transistor output impedance including the resistance $R_c$. When it passes the cut-in voltage $V_y$ of $Q_2$ (at a time $t = T$), a regenerative action takes place turning $Q_i$ OFF and eventually returning the multivibrator to its initial stable state. The transition from the stable state to the quasi-stable state takes place at $t = 0$, and the reverse transition from the quasi-stable state to the stable state takes place at $t = T$.

The time $T$ for which the circuit is in its quasi-stable state is also referred to as the delay time, and also as the gate width, pulse width, or pulse duration. The delay time may be varied by varying the time constant $t(= RC)$.

**Expression for the gate width $T$ of a monostable multivibrator neglecting the reverse saturation current /CBO**

The below Figure (a) shows the waveform at the base of transistor $Q_2$ of the monostable multivibrator.
For \( t < 0 \), \( Q_2 \) is ON and so \( v_{B2} = V_{BE(sat)} \). At \( t = 0 \), a negative signal applied brings \( Q_2 \) to OFF state and \( Q_1 \) into saturation. A current \( I \) flows through \( R_c \) of \( Q_1 \) and hence \( v_{ci} \) drops abruptly by \( I \) volts and so \( v_{B2} \) also drops by \( I/R_C \) instantaneously. So at \( t = 0 \), \( v_{B2} = V_{BE(sat)} - I/R_C \). For \( t > 0 \), the capacitor charges with a time constant \( RC \), and hence the base voltage of \( Q_2 \) rises exponentially towards \( V_Cc \) with the same time constant. At \( t = T \), when this base voltage rises to the cut-in voltage level \( V_y \) of the transistor, \( Q_2 \) goes to ON state, and \( Q_1 \) to OFF state and the pulse ends. In the interval \( 0 < t < T \), the base voltage of \( Q_2 \), i.e. \( v_{B2} \) is given by

\[
v_{B2} = V_{CC} - (V_{CC} - \{V_{BE(sat)} - I/R_C\}) e^{-\frac{t}{\tau}}
\]

\( \text{Fig a) Voltage variation at the base of } Q_2 \text{ during the quasi-stable state} \)

But \( I/R_C = V_{CC} - V_{CE(sat)} \) (because at \( t = 0^- \), \( v_{C1} = V_{CC} \) and at \( t = 0^+ \), \( v_{C1} = V_{CE(sat)} \))

\[
\therefore v_{B2} = V_{CC} - \{V_{CC} - \{V_{BE(sat)} - (V_{CC} - V_{CE(sat)})\}\} e^{-\frac{t}{\tau}}
\]

\[
= V_{CC} - \{2V_{CC} - \{V_{BE(sat)} + V_{CE(sat)}\}\} e^{-\frac{t}{\tau}}
\]

At

\[
\therefore V_y = V_{CC} - \{2V_{CC} - \{V_{CE(sat)} + V_{BE(sat)}\}\} e^{-\frac{T}{\tau}}
\]

i.e.

\[
e^{-\frac{T}{\tau}} = \frac{2V_{CC} - \{V_{CE(sat)} + V_{BE(sat)}\}}{V_{CC} - V_y}
\]

\[\therefore \frac{T}{\tau} = \ln \left[ \frac{2 \left( V_{CC} - \frac{V_{CE(sat)} + V_{BE(sat)}}{2} \right)}{V_{CC} - V_y} \right]
\]

i.e.

\[
T = \tau \ln \left(2 + \frac{V_{CC} - \frac{V_{CE(sat)} + V_{BE(sat)}}{2}}{V_{CC} - V_y} \right)
\]
Normally for a transistor, at room temperature, the cut-in voltage is the average of the saturation junction

\[ V_y = \frac{V_{CE(sat)} + V_{BE(sat)}}{2} \]

voltages for either Ge or Si transistors, i.e.

Neglecting the second term in the expression for \( T \)

\[ T = \tau \ln 2 \]

\[ T = (R + R_o)C \ln 2 = 0.693(R + R_o)C \]

but for a transistor in saturation \( R_a \ll R \).

Gate width, \( T = 0.693RC \)

The larger the \( Vcc \) is, compared to the saturation junction voltages, the more accurate the result is. The gate width can be made very stable (almost independent of transistor characteristic supply voltages, and resistance values) if \( Q1 \) is driven into saturation during the quasi-stab state.

**Waveforms of the collector-coupled monostable multivibrator**

The waveforms at the collectors and bases of both the transistors \( Q1 \) and \( Q2 \) are shown below

(a) at the base of \( Q2 \), (b) at the collector of \( Q1 \), (c) at the collector of \( Q2 \), and (d) at the base of \( Q1 \)
ASTABLE MULTIVIBRATOR

As the name indicates an astable multivibrator is a multivibrator with no permanent stable state. Both of its states are quasi stable only. It cannot remain in any one of its states indefinitely and keeps on oscillating between its two quasi stable states the moment it is connected to the supply. It remains in each of its two quasi stable states for only a short designed interval of time and then goes to the other quasi stable state. No triggering signal is required. Both the coupling elements are capacitors (ac coupling) and hence both the states are quasi stable. It is a free running multivibrator. It generates square waves. It is used as a master oscillator.

There are two types of astable multivibrators:
1. Collector-coupled astable multivibrator
2. Emitter-coupled astable multivibrator

THE COLLECTOR-COUPLED ASTABLE MULTIVIBRATOR

The below Figure shows the circuit diagram of a collector-coupled astable multivibrator using n-p-n transistors. The collectors of both the transistors Q1 and Q2 are connected to the bases of the other transistors through the coupling capacitors C1 and C2. Since both are ac couplings, neither transistor can remain permanently at cut-off. Instead, the circuit has two quasi-stable states, and it makes periodic transitions between these states. Hence it is used as a master oscillator. No triggering signal is required for this multivibrator. The component values are selected such that, the moment it is connected to the supply, due to supply transients one
transistor will go into saturation and the other into cut-off, and also due to capacitive couplings it keeps on-oscillating between its two quasi stable states.

The waveforms at the bases and collectors for the astable multivibrator, are shown in below Figure. Let us say at \( t = 0 \), \( Q_2 \) goes to ON state and \( Q_1 \) to OFF state. So, for \( t < 0 \), \( Q_2 \) was OFF and \( Q_1 \) was ON

Hence for \( t < 0 \), \( v_{B2} \) is negative, \( v_{C2} = V_{cc} \), \( v_{B1} = V_{BE(sat)} \) and \( v_{C1} = V_{CE(sat)} \). The capacitor C2 charges from \( V_{cc} \) through \( R_2 \) and \( v_{B2} \) rises exponentially towards \( V_{cc} \). At \( t = 0 \), \( v_{B2} \) reaches the cut-in voltage \( V_y \) and \( Q_2 \) conducts. As \( Q_2 \) conducts, its collector voltage \( V_{c2} \) drops by \( \frac{1}{2} \frac{V_{cc}}{R_c} \). This drop in \( v_{c2} \) is transmitted to the base of \( Q_1 \) through the coupling capacitor C2

Fig: waveforms at the bases and collectors of a collector-coupled astable multivibrator
and hence \(v_B1\) also falls by \(\frac{2}{3}\) - Qi goes to OFF state. So, \(v_B1 = V_{BE\text{(sat)}} - \frac{I_2 R_C}{2}\), and its collector voltage \(v_{CL}\) rises towards \(V_{CC}\). This rise in \(v_{CL}\) is coupled through the coupling capacitor \(C_2\) to the base of \(Q_2\), causing an overshoot \(\delta\) in \(v_B2\) and the abrupt rise by the same amount \(\delta\) in \(v_{CL}\) as shown in Figure 4.51(c). Now since \(Q_2\) is ON, \(C_1\) charges from \(V_{CC}\) through \(R_{LT}\) and hence \(v_B1\) rises exponentially. At \(t = 7''\), when \(v_B1\) rises to \(V_Y\), Qi conducts and due to regenerative action Qi goes into saturation and \(Q_2\) to cut-off. Now, for \(t > T_1\), the coupling capacitor \(C_2\) charges from \(V_{CC}\) through \(R_2\) and at \(t = 7'' + 7''\), when \(v_B2\) rises to the cut-in voltage \(V_r\), \(Q_2\) conducts and due to regenerative feedback \(Q_2\) goes to ON state and \(Q_1\) to OFF state. The cycle of events repeats and the circuit keeps on oscillating between its two quasi-stable states. Hence the output is a square wave. It is called a square wave generator or square wave oscillator or relaxation oscillator. It is a free running oscillator.

**Expression for the frequency of oscillation of an astable multivibrator**

Consider the waveform at the base of \(Q_1\), shown in Figure 4.54(d). At \(t = 0\),

\[
v_{B1} = V_{BE\text{(sat)}} - I_2 R_C
\]

But

\[
I_2 R_C = V_{CC} - V_{CE\text{(sat)}}
\]

\[\therefore\] At \(t = 0\),

\[
v_{B1} = V_{BE\text{(sat)}} - V_{CC} + V_{CE\text{(sat)}}
\]

For \(0 < t < T_1\), \(v_{B1}\) rises exponentially towards \(V_{CC}\) given by the equation,

\[
v_p = v_f - (v_f - v_i)e^{-\frac{t}{\tau_1}}
\]

\[\therefore v_{B1} = V_{CC} - [V_{CC} - (V_{BE\text{(sat)}} - V_{CC} + V_{CE\text{(sat)}})]e^{-\frac{t}{\tau_1}}, \text{ where } \tau_1 = R_1 C_1\]

At \(t = T_1\), when \(v_{B1}\) rises to \(V_Y\), \(Q_1\) conducts

\[\therefore V_Y = V_{CC} - [2V_{CC} - (V_{BE\text{(sat)}} + V_{CE\text{(sat)}})]e^{-\frac{T_1}{R_1 C_1}}\]

or

\[e^{\frac{T_1}{R_1 C_1}} = \frac{2 \left[ V_{CC} - \frac{V_{BE\text{(sat)}} + V_{CE\text{(sat)}}}{2} \right]}{V_{CC} - V_Y}\]

\[T_1 = R_1 C_1 \ln \left(2 \frac{V_{CC} - \frac{V_{CE\text{(sat)}} + V_{BE\text{(sat)}}}{2}}{V_{CC} - V_Y} \right)
\]

\[T_1 = R_1 C_1 \ln 2 + R_1 C_1 \ln \left(\frac{V_{CC} - \frac{V_{CE\text{(sat)}} + V_{BE\text{(sat)}}}{2}}{V_{CC} - V_Y} \right)
\]

At room temperature for a transistor,

\[V_Y = \frac{V_{CE\text{(sat)}} + V_{BE\text{(sat)}}}{2}\]

\[\therefore T_1 = R_1 C_1 \ln 2 = 0.693 R_1 C_1\]
On similar lines considering the waveform of above Figure, we can show that the time $T_2$ for which $Q_2$ is OFF and $Q_1$ is ON is given by

$T = 2 \times 0.693RC = 1.386RC$  

and  

$f = \frac{1}{1.386RC}$

The frequency of oscillation may be varied over the range from cycles to mega cycles by varying $RC$. It is also possible to vary the frequency electrically by connecting $R_1$ and $R_2$ to an auxiliary voltage source $V$ (the collector supply remains $+VCC$) and then varying this voltage $V$.

THE EMITTER-COUPLED ASTABLE MULTIVIBRATOR

An emitter-coupled astable multivibrator may be obtained by using three power supplies or a single power supply. The below Figure (a) shows the circuit diagram of a free-running emitter coupled multivibrator using n-p-n transistors. Figure 4.64 shows its waveforms. Three power supplies are indicated for the sake of simplifying the analysis. A more practical circuit using a single supply is indicated in below Figure (b). Let us assume that the circuit operates in such a manner that $Q_1$ switches between cut-off and saturation and $Q_2$ switches between cut-off and its active region.

![Fig a) Astable Emitter-Coupled Multivibrator](image-url)
Fig b) Emitter Coupled multivibrator

The waveforms at the base and collector are as shown below:

Fig waveforms of the emitter-coupled astable multivibrator
Advantages
1. It is inherently self-starting.
2. The collector of Q2 where the output is taken may be loaded heavily even capacitively.
3. The output is free of recovery transients.
4. Because it has an isolated input at the base of Q1, synchronization is convenient.
5. Frequency adjustment is convenient because only one capacitor is used.

Disadvantages
1. This circuit is more difficult to adjust for proper operating conditions.
2. This circuit cannot be operated with T1 and T2 widely different.
3. This circuit uses more components than does the collector-coupled circuit.

Schmitt trigger
In electronics, Schmitt trigger is a circuit with positive feedback and a loop gain >1. The circuit is named "trigger" because the output retains its value until the input changes sufficiently to trigger a change: in the non-inverting configuration, when the input is higher than a certain chosen threshold, the output is high; when the input is below a different (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. This dual threshold action is called hysteresis and implies that the Schmitt trigger possesses memory and can act as a bi-stable circuit (latch). There is a close relation between the two kinds of circuits: a Schmitt trigger can be converted into a latch and a latch can be converted into a Schmitt trigger. Schmitt trigger devices are typically used in open-loop controller configurations for noise immunity and closed loop negative feedback configurations to implement bi-stable regulators, triangle/square wave generators, etc.

The original Schmitt trigger is based on the dynamic threshold idea that is implemented by a voltage divider with a switchable upper leg (the collector resistors Rc1 and Rc2) and a steady lower leg (RE). T1 acts as a comparator with a differential input (T1 base-emitter junction) consisting of an inverting (T1 base) and a non-inverting (T1 emitter) inputs. The input voltage is applied to the inverting input; the output voltage of the voltage divider is applied to the non-inverting input thus determining its threshold. The comparator output drives the second common collector stage T2 (an emitter follower) through the voltage follower R1-R2. The emitter-coupled transistors T1 and T2 actually compose an electronic double throw switch that switches over the
upper legs of the voltage divider and changes the threshold in a different (to the input voltage) direction.

This configuration can be considered as a differential amplifier with series positive feedback between its non-inverting input (T2 base) and output (T1 collector) that forces the transition process. There is also a smaller negative feedback introduced by the emitter resistor RE. To make the positive feedback dominate over the negative one and to obtain a hysteresis, the proportion between the two collector resistors is chosen \( Rc1 > Rc2 \). Thus less current flows through and less voltage drop is across RE when T1 is switched on than in the case when T2 is switched on. As a result, the circuit has two different thresholds in regard to ground.

![Schmitt trigger implemented by two emitter-coupled transistor stages](image)

**Operation:**

**Initial state.** For NPN transistors as shown, imagine the input voltage is below the shared emitter voltage (high threshold for concreteness) so that T1 base-emitter junction is backward-biased and T1 does not conduct. T2 base voltage is determined by the mentioned divider so that T2 is conducting and the trigger output is in the low state. The two resistors \( Rc2 \) and \( RE \) form
another voltage divider that determines the high threshold. Neglecting VBE, the high threshold value is approximately

\[ V_{HT} = \frac{R_E}{R_E + R_{c2}} V_+ . \]

The output voltage is low but well above the ground. It is approximately equal to the high threshold and may not be low enough to be a logical zero for next digital circuits. This may require additional shifting circuit following the trigger circuit.

**Crossing up the high threshold:**

When the input voltage (T1 base voltage) rises slightly above the voltage across the emitter resistor RE (the high threshold), T1 begins conducting. Its collector voltage goes down and T2 begins going cut-off, because the voltage divider now provides lower T2 base voltage. The common emitter voltage follows this change and goes down thus making T1 conduct more. The current begins steering from the right leg of the circuit to the left one. Although T1 is more conducting, it passes less current through RE (since Rc1 > Rc2); the emitter voltage continues dropping and the effective T1 base-emitter voltage continuously increases. This avalanche-like process continues until T1 becomes completely turned on (saturated) and T2 turned off. The trigger is transitioned to the high state and the output (T2 collector) voltage is close to V+. Now, the two resistors Rc1 and RE form a voltage divider that determines the low threshold. Its value is approximately

\[ V_{LT} = \frac{R_E}{R_E + R_{c1}} V_+ . \]

**Crossing down the low threshold:**

With the trigger now in the high state, if the input voltage lowers enough (below the low threshold), T1 begins cutting-off. Its collector current reduces; as a result, the shared emitter voltage lowers slightly and T1 collector voltage rises significantly. R1-R2 voltage divider conveys this change to T2 base voltage and it begins conducting. The voltage across RE rises, further reducing the T1 base-emitter potential in the same avalanche-like manner, and T1 ceases to conduct. T2 becomes completely turned-on (saturated) and the output voltage becomes low again.
UNIT –V
TIME BASE GENERATORS

TIME BASE GENERATORS

A time-base generator is an electronic circuit which generates an output voltage or current waveform, a portion of which varies linearly with time. Ideally the output waveform should be a ramp. Time-base generators may be voltage time-base generators or current time-base generators. A voltage time-base generator is one that provides an output voltage waveform, a portion of which exhibits a linear variation with respect to time. A current time-base generator is one that provides an output current waveform, a portion of which exhibits a linear variation with respect to time. There are many important applications of time-base generators, such as in CROs, television and radar displays, in precise time measurements, and in time modulation. The most important application of a time-base generator is in CROs. To display the variation with respect to time of an arbitrary waveform on the screen of an oscilloscope it is required to apply to one set of deflecting plates a voltage which varies linearly with time. Since this waveform is used to sweep the electron beam horizontally across the screen it is called the sweep voltage and the time-base generators are called the sweep circuits.

GENERAL FEATURES OF A TIME-BASE SIGNAL

Figure (a) shows the typical waveform of a time-base voltage. As seen the voltage starting from some initial value increases linearly with time to a maximum value after which it returns again to its initial value. The time during which the output increases is called the sweep time and the time taken by the signal to return to its initial value is called the restoration time, the return time, or the flyback time. In most cases the shape of the waveform during restoration time and the restoration time itself are not of much consequence. However, in some cases a restoration time which is very small compared with the sweep time is required. If the restoration time is almost zero and the next linear voltage is initiated the moment the present one is terminated then a saw-tooth waveform shown in (b) is generated. The waveforms of the type shown in Figures (a) and (b) are generally called sweep waveforms even when they are used in applications not involving the deflection of an electron beam. In fact, precisely linear sweep signals are difficult to generate by time-base generators and moreover nominally linear sweep signals may be distorted when transmitted through a coupling.
Fig 5.1 (a) General sweep voltage and (b) saw-tooth voltage waveforms.

The deviation from linearity is expressed in three most important ways:
1. The slope or sweep speed error, $es$
2. The displacement error, $ed$
3. The transmission error, $et$

**The slope or sweep-speed error, $es$**

An important requirement of a sweep is that it must increase linearly with time, i.e. the rate of change of sweep voltage with time be constant. This deviation from linearity is defined as

$$
es = \frac{\text{difference in slope at beginning and end of sweep}}{\text{initial value of slope}}$$

$$= \frac{\frac{dv_0}{dt}|_{t=0} - \frac{dv_0}{dt}|_{t=T_s}}{\frac{dv_0}{dt}|_{t=0}}$$

**The displacement error, $ed$**

Another important criterion of linearity is the maximum difference between the actual sweep voltage and the linear sweep which passes through the beginning and end points of the actual sweep. The displacement error $ed$ is defined as

$$ed = \frac{\text{maximum difference between the actual sweep voltage and the linear sweep which passes through the beginning and end points of the actual sweep}}{\text{amplitude of the sweep at the end of the sweep time}}$$

$$= \frac{(v_s - v'_s)_{\text{max}}}{V_s}$$
As shown in Figure (a), $v_s$ is the actual sweep and $v_s'$ is the linear sweep.

**The transmission error, $e_t$**

When a ramp signal is transmitted through a high-pass circuit, the output falls away from the input as shown in Figure (b). This deviation is expressed as transmission error $e_t$, defined as the difference between the input and the output divided by the input at the end of the sweep

$$e_t = \frac{V_s' - V_s}{V_s'}$$

where as shown in Figure (b), $V_s'$ is the input and $V_s$ is the output at the end of the sweep, i.e. at $t = T_s$

Fig.5.2 (a) Sweep for displacement error and (b) sweep for transmission error

If the deviation from linearity is small so that the sweep voltage may be approximated by the sum of linear and quadratic terms in $t$, then the above three errors are related as:

$$e_d = \frac{e_s}{8} = \frac{e_t}{4}$$

$$e_s = 2e_t = 8e_d$$

which implies that the sweep speed error is the more dominant one and the displacement error is the least severe one.

**METHODS OF GENERATING A TIME-BASE WAVEFORM**

In time-base circuits, sweep linearity is achieved by one of the following methods.

1. **Exponential charging.** In this method a capacitor is charged from a supply voltage through a resistor to a voltage which is small compared with the supply voltage.
2. **Constant current charging.** In this method a capacitor is charged linearly from a constant current source. Since the charging current is constant the voltage across the capacitor increases linearly.

3. **The Miller circuit.** In this method an operational integrator is used to convert an input step voltage into a ramp waveform.

4. **The Phantastron circuit.** In this method a pulse input is converted into a ramp. This is a version of the Miller circuit.

5. **The bootstrap circuit.** In this method a capacitor is charged linearly by a constant current which is obtained by maintaining a constant voltage across a fixed resistor in series with the capacitor.

6. **Compensating networks.** In this method a compensating circuit is introduced to improve the linearity of the basic Miller and bootstrap time-base generators.

7. **An inductor circuit.** In this method an RLC series circuit is used. Since an inductor does not allow the current passing through it to change instantaneously, the current through the capacitor more or less remains constant and hence a more linear sweep is obtained.

**MILLER AND BOOTSTRAP TIME-BASE GENERATORS—BASIC PRINCIPLES**

The linearity of the time-base waveforms may be improved by using circuits involving feedback. Figure 5.3 (a) shows the basic exponential sweep circuit in which S opens to form the sweep. A linear sweep cannot be obtained from this circuit because as the capacitor charges, the charging current decreases and hence the rate at which the capacitor charges, i.e. the slope of the output waveform decreases. A perfectly linear output can be obtained if the initial charging current \( I = \frac{V}{IR} \) is maintained constant. This can be done by introducing an auxiliary variable generator \( v \) whose generated voltage \( v \) is always equal to and opposite to the voltage across the capacitor as shown in Figure 5.3 (b). Two methods of simulating the fictitious generator are discussed below.

![Diagram](image)

Fig. 5.3 (a) The current decreases exponentially with time and (b) the current remains constant
In the circuit of Figure 5.3 (b) suppose the point Z is grounded as in below Figure 5.4 (a). A linear sweep will appear between the point Y and ground and will increase in the negative direction. Let us now replace the fictitious (imaginary) generator by an amplifier with output terminals YZ and input terminals XZ as shown in below Figure 5.4 (b). Since we have assumed that the generated voltage is always equal and opposite to the voltage across the capacitor,

![Figure 5.4](image)

Fig. 5.4 (a) Figure 5.3(b) with Z grounded and (b) Miller integrator circuit.

the voltage between X and Z is equal to zero. Hence the point X acts as a virtual ground. Now for the amplifier, the input is zero volts and the output is a finite negative value. This can be achieved by using an operational integrator with a gain of infinity. This is normally referred to as the Miller integrator circuit or the Miller sweep. Suppose that the point Y in Figure 5.3(b) is grounded and the output is taken at Z. A linear sweep will appear between Z and ground and will increase in the positive direction. Let us now replace the fictitious generator by an amplifier with input terminals XY and output terminals ZY as shown in Figure 5.5. Since we have assumed that the generated voltage v at any instant is equal to the voltage across the capacitor vc, then v0 must be equal to v, and the amplifier voltage gain must be equal to unity. The circuit of Figure 5.5 is referred to as the Bootstrap sweep circuit.

![Figure 5.5](image)

Fig. 5.5 Bootstrap sweep circuit.
The Miller sweep

The Miller integrating circuit of Figure 5.4 (b) is redrawn in Figure 5.6(a). A switch S at the closing of which the sweep starts is included. The basic amplifier has been replaced at the input side by its input resistance and on the output side by its Thevenin’s equivalent. $R_0$ is the output resistance of the amplifier and $A$ its open circuit voltage gain. Figure 5.6 (b) is obtained by replacing $V$, $R$ and $t_f$, on the input side by a voltage source $V$ in series with a resistance $R’$ where

$$V’ = V \frac{R_i}{R_i + R} = \frac{V}{1 + \frac{R}{R_i}} \quad \text{and} \quad R’ = R || R_i = \frac{R R_i}{R + R_i}$$

Neglecting the output resistance in the circuit of Figure 5.6 (b), if the switch is closed at $t = 0$ and if the initial voltage across the capacitor is zero, then $v_0 (t = 0^+) = 0$, because at $t = 0^-$, $V; \sim 0$ and since the voltage across the capacitor cannot change instantaneously.

At $t = 0^+$, $v_i - A v_i = 0$ \quad or \quad $v_i = A v_i = v_o = 0$

This indicates that the sweep starts from zero.

At $t = \infty$, the capacitor acts as an open-circuit for dc. So no current flows and therefore

$$v_i = V’ \quad \text{and} \quad v_o = A V’$$

Fig. 5.6 (a) A Miller integrator with switch $S$, input resistance $R_f$ and Thevenin’s equivalent on the output side and (b) Figure 5.6(a) with input replaced by Thevenin’s equivalent.
This indicates that the output is exponential and the sweep is negative-going since $A$ is a negative number.

\[
\text{Slope error, } e_s = \frac{V_s}{V}
\]

where $V_s$ is the sweep amplitude and $V$ is the peak-to-peak value of the output

\[
e_{s\text{ (miller)}} = \frac{V_s}{|A| V'} = \frac{V_s}{|A|} \cdot \frac{R_i + R}{VR_i} = \frac{V_s}{V} \cdot \frac{1 + \frac{R}{R_i}}{|A|}
\]

The deviation from linearity is $\frac{R}{R_i}$ times that of an $RC$ circuit charging directly from a source $V$. If $R_0$ is taken into account, the final value attained by $v_0$ remains as before, $AV = -|A|V$.

The initial value however is slightly different.

To find $v_0$ at $t = 0^+$, writing the KVL around the mesh in Figure 5.13(b), assuming zero voltage across the capacitor, we have

\[
V' - R'i - R_oi - Av_i = 0
\]

\[
v_i = V' - R'i
\]

From the above equations, we find

\[
v_i(t = 0^+) = \Delta v_i = v_o(t = 0^+) = \Delta v_o = \frac{\frac{R_0}{R'}}{1 - A + \frac{R_0}{R'}} V'
\]

\[
v_i(t = 0^+) = \frac{R_0V'}{R'\cdot|A|}
\]

Therefore, if $R_0$ is taken into account, $v_0(t = 0^+)$ is a small positive value and still it will be a negative going sweep with the same terminal value. Thus the negative-going ramp is preceded by a small positive jump. Usually this jump is/small compared to the excursion $AV'$, Hence, improvement in linearity because of the increase in total excursion is negligible.
The bootstrap sweep

Figure 5.7 shows the bootstrap circuit of Figure 5.5. The switch S at the opening of which the sweep starts is in parallel with the capacitor C. Here, $R_i$, is the input resistance, $A$ is the open-circuit voltage gain, and $R_0$ is the output resistance of the amplifier.

![Bootstrap circuit of Figure 5.5 with switch S which opens at $t = 0$, input resistance $R_f$, and Thevenin's equivalent of the amplifier on the output side.](image)

At $t = 0^-$, the switch was closed and so $v_t = 0$. Since the voltage across the capacitor cannot change instantaneously, at $t = 0^+$ also, $v_L = 0$ and hence $A v_L = 0$, and the circuit shown in Figure 5.8 results.

$$t = 0^+, \quad v_o = -V \frac{R_0}{R + R_0}$$

The output has the same value at $t = 0$ and hence there is no jump in the output voltage at $t = 0$.

![Equivalent circuit of Figure 5.7 at $t = 0$.](image)

At $t = \infty$, the capacitor acts as an open-circuit and the equivalent circuit shown in Figure 5.9 results.
Writing KVL in the circuit of Figure 5.9,

\[ V - iR - iR_i + AV_i - iR_o = 0 \]

i.e.,

\[ i = \frac{V}{R + R_o + R_i (1 - A)} \]

\[ v_o(t = \infty) = \frac{V(AR_i - R_o)}{R + R_o + R_i (1 - A)} \]

Since \( A \ll 1 \), and if \( R_0 \) is neglected, we get

\[ v_o(t = \infty) = \frac{V}{(1 - A) + \frac{R}{R_i}} \]

\[ v_o(t = \infty) - v_o(t = 0) = \frac{V}{(1 - A) + \frac{R}{R_i}} \]

\[ e_s(bootstrap) = \frac{\text{Sweep amplitude}}{\text{Total excursion of output}} = \frac{V_s}{V \sqrt{\left(1 - A + \frac{R}{R_i}\right)}} = \frac{V_s}{V} \left(1 - A + \frac{R}{R_i}\right) \]

This shows that the slope error is \( [1 - A + (R/R_i)] \) times the slope error that would result if the capacitor is charged directly from \( V \) through a resistor.
Comparing the expressions for the slope error of Miller and bootstrap circuits, we can see that it is more important to keep \( R/R_j \) small in the bootstrap circuit than in the Miller circuit. Therefore, the Miller integrator has some advantage over the bootstrap circuit in that in the Miller circuit higher input impedance is less important.

**THE TRANSISTOR MILLER TIME-BASE GENERATOR**

Figure 5.10 shows the circuit diagram of a transistor Miller time-base generator. It consists of a three stage amplifier. To have better linearity, it is essential that a high input impedance amplifier be used for the Miller integrator circuit. Hence the first stage of the amplifier of Figure 5.10 is an emitter follower. The second stage is a common-emitter amplifier and it provides the necessary voltage amplification. The third stage (output stage) is also an emitter follower for two reasons. First, because of its low output impedance \( R_0 \) it can drive a load such as the horizontal amplifier. Second, because of its high input impedance it does not load the collector circuit of the second stage and hence the gain of the second stage can be very high. The capacitor \( C \) placed between the base of Qi and the emitter of Q3 is the timing capacitor. The sweep speed is changed from range to range by switching \( R \) and \( C \) and may be varied continuously by varying VBB.

![Fig.5.10 A Transistorized Miller Time-Base Generator](image)

Under quiescent condition, the output of the Schmitt gate is at its lower level. So transistor Q4 is ON. The emitter current of Q4 flows through \( R_1 \) and hence the emitter is at a negative potential. Therefore the diode D conducts. The current through \( R \) flows through the diode D and the transistor Q4. The capacitor \( C \) is bypassed and hence is prevented from charging.
When a triggering signal is applied, the output of the Schmitt gate goes to its higher level. So the base voltage of Q4 rises and hence the transistor Q4 goes OFF. A current flows now from 10 V source through \( R_I \). The positive voltage at the emitter of Q4 now makes the diode D reverse biased. At this time the upper terminal of \( C \) is connected to the collector of Q4 which is in cut-off. The capacitor gets charged from VBB and hence a run down sweep output is obtained at the emitter of Q3. At the end of the sweep, the capacitor \( C \) discharges rapidly through D and Q4. Considering the effect of the capacitance \( C_1 \), the slope or sweep speed error is given by

\[
e_s = \frac{V_s}{V} \left( 1 - A + \frac{R}{R_I} + \frac{C}{C_1} \right)
\]

**THE TRANSISTOR BOOTSTRAP TIME-BASE GENERATOR**

Figure 5.11 shows a transistor bootstrap time-base generator. The input to transistor Q1 is the gating waveform from a monostable multivibrator (it could be a repetitive waveform like a square wave). Figure 5.12(a) shows the base voltage of Q1. Figure 5.12(b) shows the collector current waveform of Q1 and Figure 5.12(c) shows the output voltage waveform at the emitter of Q2.

![Fig.5.11 A Voltage Time Base Generator](image)

Under quiescent conditions, i.e. before the application of the gating waveform at \( t = 0 \), Q1 is in saturation because it gets enough base drive from YCC through \(^B\)-So the voltage across the
capacitor which is also the voltage at the collector of Q1 and the base of Q2 is $V_{CE} \text{(sat)}$. Since Q2 is conducting and acting as an emitter follower, the voltage at the emitter of Q2 which is also the output voltage is less than this base voltage by $V_{BE2}$, i.e.,

$$v_o = V_{CE} \text{(sat)} - V_{BE2}$$

is a small negative voltage (a few tenths of a volt negative). If we neglect this small voltage as well as the small drop across the diode D, then the voltage across $C_1$ as well as across $R$ is $V_{cc}$- Hence the current $i_\text{r}$ through $R$ is $V_{cc}/R$. Since the quiescent output voltage at the emitter of Q2 is close to zero, the emitter current of Q2.

Hence the base current of Q2 is

$$i_{B2} = \frac{V_{EE}}{h_{FE} R E}$$

$$i_{R} = i_{C1} + i_{B2}$$

Since the base current of Q2, i.e. $i_{B2}$ is very small compared with the collector current $i_{C1}$ of Q1

$$i_{C1} \approx i_{R} \approx \frac{V_{CC}}{R}$$

For Q1 to be really in saturation under quiescent condition, its base current ($i_B = V_{CC}/R_B$) to be at least equal to $\frac{V_{CC}}{h_{FE}}$, so that

$$\frac{V_{CC}}{R_B} > \frac{V_{CC}}{h_{FE} R} \quad \text{i.e.} \quad R_B < h_{FE} R$$

Fig.5.12 Voltage time-base generator of Figure 5.11: (a) the base voltage of Q1 (b) the collector current of Q1, and (c) the output voltage at the emitter of Q2.
CURRENT TIME-BASE GENERATORS

We have mentioned earlier that a linear current time-base generator is one that provides an output current waveform a portion of which exhibits a linear variation with respect to time. This linearly varying current waveform can be generated by applying a linearly varying voltage waveform generated by a voltage time-base generator, across a resistor. Alternatively, a linearly varying current waveform can be generated by applying a constant voltage across an inductor. Linearly varying currents are required for magnetic deflection applications.

A SIMPLE CURRENT SWEEP

Figure 5.13 shows a simple transistor current sweep circuit. Here the transistor is used as a switch and the inductor $L$ in series with the transistor is bridged across the supply voltage. $Rd$ represents the sum of the diode forward resistance and the damping resistance. The gating waveform shown in Figure 5.26(b) applied to the base of the transistor is in two levels. These levels are selected such that when the input, is at the lower level the transistor is cut-off and when it is at the upper level the transistor is in saturation. For $t < 0$, the input to the base is at its lower level (negative). So the transistor is cut-off. Hence no currents flow in the transistor and $i_L = 0$ and $V_{CE} = V_{cc}$. At $t = 0$, the gate signal goes to its upper level (positive). So the transistor conducts and goes into saturation. Hence the collector voltage falls to $V_{CE(sat)}$ and the entire supply voltage $V_{cc}$ is applied across the inductor. So the current through the inductor

$$i_L = \frac{1}{L} \int V_{cc} \, dt = \frac{V_{cc}t}{L}$$

![Fig.5.13 simple transistor current sweep circuit](image-url)
Increases linearly with time. This continues till \( t = T_g \), at which time the gating signal comes to its lower level and so the transistor will be cut-off. During the sweep interval \( T_s \) (i.e. from \( t = 0 \) to \( t = T_g \)), the diode D is reverse biased and hence it does not conduct. At \( t \approx T_s \), when the transistor is cut-off and no current flows through it, since the current through the inductor cannot change instantaneously it flows through the diode and the diode conducts. Hence there will be a voltage drop of \( ILR_d \) across the resistance \( R_d \). So at \( t = T_g \), the potential at the collector terminal rises abruptly to \( V_{cc} + \frac{f_i d}{L} \) i.e. there is a voltage spike at the collector at \( t = T_g \). The duration of the spike depends on the inductance of \( Z \) - but the amplitude of the spike does not. For \( t > T_g \), the inductor current decays exponentially to zero with a time constant \( T_LR_d \). So the voltage at the collector also decays exponentially and settles at \( V_{cc} \) under steady-state conditions. The inductance \( L \) normally represents a physical yoke and its resistance \( R_L \) may not be negligible. If \( R_{CS} \) represents the collector saturation resistance of the transistor, the current increases in accordance with the equation

\[
i_L = \frac{V_{cc}}{R_L + R_{CS}} \left( 1 - e^{-(R_L + R_{CS})/IL} \right)
\]

\[
i_L \approx \frac{V_{cc}}{R_L + R_{CS}} \left( 1 - \left( 1 - \frac{(R_L + R_{CS})t}{L} \right) + \frac{1}{2} \left( \frac{(R_L + R_{CS})t}{L} \right)^2 \right) + ... \]

\[
i_L = \frac{V_{cc}t}{L} \left( 1 - \frac{1}{2} \frac{(R_L + R_{CS})t}{L} \right)
\]

If the current increases linearly to a maximum value \( I_L \), the slope error is given by

\[
e_s = \frac{I_L}{V_{cc}} = \frac{(R_L + R_{CS})I_L}{V_{cc}}
\]
A TRANSISTOR CURRENT TIME-BASE GENERATOR

Figure 5.14 shows the circuit diagram of a transistor current time-base generator. Transistor Q1 is a switch which serves the function of S. Transistor Q1 gets enough base drive from VCC1 through KB a °d hence is in saturation under quiescent conditions. At t = 0, when the gating signal is applied it turns off Q1 and a trapezoidal voltage waveform appears at the base of Q2. Transistors Q2 and Q3 are connected as darlington pair to increase the input impedance so that the trapezoidal waveform source is not loaded. Such loading would cause nonlinearity in the ramp part of the trapezoid. The emitter resistor RE introduces negative current feedback into the output stage and thereby improves the linearity with which the collector current responds to the base voltage. For best linearity it is necessary to make the emitter resistance as large as possible. RE is selected so that the voltage developed across it will be comparable to the supply voltage.

![Fig.5.14 A Transistor Current Sweep Circuit](image)

![Fig.5.14 a) Circuit Diagram b) waveform of iL c) waveform of VCE](image)