

LINEAR & DIGITAL IC

LECTURE NOTES

B.TECH (III-ECE I-SEM)

(2021-22)

Prepared by

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Malla Reddy College of Engineering & Technology

(Autonomous Institution – UGC, Govt. of India)

Recognized under 2(f) and 12 (B) of UGC ACT 1956

(Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2015 Certified)

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MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY
III Year B.Tech ECE-I Sem

L	T/P/D	C
3	-/-/-	3

(R18A0409) LINEAR & DIGITAL IC

COURSE OBJECTIVES:

The main objectives of the course are:

- 1) To introduce the basic building blocks of linear integrated circuits.
- 2) To teach the linear and non-linear applications of operational amplifiers.
- 3) To introduce the theory and applications of analog multipliers and PLL.
- 4) To teach the theory of ADC and DAC.
- 5) To introduce the concepts of waveform generation and introduce some special function Ics.

UNIT – I:

Operational Amplifier: Ideal and Practical Op-Amp, Op-Amp Characteristics, DC and AC Characteristics, Features of 741 Op-Amp, Modes of Operation – Inverting, Non-Inverting, Differential, Instrumentation Amplifier, AC Amplifier, Differentiators and Integrators, Comparators, Schmitt Trigger, Introduction to Voltage Regulators, Features of 723 Regulator, Three Terminal Voltage Regulators.

UNIT – II:

Op-Amp, IC-555 & IC 565 Applications: Introduction to Active Filters, Characteristics of Band pass, Band reject and All Pass Filters, Analysis of 1st order LPF & HPF Butterworth Filters, waveform Generators – Triangular, Sawtooth, Square wave, IC555 Timer – Functional Diagram, Monostable and Astable Operations, Applications, IC565 PLL – Block Schematic, Description of Individual Blocks, Applications.

UNIT – III:

Data Converters: Introduction, Basic DAC techniques, Different types of DACs-Weighted resistor DAC, R-2R ladder DAC, Inverted R-2R DAC, Different Types of ADCs – Parallel Comparator Type ADC, Counter Type ADC, Successive Approximation ADC and Dual Slope ADC, DAC and ADC Specifications.

UNIT – IV:

Digital Integrated Circuits: Classification of Integrated Circuits, Comparison of Various Logic Families, CMOS Transmission Gate, IC interfacing. TTL Driving CMOS & CMOS Driving TTL, Combinational Logic Ics – Specifications and Applications of TTL-74XX & CMOS 40XX Series Ics – Code Converters, Decoders, Demultiplexers, LED & LCD Decoders with Drivers, Encoders, Priority Encoders, Multiplexers, Demultiplexers, Priority Generators/Checkers, Parallel Binary Adder/ Subtractor, Magnitude Comparators.

UNIT – V:

Sequential Logic IC's and Memories: Familiarity with commonly available 74XX & CMOS 40XX Series Ics – All Types of Flip-flops, Synchronous Counters, Decade Counters, Shift Registers. Memories – ROM Architecture, Types of ROMs & Applications, RAM Architecture, Static & Dynamic RAMs.

TEXT BOOKS:

1. Linear Integrated Circuits – D. Roy Chowdhury, New Age International (p) Ltd, 2nd Edition, 2003.
2. Op-Amps & Linear ICs - Ramakanth A. Gayakwad, PHI, 2003.
3. Digital fundamentals – Floyd and Jain, Pearson Education, 8th Edition, 2005.

REFERENCE BOOKS:

1. Op Amps & Linear Integrated circuits-Concepts and Applications James M.Fiore, Cengage Learning/Jaico, 2009.
2. Operational Amplifiers with linear integrated circuits by K.Lalkishore-Pearson, 2009.
3. Linear integrated circuits and applications-Salivahana, TMH.
4. Modern digital electronics-RPJain-4/e-TMH, 2010.
5. Digital design principles and practices-John.F.Wakerly 3/e, 2005.
6. Operational amplifiers with linear integrated circuits, 4/e William D.Stanley, Pearson education India, 2009.

COURSE OUTCOMES:

After completion of this course, the students will have:

- A thorough understanding of operational amplifiers with linear integrated circuits.
- Understanding of the different families of digital integrated circuits and their characteristics.
- Also students will be able to design circuits using operational amplifiers for various applications.

UNIT-I OPERATIONAL AMPLIFIER

INTRODUCTION:

An operational amplifier is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output stage. An operational amplifier is available as a single integrated circuit package. The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication, and integration. Thus the name operational amplifier stems from its original use for these mathematical operations and is abbreviated to op-amp. With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications, such as ac and dc signal amplification, active filters, oscillators, comparators, regulators, and others.

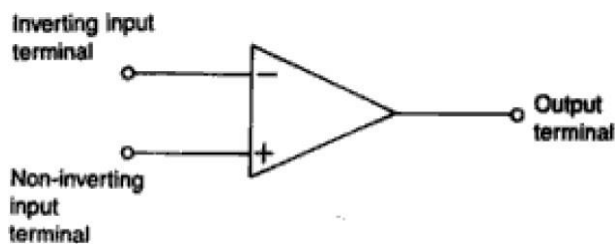


Fig. 2.1 Op-amp circuit symbol

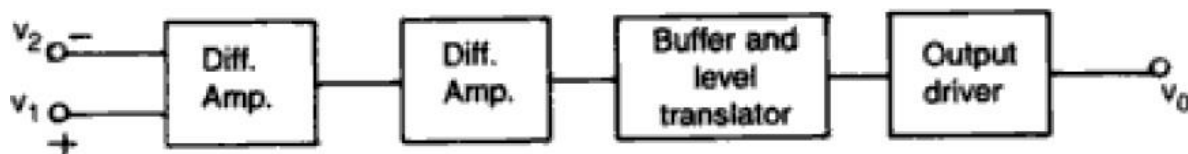


Fig. 2.10 Block schematic of an op-amp

It has two input terminals and one output terminal. The terminal with a (-) sign is called inverting input terminal and the terminal with (+) sign is called the non-inverting input terminal.

HISTORY

- First developed by **John R. Ragazzine** in **1947** with vacuum tube.
- In 1960 at **FAIRCHILD SEMICONDUCTOR CORPORATION**, **Robert J. Widlar** fabricated op amp with the help of IC fabrication technology.
- In 1968 FAIRCHILD introduces the **op-amp** that was to become the industry standard.

Op-amp pin diagram

There are 8 pins in a common Op-Amp, like the 741 which is used in many instructional courses.

- Pin 1: Offset null
- Pin 2: Inverting input terminal
- Pin 3: Non-inverting input terminal
- Pin 4: $-V_{CC}$ (negative voltage supply)
- Pin 5: Offset null
- Pin 6: Output voltage
- Pin 7: $+V_{CC}$ (positive voltage supply)
- Pin 8: No Connection

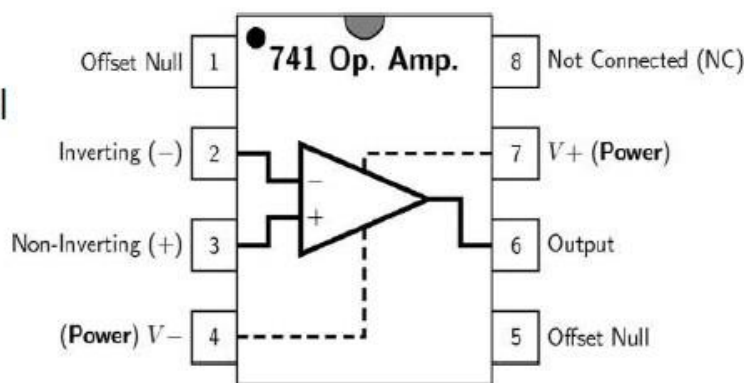


Figure : Pin connection, LM741.

Important terms and equation

a = gain of amplifiers.

V_d = difference between the voltage.

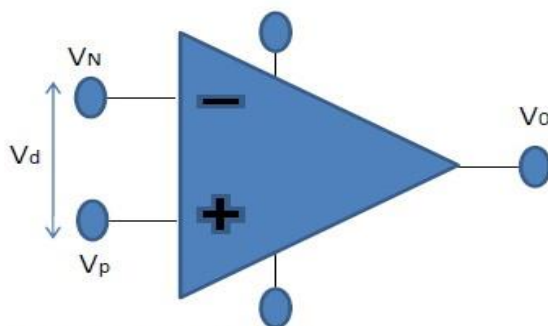
V_o = gain of voltage.

The equation :

$$V_o = a (V_P - V_N)$$

Electrical parameter :

1. **Input bias current (I_b):** average of current that flows into the inverting and non-inverting input terminal of op-amp.
2. **I/p and o/p impedance:** It is the resistance offered by the inputs and the output terminals to varying voltages. The quantity is expressed in Ohms.
3. **Open Loop Gain:** It is the overall voltage gain or the amplification.
4. **Input offset voltage :** It is a voltage that must be applied between the two terminal of an op-amp to null the o/p.
5. **Input offset current (I_i):** The algebraic different between the current in to the inverting and Non-inverting terminal.



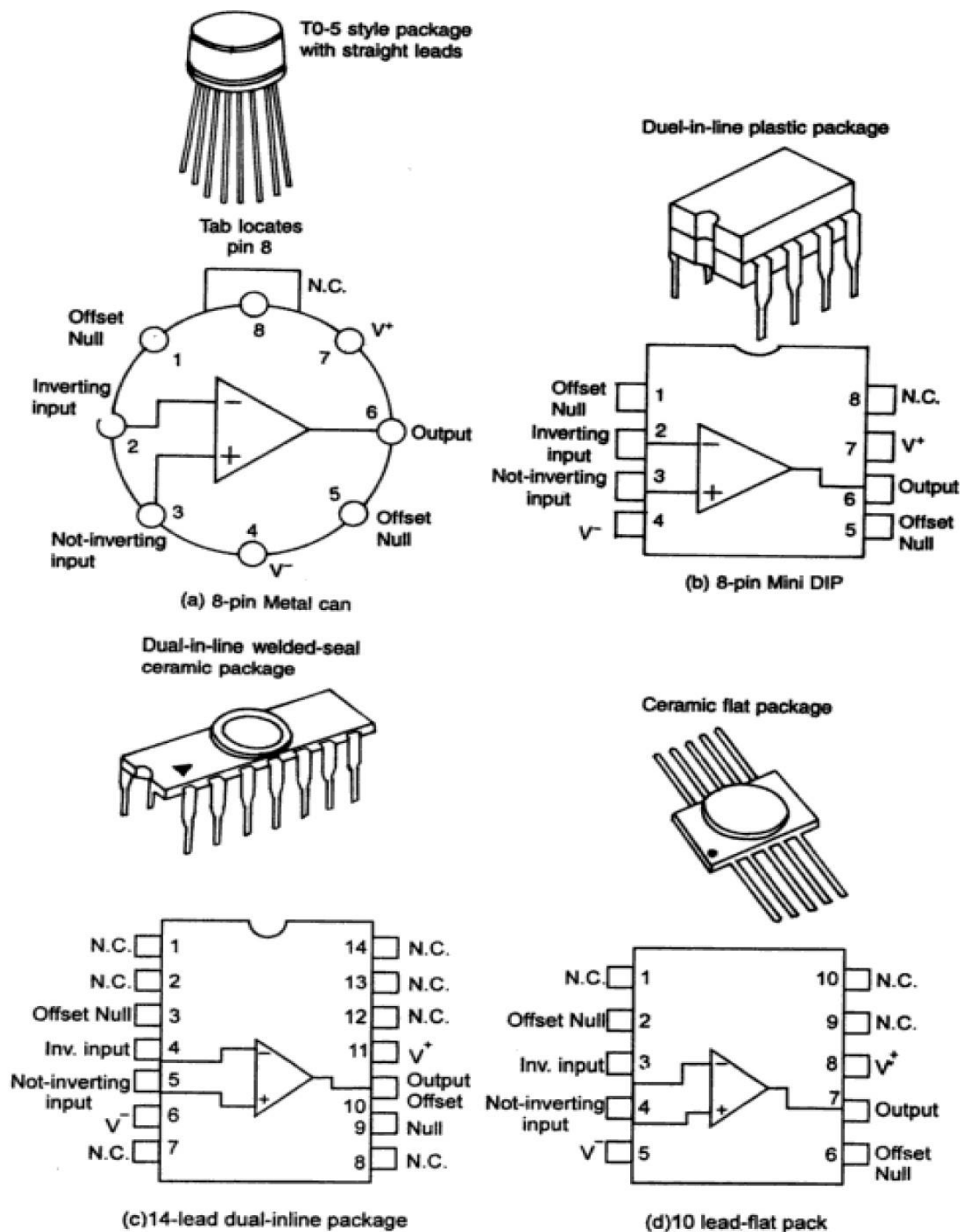


Fig. 2.2 (a, b, c, d) Various IC packages of $\mu A 741$ op-amp along with connection diagrams (top view)

Manufacturer's Designation for Linear ICs

Each manufacturer uses a specific code and assigns a specific type number to the ICs produced. For example, 741 an internally compensated op-amp originally manufactured by Fairchild is sold as $\mu A741$. Here μA represents the identifying initials used by Fairchild. The codes used by some of the well-known manufacturers of linear ICs are:

(1) Fairchild	$\mu A, \mu AF$
(2) National Semiconductor	LM, LH, LF, TBA
(3) Motorola	MC, MFC
(4) RCA	CA, CD
(5) Texas Instruments	SN
(6) Signetics	N/S, NE/SE
(7) Burr-Brown	BB

Some linear ICs are available in different classes such as A, C, E, S and SC. For example 741, 741 A, 741 C, 741 E, 741 S and 741 SC are different versions of the same op-amp. The main difference of these op-amps are:

741	Military grade op-amp (Operating temperature range -55° to 125°C)	
741C	Commercial grade op-amp (Operating temperate range 0° to $70^{\circ}/75^{\circ}\text{C}$)	
741A	Improved version of 741	} Better electrical specifications
741E	Improved version of 741 C	
741S	Military grade op-amp with higher slew-rate	
741SC	Commercial grade op-amp with higher slew-rate	

CLASSIFICATION OF ICs:

Integrated circuits offer a wide range of applications and could be broadly classified as:

Digital ICs

Linear ICs

Based upon the above requirements, two distinctly different IC technology namely, Monolithic technology and Hybrid technology have been developed.

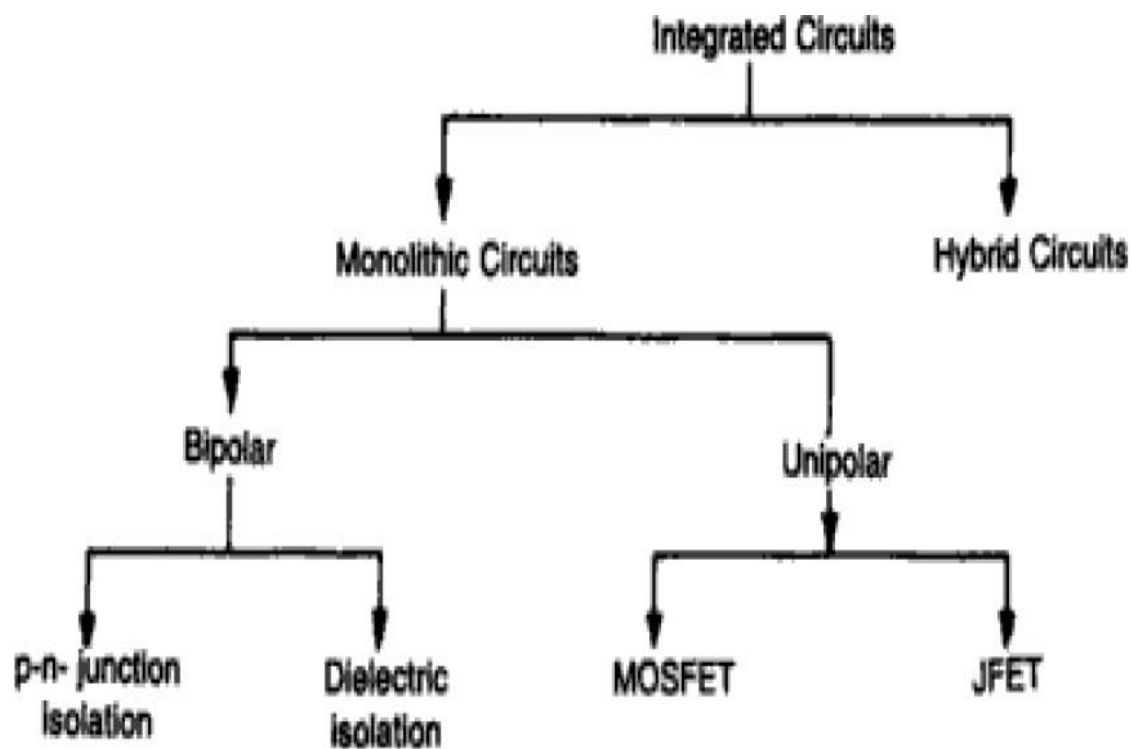


Fig. 1.1 Classification of ICs

TRANSISTOR AND SCALING TECHNOLOGY:

Invention of transistor (Ge)		1947
Development of Silicon transistor		1955–1959
Silicon Planar Technology	Junction transistor diode	1959
First ICs, Small Scale Integration (SSI)	3 to 30 gates/chip approx. or 100 transistors/chip (Logic gates, Flip-flops)	1960–65
Medium Scale Integration (MSI)	30 to 300 gates/chip or 100 to 1000 transistors/chip (Counters, Multiplexers, Adders)	1965–1970
Large Scale Integration (LSI)	300 to 3000 gates/chip or 1000–20,000 transistors/chip (8 bit microprocessors, ROM, RAM)	1970–1980
Very Large Scale Integration (VLSI)	More than 3000 gates/chip or 20,000–1,00,00,00 transistors/chip (16 and 32 bit microprocessors)	1980–1990
Ultra Large Scale Integration (ULSI)	$10^6 - 10^7$ transistors/chip (Special processors, Virtual reality) machines, Smart sensors	1990–2000
Giant-Scale Integration (GSI)	$> 10^7$ transistors/chip	

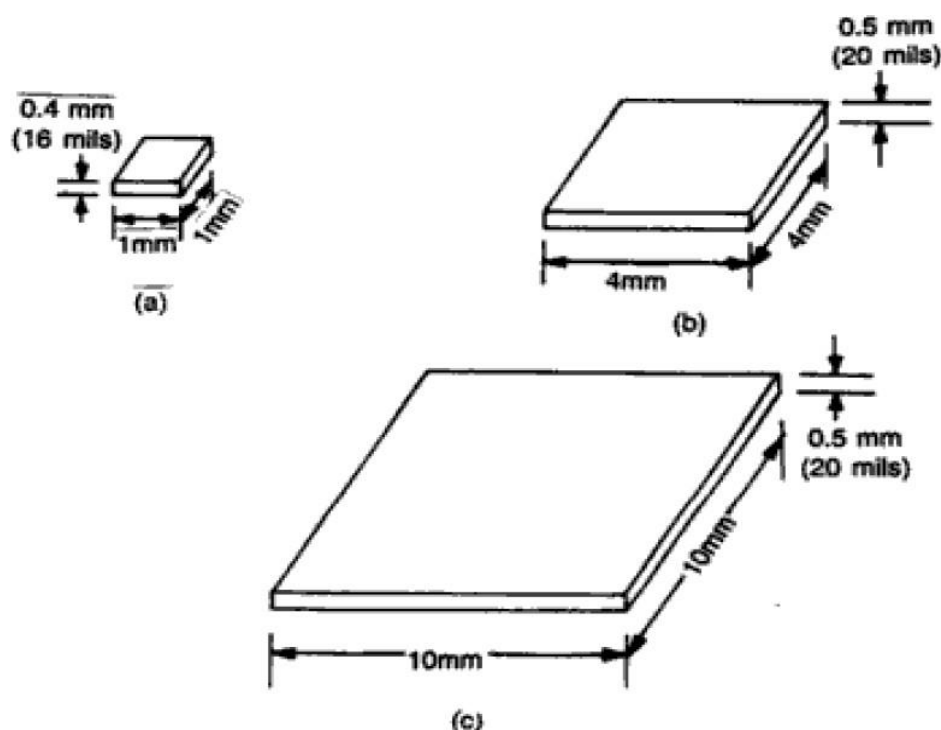


Fig. 1.2 Integrated circuit chips (a) SSI chip (b) MSI chip (c) LSI or VLSI chip

The basic processes used to fabricate ICs using silicon planar technology can be categorised as follows:

1. Silicon wafer (substrate) preparation
2. Epitaxial growth
3. Oxidation
4. Photolithography
5. Diffusion
6. Ion implantation
7. Isolation technique
8. Metallization
9. Assembly processing and packaging

IDEAL OPERATIONAL AMPLIFIER:

This op-amp is said to be ideal if it has the following characteristics.

Open loop voltage gain,	A_{OL}	=	∞
Input impedance,	R_i	=	∞
Output impedance	R_o	=	0
Bandwidth	BW	=	∞

Zero offset, i.e. $v_o = 0$ when $v_1 = v_2 = 0$.

- (i) an ideal op-amp draws no current at both the input terminals i.e., $i_1 = i_2 = 0$. Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.
- (ii) Since gain is ∞ , the voltage between the inverting and non-inverting terminals, i.e., differential input voltage $v_d = (v_1 - v_2)$ is essentially zero for finite output voltage v_o .
- (iii) The output voltage v_o is independent of the current drawn from the output as $R_o = 0$. The output thus can drive an infinite number of other devices.

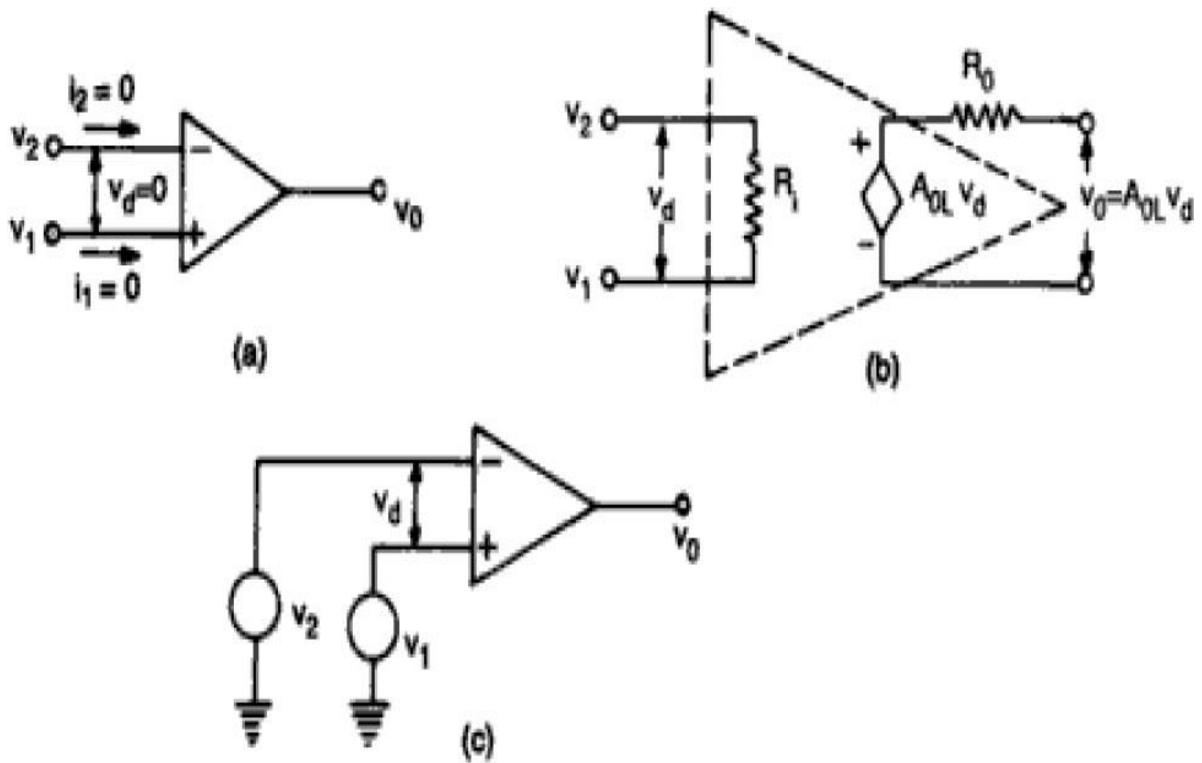
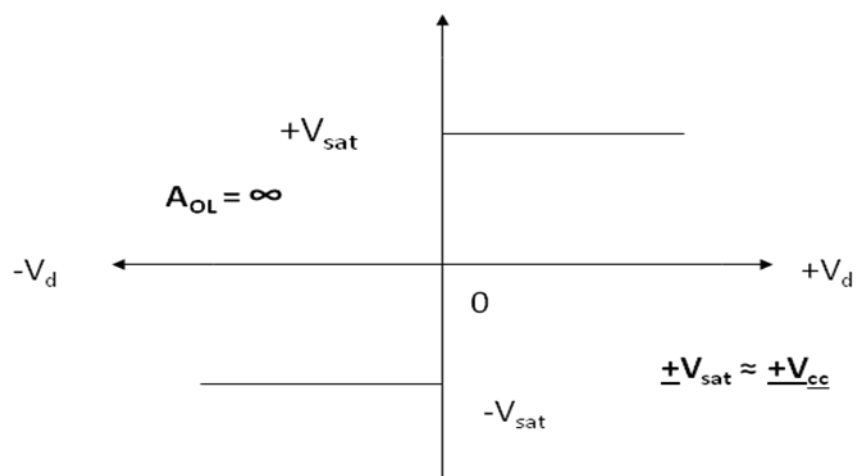


Fig. 2.4 (a) Ideal op-amp (b) Equivalent circuit of an op-amp (c) Open loop circuit

Ideal Voltage transfer curve:



Practical Op-Amplifier:

- The open loop gain of practical Op – Amp is around 7000.
- Practical Op – Amp has non zero offset voltage. That is, the zero output is obtained for the non – zero differential input voltage only.
- The bandwidth of practical Op – Amp is very small value. This can be increased to desired value by applying an adequate negative feedback to the Op – Amp.
- The output impedance is in the order of hundreds. This can be minimized by applying an adequate negative feedback to the Op – Amp.
- The input impedance is in the order of Mega Ohms only. (Whereas the ideal Op – Amp has infinite input impedance).

Differences between Ideal and practical Op-Amps:

Characteristics	Ideal Op-amp	PracticalOp-amp
Voltage gain	Infinite	High
Input resistance	Infinite	High
Output resistance	Zero	Low
Outputvoltagewheninputvoltageis zero	Zero	Low
Band width	Infinite	High
CMRR	Infinite	High
Slew Rate	Infinite	High

Op-amp Characteristics:

Earlier we have used an ideal op-amp, and assumed that the op-amp responds equally well to both ac and dc input voltages. However, a practical op-amp does not behave this way. A practical op-amp has some dc voltage at the output even with both the inputs grounded.

DC Characteristics:

- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift

AC Characteristics

- Slew rate
- Frequency response

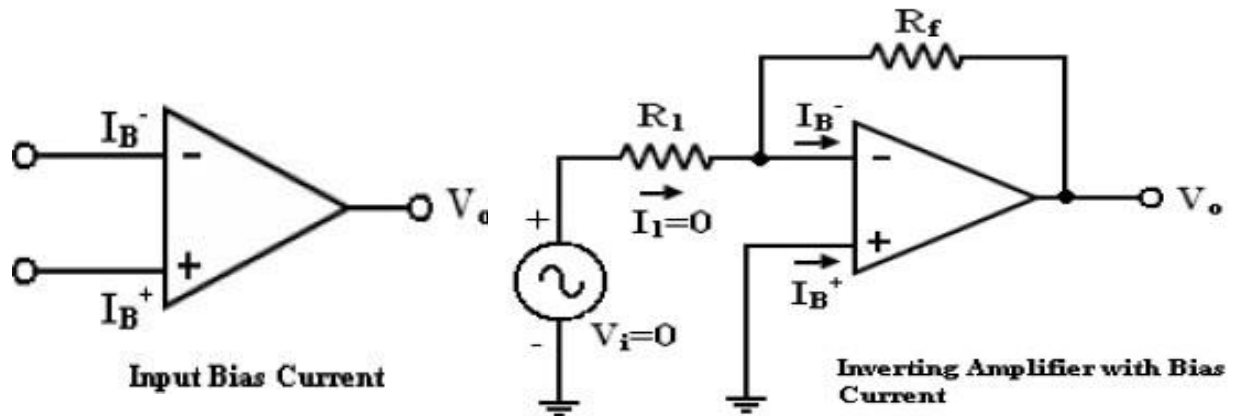
DC Characteristics:

The non ideal dc characteristics that add error components to the dc output voltage are,

1. Input Bias Current
2. Input Offset Current
3. Input offset Voltage
4. Total Output offset Voltage
5. Thermal drift

1. Input Bias Current:

- In an ideal op-amp, we assumed that no current is drawn from the input terminals.
- The base currents entering into the inverting and non-inverting terminals (I_B^+ & I_B^- respectively).



(a) Input bias currents (b) inverting amplifier with bias currents

Input bias current I_B is the average value of the base currents entering into terminal of an op-amp.

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

The effect can be compensated with compensation resistor R_{comp} . By KVL, $V_o = V_2 - V_1$. By selecting proper value of R_{comp} , V_2 can be cancelled with V_1 and the $V_o = 0$. The value of R_{comp} is derived as,

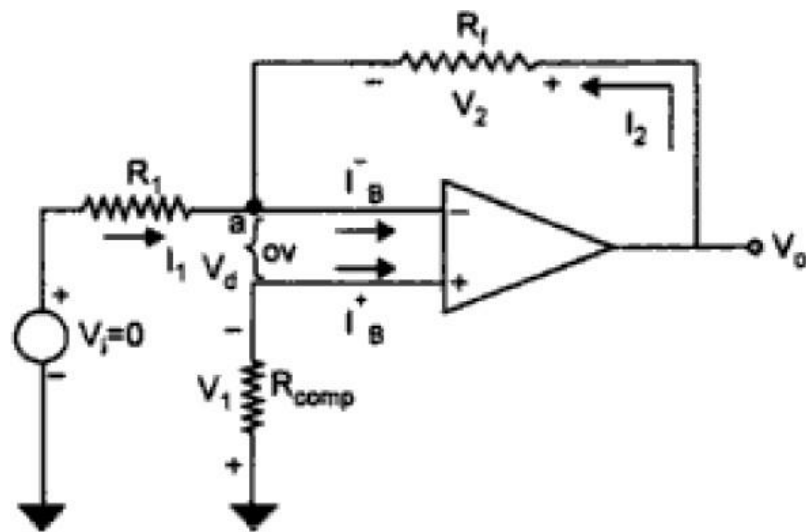


Fig.(C) Bias current compensation

$$V_1 = I_B^+ R_{comp}$$

$$I_B^+ = V_1 / R_{comp}$$

The node 'a' is at voltage $(-V_1)$. Because the voltage at the non-inverting input terminal is $(-V_1)$.

So with $V_i = 0$ we get,

$$I_1 = V_1 / R_1$$

$$I_2 = V_2 / R_f$$

For compensation, V_o should equal to zero ($V_o = 0, V_i = 0$).

$$I_2 = V_1 / R_f$$

KVL at node a gives

$$I_B^- = I_2 + I_1 = \frac{V_1}{R_f} + \frac{V_1}{R_1} = V_1 \frac{(R_1 + R_f)}{R_1 R_f}$$

Assume $I_B^- = I_B^+$, we get

$$V_1 \frac{(R_1 + R_f)}{R_1 R_f} = \frac{V_1}{R_{comp}}$$

$$R_{comp} = \frac{(R_1 + R_f)}{R_1 R_f} = R_1 \parallel R_f$$

that is, to compensate for bias currents, the compensating resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting input terminal.

2. Input offset current:

Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. Since the input transistors cannot be made identical, there will always be some small difference between I_B^+ and I_B^- . This difference is called the offset current I_{os} and can be written as

$$|I_{os}| = I_B^+ - I_B^- \quad (3.10)$$

Offset current I_{os} for BJT op-amp is 200 nA and that for FET op-amp is 10 pA. Even with bias current compensation, offset current will produce an output voltage when the input voltage V_i is zero.

$$V_1 = I_B^- R_{comp}$$

$$I_1 = V_1/R_1$$

From Fig.C on above,

KCL at node a gives,

$$I_2 = (I_B^- - I_1) = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1} \right)$$

$$\begin{aligned} \text{Again, } V_o &= I_2 R_f - V_1 = I_2 R_f - I_B^+ R_{comp} \\ &= \left(I_B^- - I_B^+ \frac{R_{comp}}{R_1} \right) R_f - I_B^+ R_{comp} \end{aligned}$$

$$\text{Hence, } V_o = R_f [I_B^- - I_B^+] = R_f I_{os}$$

So even with bias current compensation and with feedback resistor of 1M, a BJT op-amp has an output offset voltage

$$V_o = 1\text{M } \Omega \times 200\text{nA}$$

$$V_o = 200\text{mV with } V_i = 0$$

with a zero input voltage. It can be seen from Eq. that the effect of offset current can be minimized by keeping feedback resistance small. Unfortunately, to obtain high input impedance, R_1 must be kept large. With R_1 large, the feedback resistor R_f must also be high so as to obtain reasonable gain.

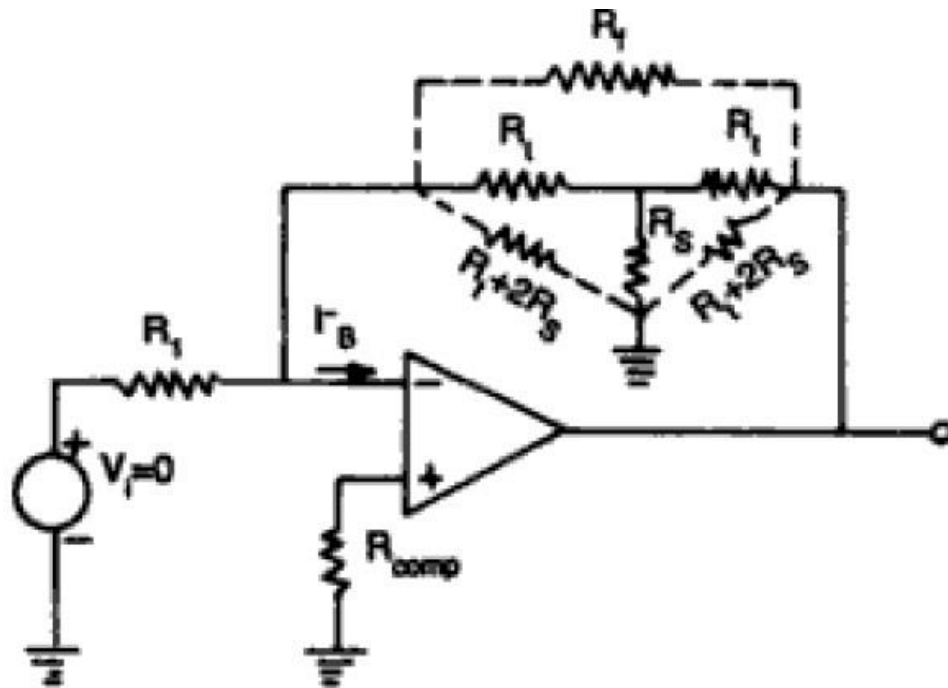


Fig. 3.1 (d) Inverting amplifier with T-feedback network

The T-feedback network in Fig. 3.1 (d) is a good solution. This will allow large feedback resistance, while keeping the resistance to ground (seen by the inverting input) low as shown in the dotted network. The T-network provides a feedback signal as if the network were a single feedback resistor. By T to π conversion,

$$R_f = \frac{R_t^2 + 2 R_t R_s}{R_s}$$

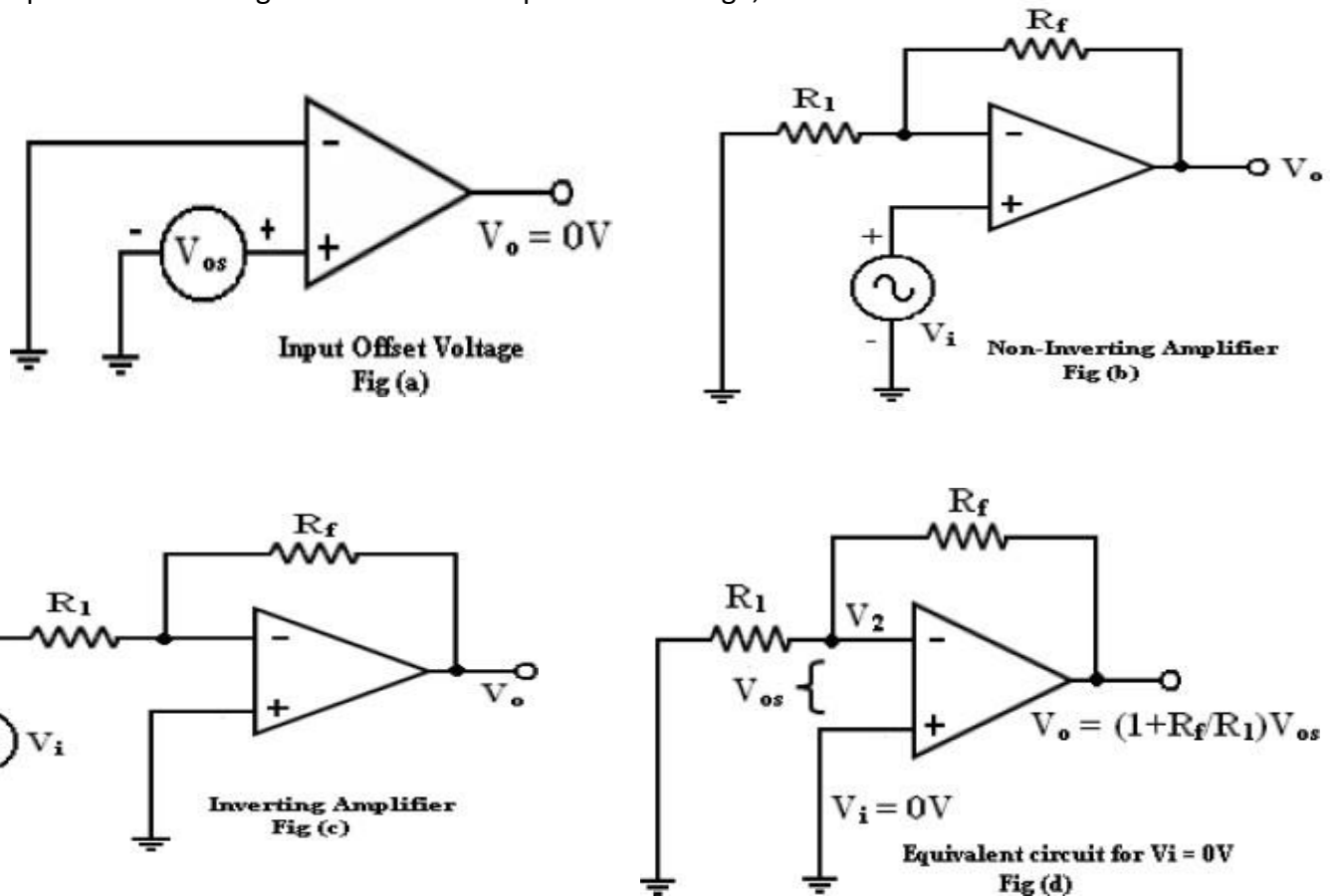
To design a T-network, first pick

$$R_t \ll \frac{R_f}{2}$$

$$\text{Then calculate } R_s = \frac{R_t^2}{R_f - 2R_t}$$

3. Input offset voltage:

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage, V_{os}



Let us determine the V_{os} on the output of inverting and non-inverting amplifier. If $V_i = 0$ (Fig (b) and (c)) become the same as in figure (d).

V_2 at the -ve input terminal is given by,

$$V_2 = \left(\frac{R_1}{R_1 + R_f} \right) V_o,$$

$$V_o = \left(\frac{R_1 + R_f}{R_1} \right) V_2 = \left(1 + \frac{R_f}{R_1} \right) V_2$$

since, $V_{ios} = |V_i - V_2|$ and $V_i = 0$

$$V_{ios} = V_2, V_o = \left(1 + \frac{R_f}{R_1} \right) V_{ios}$$

4. Total Output Offset Voltage:

The maximum offset voltage at the output of an inverting and non-inverting amplifier without any compensation technique used is given by

$$V_{oT} = \left(1 + \frac{R_f}{R_1} \right) V_{ios} + R_f I_B$$

With Rcomp in the circuit, total output offset voltage will be given by

$$V_{oT} = \left(1 + \frac{R_f}{R_1} \right) V_{ios} + R_f I_{os}$$

5. THERMAL DRIFT:

- Bias current, offset current and offset voltage change with temperature.
- A circuit carefully nulled at 25°C may not remain so when the temperature rises to 35°C. This is called drift.
- Offset current drift is expressed in nA/°C.
- Offset voltage drift is expressed in mV/°C.
- Indicates the change in offset for each degree Celsius change in temperature

AC Characteristics:

1. Frequency Response

Ideally, an op-amp should have an infinite bandwidth but practically op-amp gain decreases at higher frequencies. Such a gain reduction with respect to frequency is called as roll off.

Obtaining the frequency response:

To obtain the frequency response, consider the high frequency model of the op-amp with capacitor C at the output, taking into account the **capacitive effect** present

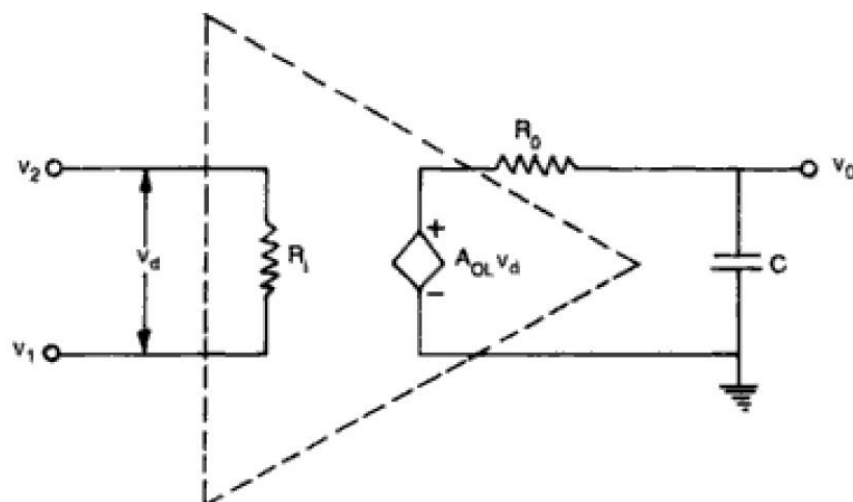


Fig. 3.4 (a) High frequency model of an op-amp with single corner frequency

The open loop voltage gain of an op-amp with only one corner frequency is obtained from Fig. 3.4 (a) as

$$v_o = \frac{-jX_c}{R_o - jX_c} A_{OL} v_d$$

$$A = \frac{v_o}{v_d} = \frac{A_{OL}}{1 + j 2\pi f R_o C}$$

$$A = \frac{A_{OL}}{1 + j(f/f_1)}$$

where

$$f_1 = \frac{1}{2\pi R_o C}$$

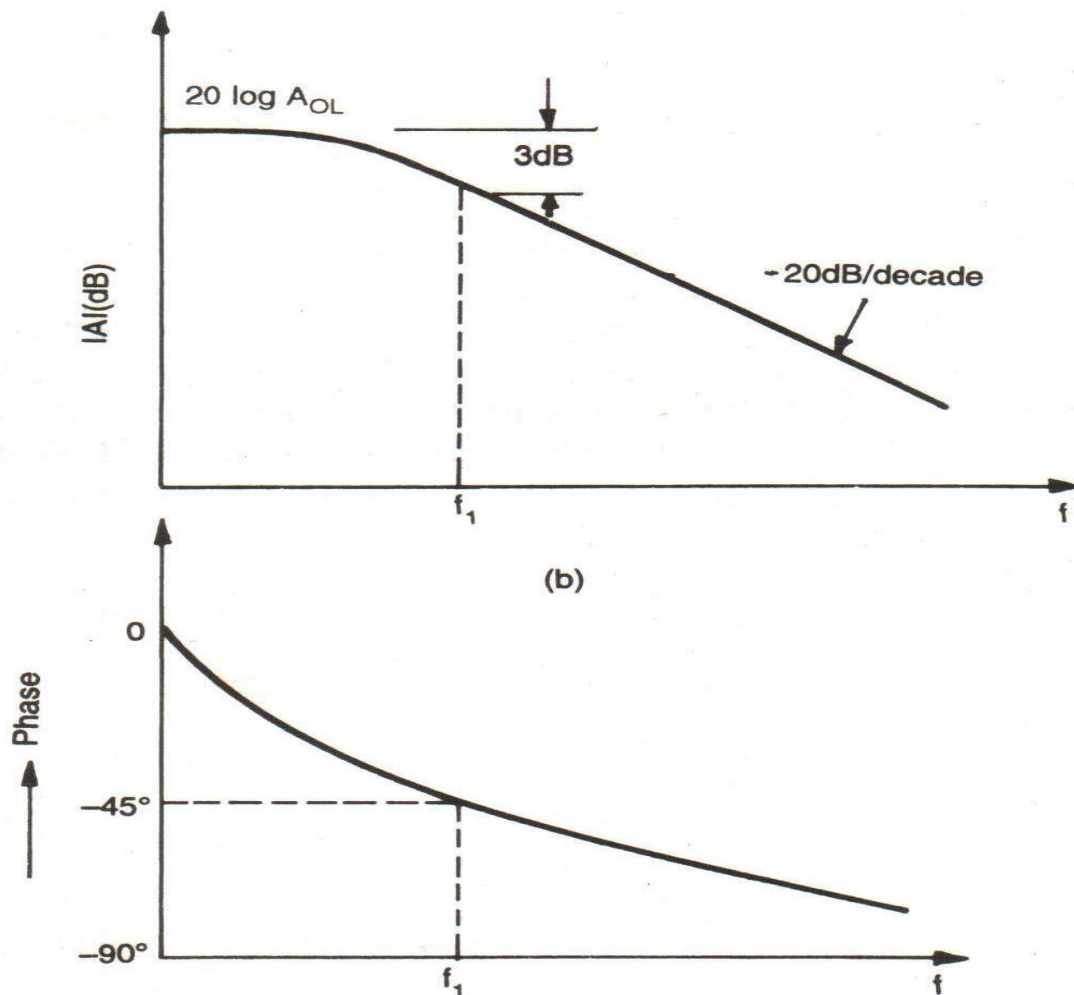
is the corner frequency or the upper 3-dB frequency of the op-amp. The magnitude and the phase angle of the open loop voltage gain are function of frequency and can be written as

$$|A| = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}}$$

$$\phi = -\tan^{-1} (f/f_1)$$

From the magnitude & phase characteristics, it can be seen that

- for $f \ll f_1$, the magnitude of the gain is $20 \log A_{OL}$ in dB
- for $f = f_1$, the gain is 3dB down from the dc value of A_{OL} , called corner frequency.
- for $f \gg f_1$, the gain rolls-off at the rate of -20 dB/decade or -6 dB/octave .



- From the phase characteristics
 - Phase angle is zero at $f = 0$

- At f_1 , the phase angle is -45° (lagging) and
- An infinite frequency, the phase angle is -90° .

For single RC pair, maximum phase change of 90° can occur. The voltage transfer function in s-domain can be written as

$$A = \frac{A_{OL}}{1 + j(f/f_1)} = \frac{A_{OL}}{1 + j(\omega/\omega_1)}$$

$$= \frac{A_{OL} \cdot \omega_1}{j\omega + \omega_1} = \frac{A_{OL} \cdot \omega_1}{s + \omega_1}$$

A practical op-amp, however, has number of stages and each stage produces a capacitive component. Thus due to a number of RC pole pairs, there will be a number of different break frequencies. The transfer function of an op-amp with three break frequencies can be assumed as

$$A = \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}; 0 < f_1 < f_2 < f_3$$

or,

$$A = \frac{A_{OL} \cdot \omega_1 \cdot \omega_2 \cdot \omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)}$$

with $0 < \omega_1 < \omega_2 < \omega_3$.

For a typical op-amp, straight line approximation of open-loop gain vs frequency in logarithmic scale is shown in Fig. 3.5. The open loop

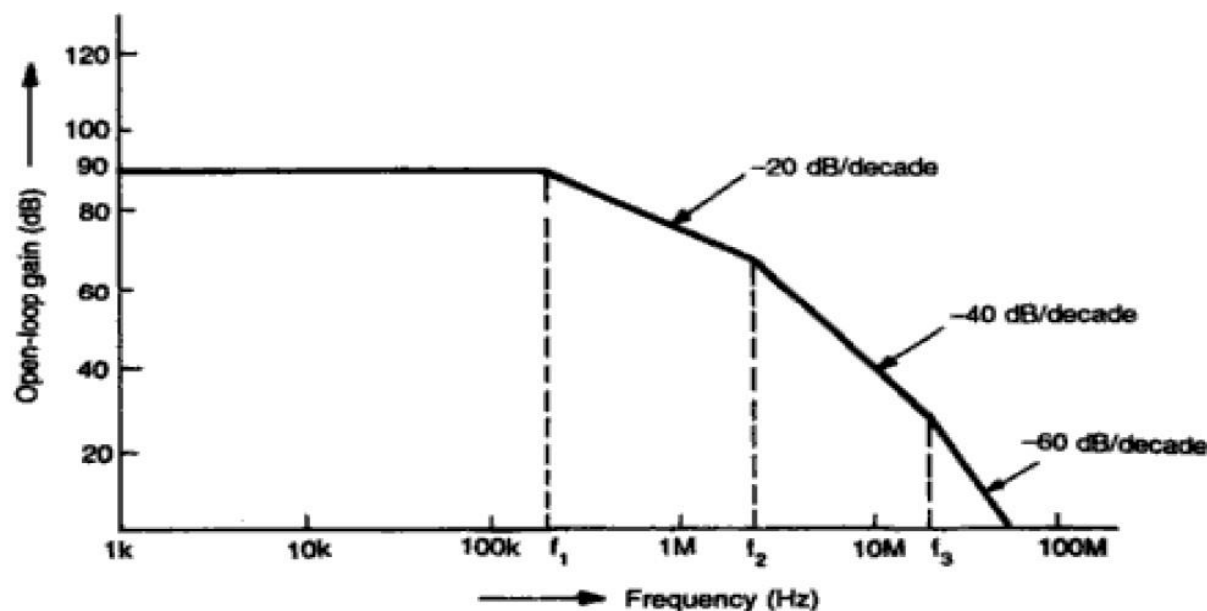


Fig. 3.5 Approximation of open loop gain vs frequency curve

frequency response is flat (90 dB) from low frequencies (including dc) to 200 kHz, the first break frequency. From 200 kHz to 2 MHz, the gain drops from 90 dB to 70 dB which is at a -20 dB/decade or -6 dB/octave rate. At frequencies from 2 MHz to 20 MHz, the roll-off rate is -40 dB/decade or -12 dB/octave. Accordingly, as frequency is increasing,

Stability of an Op-Amp

Op-amps are rarely used in open loop configuration because of its high gain. Let us now consider the effect of feedback on op-amp frequency response. Consider an op-amp amplifier of Fig. 3.6. (a). It uses resistor feedback network and may be used as an inverting amplifier for $v_2 = 0$ and as non-inverting amplifier for $v_1 = 0$.

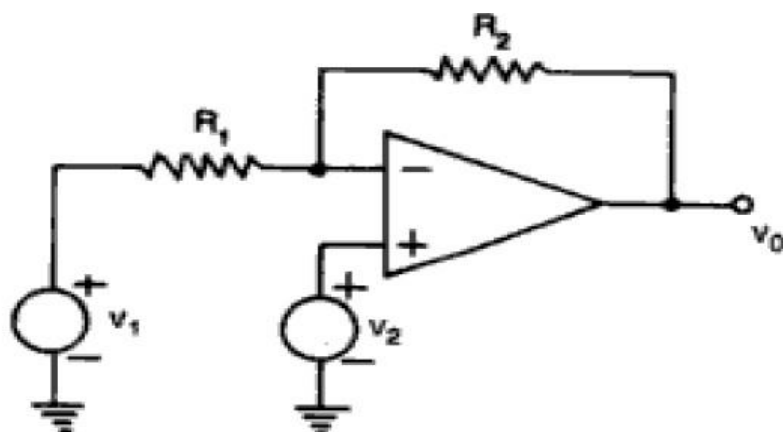


Fig. 3.6 (a) Resistive feedback provided in op-amp

The closed loop transfer function is

$$A_{CL} = A / (1 + A\beta)$$

If the characteristic equation $(1 + A\beta) = 0$, circuit will become unstable, (i.e.) it leads to sustained oscillation

Re-writing the characteristic equation as

$$(1 - (-A\beta)) = 0 \text{ leads to } -A\beta = 1$$

Magnitude and Phase condition becomes

$$|A\beta| = 1 \quad \text{and}$$

$$\angle -A\beta = 0 \text{ (or multiple of } 2\pi)$$

$$\angle A\beta = \pi \text{ (or odd multiple of } \pi)$$

- At low frequencies, the resistor in the feedback has no effect, except producing 180 deg. Phase shift.
- However, at high frequencies, for each corner frequencies, an additional phase shift of maximum -90° can take place in open loop gain A.
- For two corner frequencies, it will be -180° deg.
- For a specific value of β , $A\beta = 1$, when A is -180° deg.
- This results in oscillation and this instability means unbounded output.
- $(1 + A\beta) < 1$ (or) $A\beta < 0$ & $A_{CL} > A$

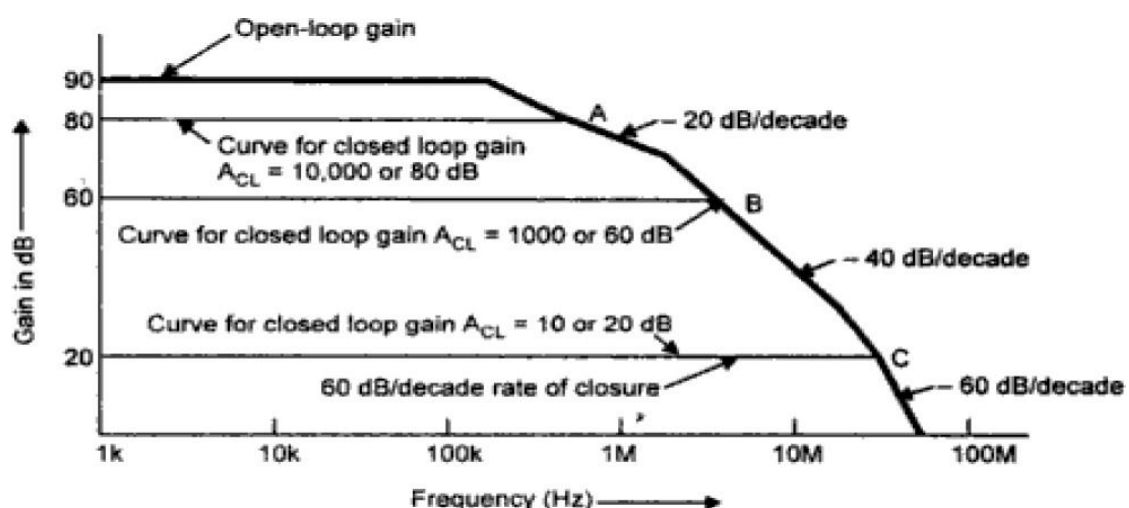


Fig. 3.6 (b) Effect of feedback on open loop gain vs frequency curve

Slew rate:

It is defined as the maximum rate of change of output voltage caused by a step input voltage.

The slew rate is specified in V/μsec

$$\text{Slew rate} = S = dV_o / dt \big|_{\max}$$

It is specified by the op-amp in unity gain condition.

The slew rate is caused due to limited charging rate of the compensation capacitor and current limiting and saturation of the internal stages of op-amp, when a high frequency large amplitude signal is applied.

$$\text{It is given by } dV_c / dt = I / C$$

For large charging rate, the capacitor should be small or the current should be large.

$$S = I_{\max} / C$$

For 741 IC the charging current is 15 μA and the internal capacitor is 30 pF. $S = 0.5V / \mu\text{sec}$

Slew rate limits the response speed of all large signal wave shapes.

Slew rate equation:

$$V_s = V_m \sin \omega t$$

$$V_o = V_m \sin \omega t$$

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t$$

$$S = \text{slew rate} = \left. \frac{dV_o}{dt} \right|_{\max}$$

$$S = V_m \omega = 2 \pi f V_m$$

$$S = 2 \pi f V_m \text{ V / sec}$$

This is also called **full power bandwidth** of the op-amp

For distortion free output, the maximum allowable input frequency f_m can be obtained as

$$f_m = \frac{S}{2\pi V_m}$$

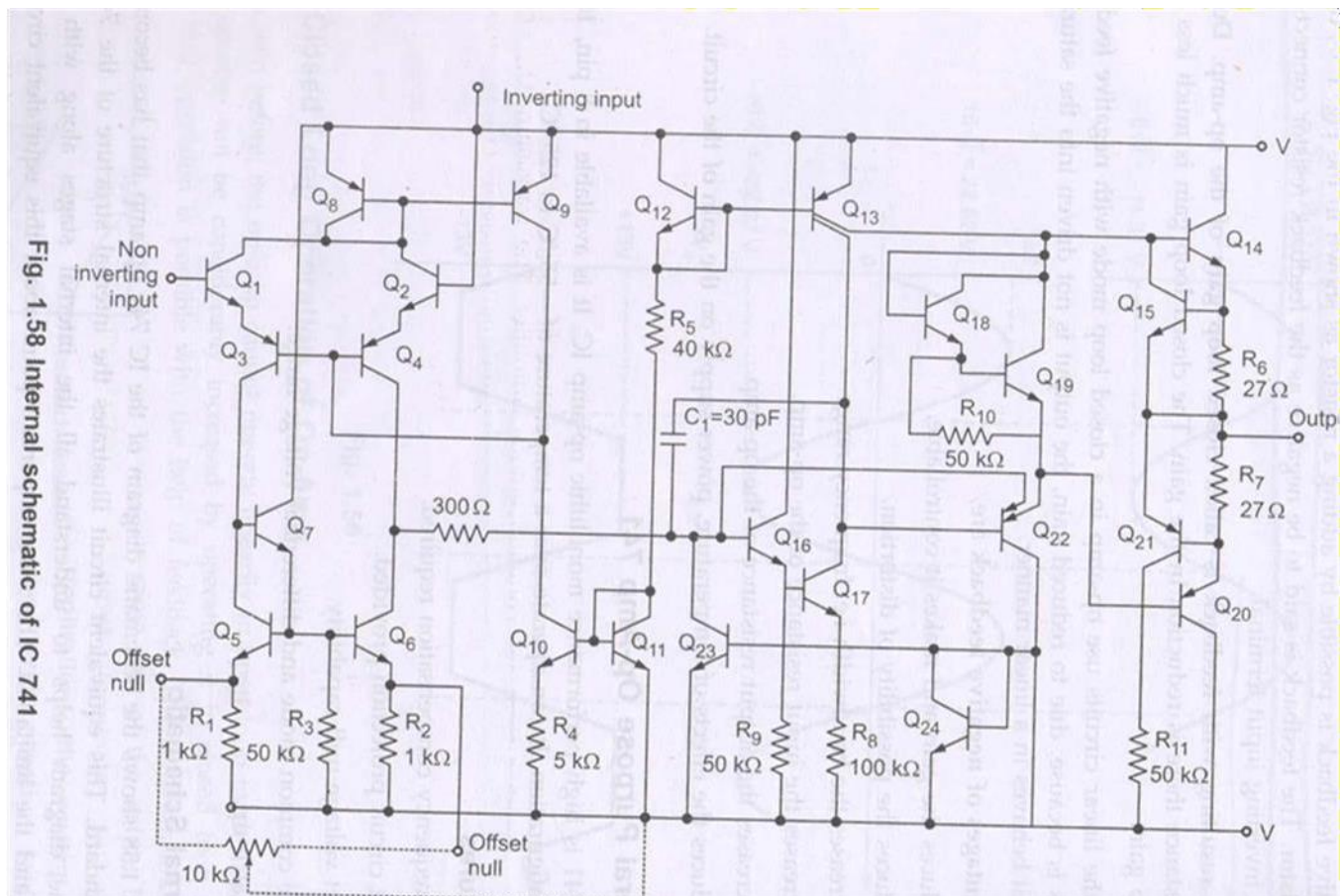
Features of 741 Op-Amp:

The IC 741 is high performance monolithic op-amp IC. It is available in 8pin, 10pin or 14pin configuration. It can operate over a temperature of -55°C to 125°C .

Features:

- i) No frequency compensation required
- ii) Short circuit protection provided
- iii) Offset Voltage null capability
- iv) Large common mode and differential voltage range
- v) No latch up
- vi) It consumes low power

Internal schematic of 741 op-amp:



8pin DIP package of IC 741:

The 8 pin DIP package of IC 741 is shown in the Fig. 1.59.

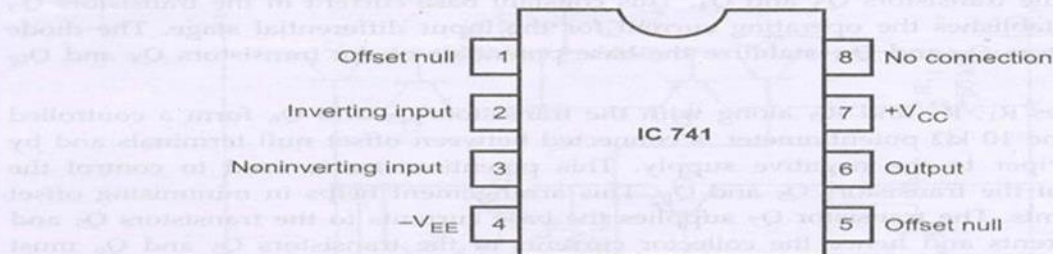


Fig. 1.59 8 Pin diagram

1.26.3 Ideal Vs Practical Characteristics of IC 741 Op-Amp

The Table 1.7 lists the ideal op-amp characteristics and the typical characteristics of 741 IC, a popular general purpose op-amp IC.

Sr. No	Parameter	Symbol	Ideal	Typical for 741 IC
1	Open loop voltage gain	A_{OL}	∞	2×10^5
2	Output impedance	Z_{out}	0	75Ω
3	Input impedance	Z_{in}	∞	2 M Ω
4	Input offset current	I_{ios}	0	20 nA
5	Input offset voltage	V_{ios}	0	1 mV
6	Bandwidth	B.W	∞	1 MHz
7	CMRR	ρ	∞	90 dB
8	Slew rate	S	∞	0.5 V/ μ sec
9	Input bias current	I_b	0	80 nA
10	PSRR	PSRR	0	30 μ V/V

Table 1.7

Modes of Operation using an op-amp:

- ✓ **Open Loop** : The output assumes one of the two possible output states, that is $+V_{sat}$ or $-V_{sat}$ and the amplifier acts as a switch only.
- ✓ **Closed Loop**: The utility of an op-amp can be greatly increased by providing negative feedback. The output in this case is not driven into saturation and the circuit behaves in a linear manner.

Open loop op-amp configurations:

- ✓ The configuration in which output depends on input, but output has no effect on the input is called open loop configuration.

- ✓ No feedback from output to input is used in such configuration.
- ✓ The op-amp can be used in three modes in open loop configuration they are
 1. Differential amplifier
 2. Inverting amplifier
 3. Non inverting amplifier

Differential Amplifier:

The amplifier which amplifies the difference between the two input voltages is called differential amplifier.

$$V_o = A_{OL} V_d = A_{OL} (V_1 - V_2) = A_{OL} (V_{in1} - V_{in2})$$

For very small V_d , output gets driven into saturation due to high A_{OL} , hence this application is applicable for very small range of differential input voltage.

Inverting Amplifier:

The amplifier in which the output is inverted i.e. having 180° phase shift with respect to the input is called an inverting amplifier .

$$V_o = -A_{OL} V_{in2}$$

The negative sign indicates that there is phase shift of 180° between input and output i.e. output is inverted with respect to input

Non-inverting Amplifier:

The amplifier in which the output is amplified without any phase shift in between input and output is called non inverting amplifier

$$V_o = A_{OL} V_{in1}$$

The positive output shows that input and output are in phase and input is amplified A_{OL} times to get the output.

Why op-amp is generally not used in open loop mode?

- As open loop gain of op-amp is very large, very small input voltage drives the op-amp voltage to the saturation level. Thus in open loop configuration, the output is at its

positive saturation voltage ($+V_{sat}$) or negative saturation voltage ($-V_{sat}$) depending on which input V_1 or V_2 is more than the other.

- For a.c. input voltages, output may switch between positive and negative saturation voltages.

Closed loop operation of op-amp:

The closed loop operation is possible with the help of feedback. The feedback allows to feed some part of the output back to the input terminals. In the linear applications, the op-amp is always used with negative feedback. The negative feedback helps in controlling gain, which otherwise drives the op-amp out of its linear range, even for a small noise voltage at the input terminals

Inverting Amplifier:

In an inverting amplifier circuit, the operational amplifier inverting input receives feedback from the output of the amplifier.

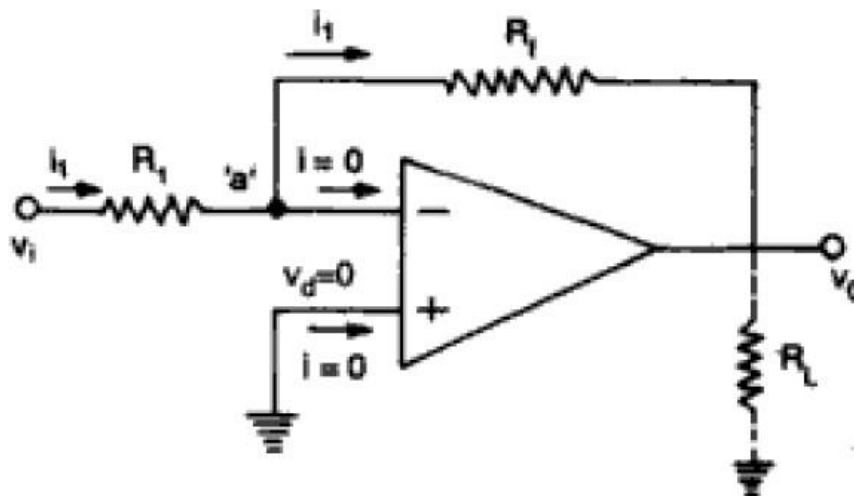


Fig. 2.5 (a) Inverting amplifier

Analysis: For simplicity, assume an ideal op-amp. As $v_d = 0$, node 'a' is at ground potential and the current i_1 through R_1 is

$$i_1 = \frac{v_i}{R_1} \quad (2.2)$$

Also since op-amp draws no current, all the current flowing through R_1 must flow through R_f . The output voltage,

$$v_o = -i_1 R_f = -v_i \frac{R_f}{R_1} \quad (2.3)$$

Hence, the gain of the inverting amplifier (also referred as closed loop gain) is,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1} \quad (2.4)$$

Alternatively, the nodal equation at the node 'a' in Fig. 2.5 (a) is

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{R_f} = 0$$

where v_a is the voltage at node 'a'. Since node 'a' is at virtual ground $v_a = 0$. Therefore, we get,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$

The negative sign indicates a phase shift of 180° between v_i and v_o . Also since inverting input terminal is at virtual ground, the effective input impedance is R_1 . The value of R_1 should be kept fairly large to avoid loading effect. This however, limits the gain that can be obtained from this circuit. A load resistor R_L is usually put at the output in actual practice otherwise, the input impedance of the measuring device such as oscilloscope or DVM acts as the load.

Example 2.1

Design an amplifier with a gain of -10 and input resistance equal to $10\text{ k}\Omega$.

Solution

Since the gain of the amplifier is negative, an inverting amplifier has to be made.

In Fig. 2.5 (a) choose $R_1 = 10\text{ k}\Omega$

$$\begin{aligned}\text{Then } R_f &= -A_{CL} R_1 \text{ (from Eq. 2.4)} \\ &= -(-10) \times 10\text{ k}\Omega = 100\text{ k}\Omega\end{aligned}$$

Example 2.2

In Fig. 2.5 (b), $R_1 = 10\text{ k}\Omega$, $R_f = 100\text{ k}\Omega$, $v_i = 1\text{ V}$. A load of $25\text{ k}\Omega$ is connected to the output terminal. Calculate (i) i_1 (ii) v_o (iii) i_L and total current i_o into the output pin.

Solution

$$(a) \ i_1 = \frac{v_i}{R_1} = \frac{1\text{ V}}{10\text{ k}\Omega} = 0.1\text{ mA}$$

$$(b) \ v_o = -\frac{R_f}{R_1} v_i = -\frac{100\text{ k}\Omega}{10\text{ k}\Omega} 1\text{ V} = -10\text{ V}$$

$$(c) \ i_L = \frac{v_o}{R_L} = \frac{10\text{ V}}{25\text{ k}\Omega} = 0.4\text{ mA}$$

The direction of i_L is shown in Fig. 2.5 (b).

(d) i_1 as calculated above is 0.1 mA .

Therefore, total current $i_o = i_1 + i_L = 0.1\text{ mA} + 0.4\text{ mA} = 0.5\text{ mA}$. In an inverting amplifier, for a +ive input, output will be -ive, therefore the direction of i_o is as shown in Fig. 2.5 (b).

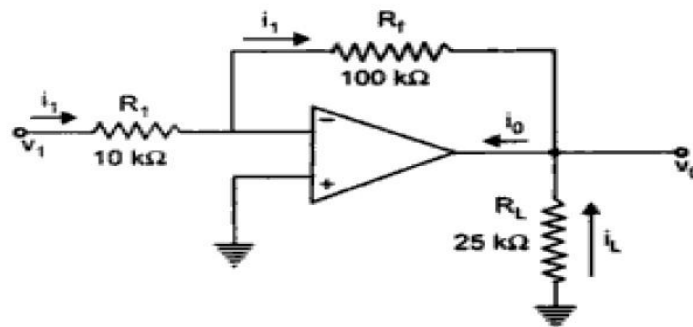


Fig. 2.5 (b) Circuit for Example 2.2

Non-Inverting Amplifier:

If the signal is applied to the non-inverting input terminal and feedback is given as shown in fig, the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier. Negative feedback system as output is being fed back to the inverting input terminal.

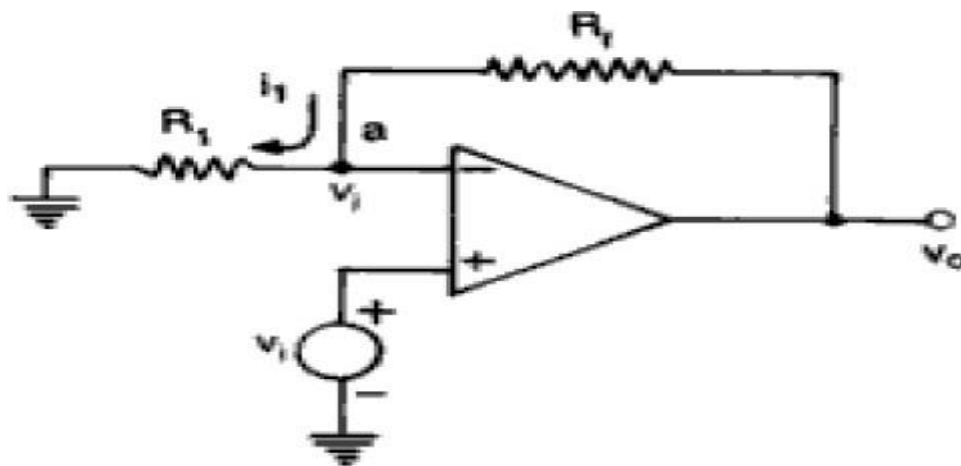


Fig. 2.7 (a) Non-inverting amplifier

As the differential voltage v_d at the input terminal of op-amp is zero, the voltage at node 'a' in Fig. 2.7 (a) is v_i , same as the input voltage applied to non-inverting input terminal. Now R_f and R_1 forms a potential divider. Hence

$$v_i = \frac{v_o}{R_1 + R_f} R_1$$

as no current flows into the op-amp.

$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}$$

Thus, for non-inverting amplifier the voltage gain,

$$A_{CL} = \frac{v_o}{v_i} = 1 + \frac{R_f}{R_1}$$

Comparison of the ideal inverting and non-inverting op-ampr.

Ideal Inverting amplifier	Ideal non-inverting amplifier
1. Voltage gain= $-R_f/R_1$	1. Voltage gain= $1+R_f/R_1$
2.The output is inverted with respect to input	2.No phase shift between input and output
3.The voltage gain can be adjusted as greater than, equal to or less than one	3.The voltage gain is always greater than one
4.The value of input impedance R_1 should be kept fairly large to avoid loading effect	4. The input impedance is very large.

Differential Amplifier:

A circuit that amplifies the difference between two signals is called a difference or differential amplifier. This type of the amplifier is very **useful in instrumentation circuits**

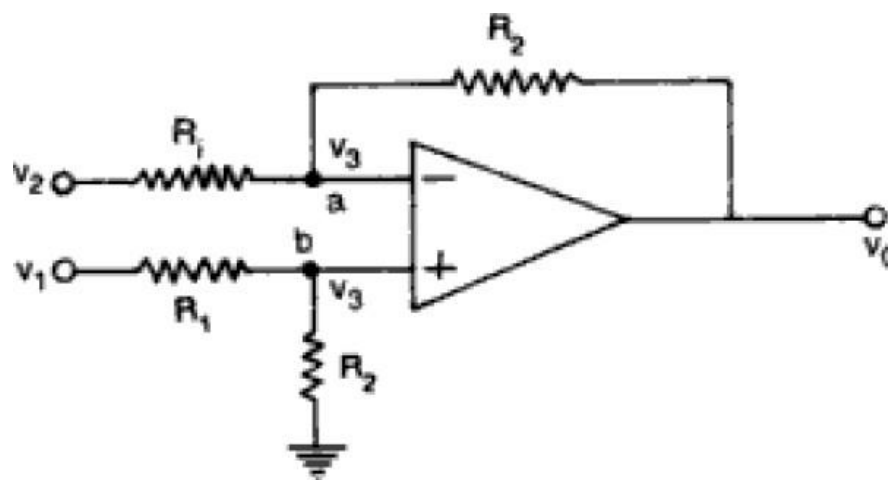


Fig. 2.8 A differential amplifier

The nodal equation at 'a' is,

$$\frac{v_3 - v_2}{R_1} + \frac{v_3 - v_o}{R_2} = 0 \quad (2.25)$$

and at 'b' is

$$\frac{v_3 - v_1}{R_1} + \frac{v_3}{R_2} = 0 \quad (2.26)$$

Rearranging, we get

$$\left(\frac{1}{R_1} + \frac{1}{R_2} \right) v_3 - \frac{v_2}{R_1} = \frac{v_o}{R_2} \quad (2.27)$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2} \right) v_3 - \frac{v_1}{R_1} = 0 \quad (2.28)$$

Subtracting Eq. (2.28) from (2.27) we get,

$$\frac{1}{R_1} (v_1 - v_2) = \frac{v_o}{R_2} \quad (2.29)$$

Therefore,

$$v_o = \frac{R_2}{R_1} (v_1 - v_2) \quad (2.30)$$

Such a circuit is very useful in detecting very small differences in signals, since the gain R_2/R_1 can be chosen to be very large. For

Difference mode and Common Mode Gains:

The output voltage depends on difference voltage (v_d) and average voltage of input signals called as common mode (v_{CM}) signals.

$$v_d = v_1 - v_2 \quad v_{CM} = \frac{v_1 + v_2}{2} \quad \dots\dots\dots(1)$$

The output voltage is expressed as

$$v_o = A_1 v_1 + A_2 v_2 \quad \text{.....(2)}$$

where, A_1 (A_2) is the voltage amplification from input 1 (2) to the output with input 2(1) grounded. Since $v_{CM} = (v_1 + v_2)/2$ and $v_d = (v_1 - v_2)$,

$$v_1 = v_{CM} + \frac{1}{2} v_d$$

and
$$v_2 = v_{CM} - \frac{1}{2} v_d$$

Substituting the value of v_1 and v_2 in Eq.(2)

$$v_o = \frac{1}{2} (A_1 - A_2) v_d + (A_1 + A_2) v_{CM}$$

$$v_o = A_{DM} v_d + A_c v_c$$

where,
$$A_{DM} = \frac{1}{2} (A_1 - A_2)$$

and
$$A_{CM} = A_1 + A_2$$

Common Mode Rejection Ratio (CMRR): the relative sensitivity of an op-amp to a difference signal as compared to a common mode signal is called as CMRR (ρ).

$$\rho = \left| \frac{A_{DM}}{A_{CM}} \right|$$

Instrumentation Amplifier:

An instrumentation amplifier is a type of differential amplifier that has been outfitted with input buffers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use in measurement and test equipment. In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier

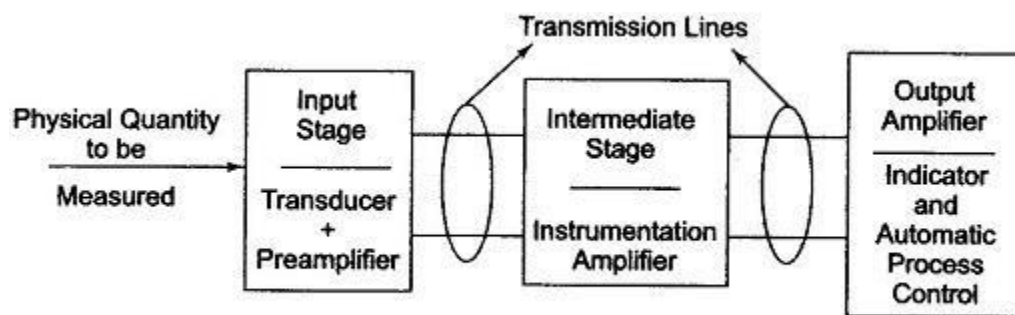
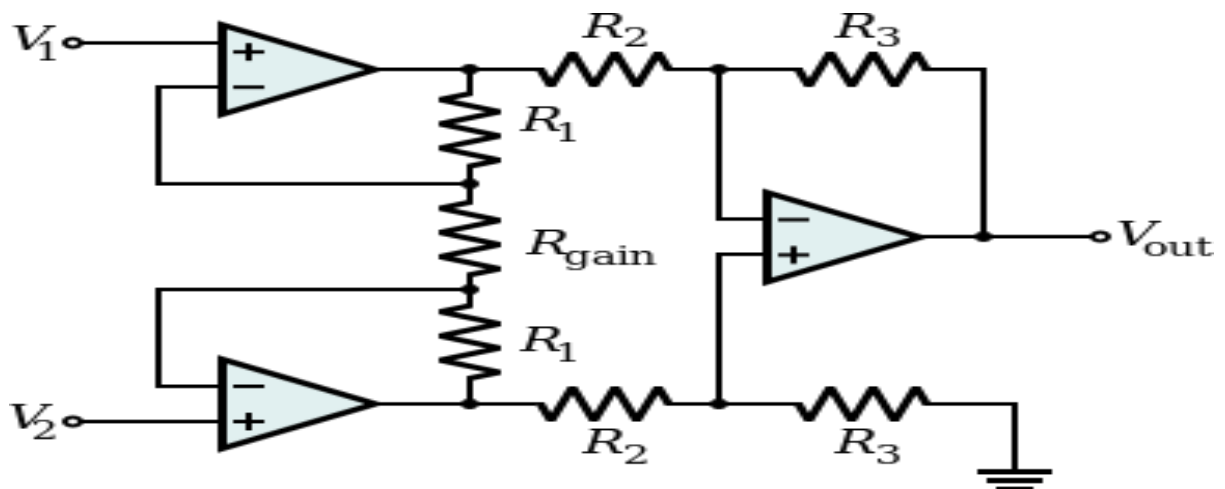


Fig. 14.24 Block Diagram of an Instrumentation System

Circuit Diagram:



- The op-amps 1 & 2 are non-inverting amplifiers and op-amp 3 is a difference amplifier. These three op-amps together, form an instrumentation amplifier.

- Instrumentation amplifier's final output V_{out} is the amplified difference of the input signals applied to the input terminals of op-amp 3.
- Let the outputs of op-amp 1 and op-amp 2 be V_{o1} and V_{o2} respectively. Then,

$$V_{out} = (R_3/R_2)(V_{o1}-V_{o2})$$

- The working of the instrumentation amplifier is, Ideally the current to the input stage op-amps is zero. Therefore the current I through the resistors R_1 , R_{gain} , and R_1 remain the same.

- Applying Ohm's law between nodes

$$I = (V_{o1}-V_{o2})/(R_1+R_{gain}+R_1) \dots (1)$$

$$I = (V_{o1}-V_{o2})/(2R_1+R_{gain})$$

- Since no current is flowing to the input of the op-amps 1 & 2, the current I between the nodes G and H can be given as,

$$I = (V_G - V_H) / R_{gain} = (V_1 - V_2) / R_{gain} \dots \dots \dots (2)$$

- Equating equations 1 and 2,

$$(V_{o1}-V_{o2})/(2R_1+R_{gain}) = (V_1-V_2)/R_{gain}$$

$$(V_{o1}-V_{o2}) = (2R_1+R_{gain})(V_1-V_2)/R_{gain} \dots \dots \dots (3)$$

- The output of the difference amplifier is given as,

$$V_{out} = (R_3/R_2) (V_{o1}-V_{o2}) \text{ Therefore, } (V_{o1} - V_{o2}) = (R_2/R_3)V_{out}$$

- Substituting $(V_{o1} - V_{o2})$ value in equation 3, we get

$$(R_2/R_3)V_{out} = (2R_1+R_{gain})(V_1-V_2)/R_{gain}$$

- **i.e. $V_{out} = (R_3/R_2)\{(2R_1+R_{gain})/R_{gain}\}(V_1-V_2)$**

The overall voltage gain of an instrumentation amplifier can be controlled by adjusting the value of resistor R_{gain} .

Features of instrumentation amplifier:

- High gain accuracy
- High CMRR
- High gain stability with low temperature coefficient
- Low dc offset
- Low output impedance

Applications:

Instrumentation amplifiers are

- used in data acquisition from small o/p transducers like [thermocouples](#), strain gauges, measurements of [Wheatstone bridge](#), etc.
- used in navigation, medical, radar, etc.
- used to enhance the S/N ratio ([signal to noise](#)) in audio applications like audio signals with low amplitude.
- used for imaging as well as video data acquisition in the conditioning of high-speed signal.
- used in RF cable systems for amplification of the high-frequency signal.

AC Amplifier:

- To amplify a small AC input signal, such as an audio or radio frequency signal. A small AC voltage is applied to the input, through a coupling capacitor (Hence, such a circuit is useful only as an AC amplifier; to amplify DC signals you should use an operational amplifier circuit).
- To get the ac frequency response of an op-amp or if the ac input signal is superimposed with dc level, it becomes essential to block the dc component.
- This is achieved by using an AC amplifier with a coupling capacitor.
- AC amplifiers are two types 1) Inverting AC ampr.
2) Non Inverting AC ampr.

Inverting AC Amplifier:

From the fig. The capacitor C blocks the dc component of the input and together with the resistor R1 sets the lower 3 db freq. of the ampr.

The output vg. $V_o = -I R_f = V_i R_f / R_1 + 1/sC$ ----- (1)

Therefore,

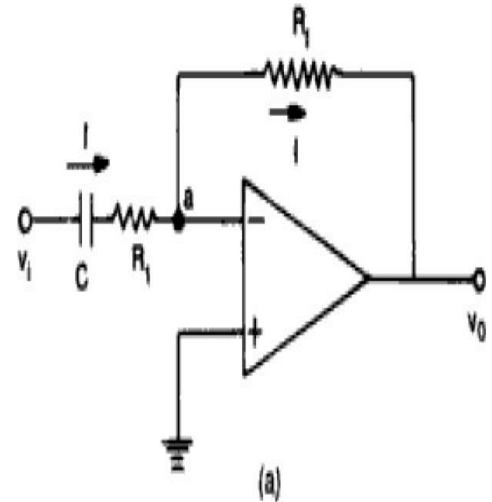
$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1} \frac{s}{s + 1/R_1 C}$$

It is seen from Eq. (4.24) that the lower 3dB frequency is,

$$f_L = \frac{1}{2\pi R_1 C}$$

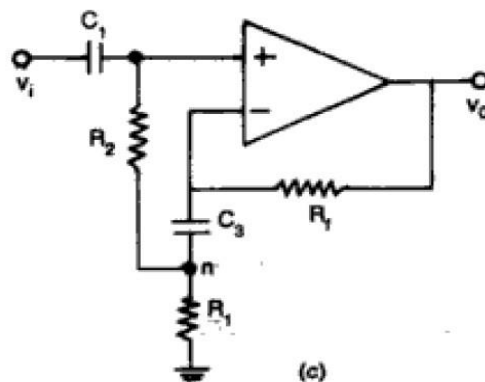
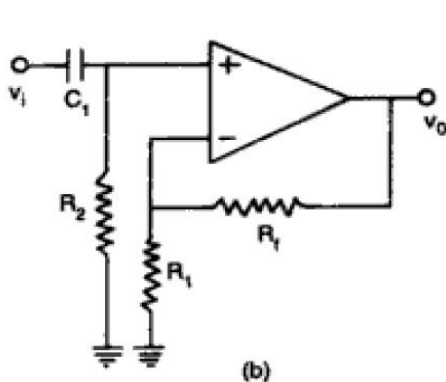
In the mid-band range of frequencies, capacitor C behaves short circuit and therefore, Eq. (4.24) becomes,

$$A_{CL} \approx -\frac{R_f}{R_1}$$



Non Inverting AC ampr.:

The circuit is shown in Fig. Here a resistor R_2 is added to provide a dc return to ground. However, this reduces the overall input impedance of the amplifier, which now becomes approximately R_2 . This problem of low input impedance is eliminated by connecting a capacitor C_s as in Fig.



Voltage Follower:

The circuit is used as a buffer to connect a high impedance signal sources to a low impedance load which may even be capacitive.

Hence the input resistance that the source sees is approximately $R_1/(1 - A_{CL})$ [from Miller's theorem] where A_{CL} is the gain of the voltage follower which is close to unity (0.9997). Thus very high input impedance can be obtained.

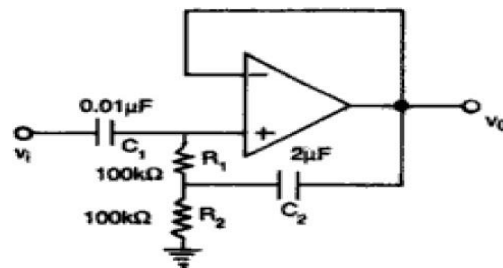


Fig. 4.7 AC voltage follower

DIFFERENTIATOR:

The Differentiator

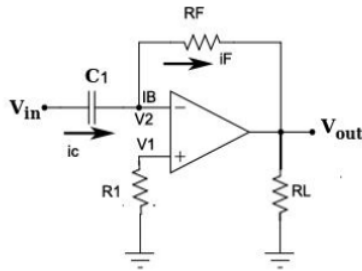


Figure 1

Figure shows the differentiator or differentiation amplifier. The circuit performs the mathematical operation of differentiation. i.e. The output waveform is the derivative of the input waveform.

The expression for the output voltage can be obtained from Kirchhoff's current equation written at node v_2 as

$$i_C = i_B + i_F$$

$$\text{since } i_B = 0$$

$$i_C = i_F$$

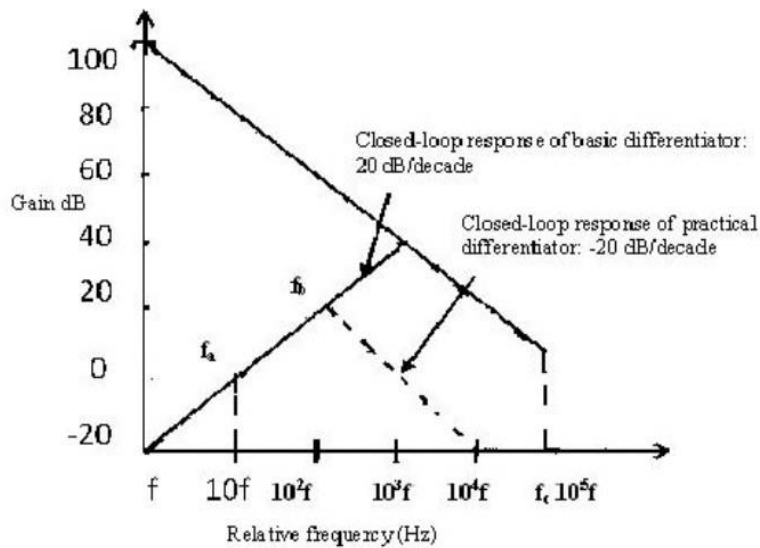
$$C_1 \frac{d}{dt}(v_{in} - v_2) = \frac{v_2 - v_o}{R_F}$$

$$\text{But } v_1 = v_2 = 0V$$

$$C_1 \frac{dv_{in}}{dt} = \frac{-v_o}{R_F}$$

$$\text{Or } v_o = -R_F C_1 \frac{dv_{in}}{dt}$$

Thus the output ' v_o ' is equal to the $R_F C_1$ times the negative instantaneous rate of change of the input voltage ' v_{in} ' with time. Since the differentiator performs the reverse of the integrator's function, a cosine wave input will produce a sine wave output, or triangular input will produce a square wave output. The differentiator given above is an unstable one and its frequency response is shown in the figure below.



In this figure 'fa' is the frequency at which the gain is 0dB and is given by

$$f_a = \frac{1}{2\pi R_F C_1}$$

Both the stability and high frequency noise problems in the differentiator shown in Fig (1) can be corrected by the addition of two components R_1 and C_F as shown in Fig (3). This circuit is a practical differentiator, the frequency response of which is shown in Fig (2) by the dotted lines. Up to frequency 'fb' the gain increases at 20dB /decade. After 'fb' gain decreases at 20dB/decade. This change in gain is caused by R_1C_1 and R_FC_F combinations. The gain limiting frequency fb is given by

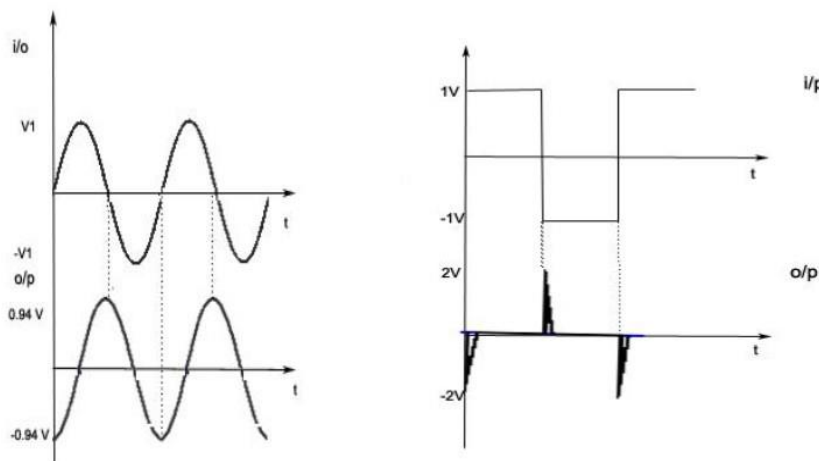
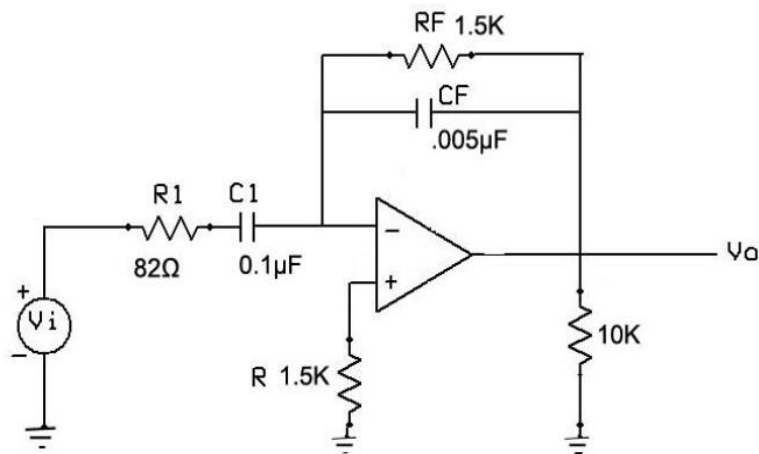
$$f_b = \frac{1}{2\pi R_1 C_1} \text{ where } R_1 C_1 = R_F C_F$$

R_FC_F and R_1C_1 help to reduce significantly the effect of high frequency input, amplifier noise and offsets. Above all, it makes the circuit more stable by presenting the increase in gain with frequency. The value of $f_b > f_a$

$$\text{Where } f_a = \frac{1}{2\pi R_F C_1}$$

$$\text{And } f_b = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_F C_F}$$

The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to $R_F C_1$. i.e. $T \geq R_F C_1$



The above figure shows the i/p and o/p wave forms of a differentiator

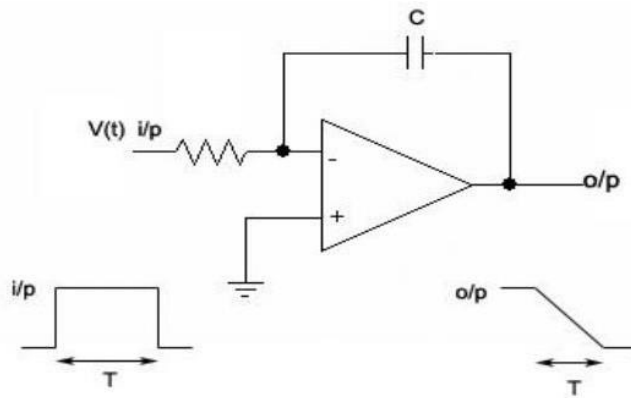
Designing of op-amp differentiator

1. Select f_a equal to the highest frequency of the input signal to be differentiated. Then assuming the value of $C_1 < 1\mu F$, calculate the value of R_F .
2. Choose $f_b = 20f_a$ and calculate the values of R_1 & C_F so that $R_1C_1 = R_FC_F$

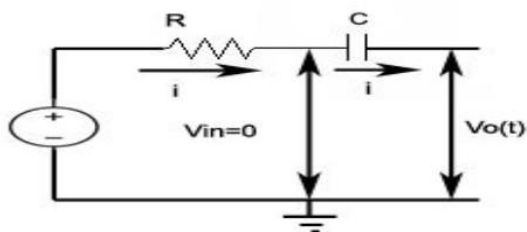
Use: The differentiator is most commonly used in waveshaping circuit to detect high frequency components in an input signal and also as a rate-of-change detector in FM modulator.

The Integrator

An integrator is a circuit that performs a mathematical operation called integration. Integration is a process of continuous addition. The most popular application of an integrator is to produce a ramp of output voltage, which is a linearly increasing or decreasing voltage.



The integrator is similar to an inverting amplifier except that the feedback is through a capacitor 'C' instead of resistor R_f .



Equivalent circuit of Op-amp Integrator

The virtual ground equivalent circuit shows that an expression between input and output voltage can be derived from the current i , which flows from input to output. The virtual ground means that the voltage at the junction point of resistor R and capacitor 'C' can be considered to be at ground but no current passes into the ground at that point.

Hence $i(t) = \frac{v(t)}{R}$ and output voltage

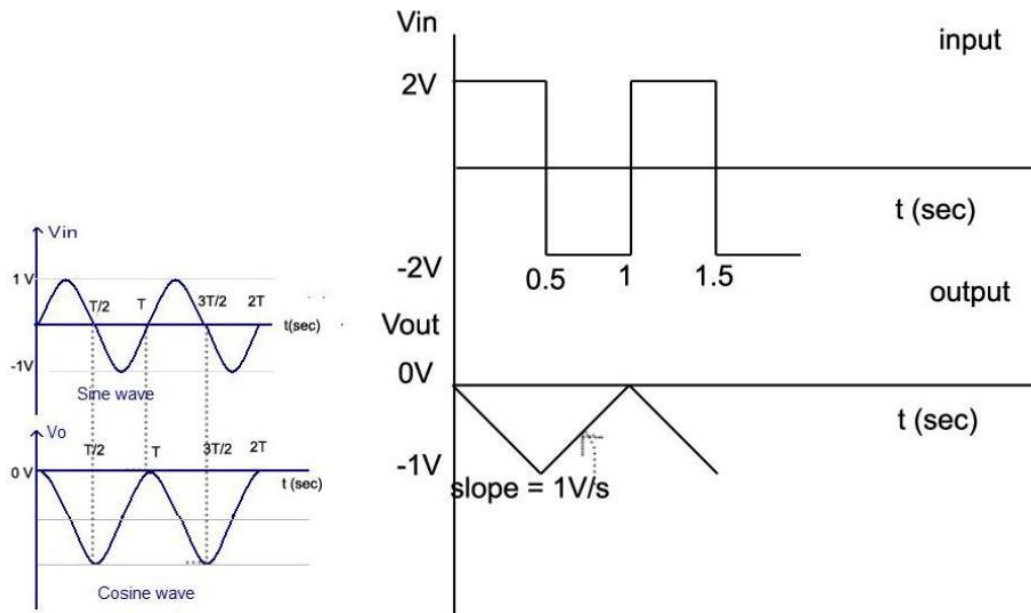
$$V_o(t) = -\frac{1}{C} \int i(t) dt = -\frac{1}{C} \int \frac{v(t)}{R} dt = -\frac{1}{RC} \int v(t) dt + A$$

Where A is the constant of integration and is proportional to the value of the output voltage V_o at time $t = 0$ second.

The output voltage is the integral of the input voltage, with an inversion and scale factor of $\frac{1}{RC}$.

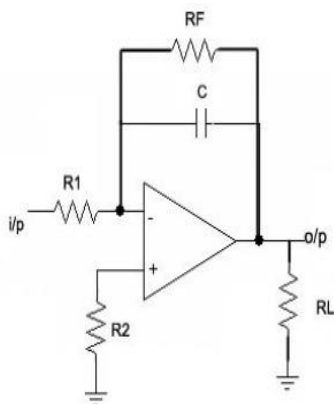
If the input voltage is a step voltage, then the output voltage will be a ramp or linearly changing voltage. If the input voltage is a square wave, the output voltage will be a triangular wave.

Integrators are widely used in ramp or sweep generators, filters, analog computers etc.



A practical integrator is shown below. The resistor R_f limits the low frequency gain and hence

The limitations of an ideal integrator can be minimized in the practical circuit by adding resistor R_f in parallel with capacitor C this R_f avoids op-amp going into open loop configuration at low frequencies.



minimizes the variations in the output voltage. The frequency response of the basic integrator is shown in figure below.

Frequency response of practical integrator:

$$A = \frac{R_f \parallel X_c}{R}$$

$$\therefore A = \frac{\left[\frac{R_f \times \frac{1}{j\omega C}}{R_f + \frac{1}{j\omega C}} \right]}{R}$$

$$\therefore A = \frac{\left[\frac{R_f}{j\omega C R_f + 1} \right]}{R}$$

$$\therefore A = \frac{R_f}{R(j\omega C R_f + 1)}$$

$$\therefore A = \frac{R_f}{R} \left[\frac{1}{(j2\pi f C R_f + 1)} \right]$$

Let $f_a = 1/(2\pi R_f C) \Rightarrow$ Break frequency or Corner frequency

$$A = \frac{R_f}{R} \left[\frac{1}{1 + j\left(\frac{f}{f_a}\right)} \right]$$

Where $f \gg$ Operating frequency the magnitude of gain A is,

$$|A| = \left| \frac{R_f}{R} \left[\frac{1}{1 + j\left(\frac{f}{f_a}\right)} \right] \right|$$

$$|A| = \left| \frac{R_f}{R} \left[\frac{1}{\sqrt{1 + \left(\frac{f}{f_a}\right)^2}} \right] \right|$$

Consider the following cases:

1. When $f=0$, the gain $|A| = |R_f/R|$ —dc gain
2. When $0 < f < f_a$, the gain $|A| \cong |R_f/R|$
3. When $f > f_a$, the gain $|A| \ll |R_f/R|$
4. When $f = f_a$, the gain $|A| = |R_f/R| (1/\sqrt{2})$ | Hence, $|A| = |0.707 (R_f/R)|$

Comparators

The comparator is a circuit that is used to compare two voltages and provide an output indicating the relationship between those two voltages. Comparators are used to compare

1. Two changing voltages to each other, as in comparing two sine waves or
2. A changing voltage to a set dc reference voltage.

Figure shows the circuit of an op-amp comparator. There is no feedback path in the circuit. In this circuit, the input voltage is applied to the non-inverting input terminal and a set reference voltage (V_{ref}) is applied to the inverting terminal of the op-amp.

Types of Comparators

1. Non-Inverting comparator

2. Inverting Comparator

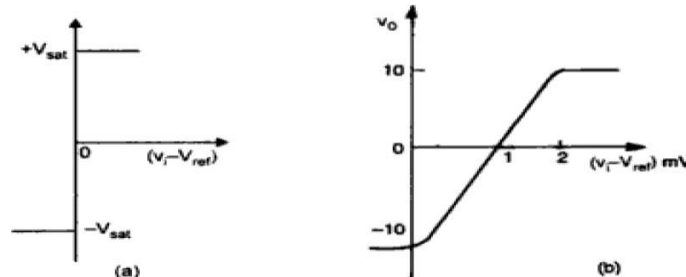
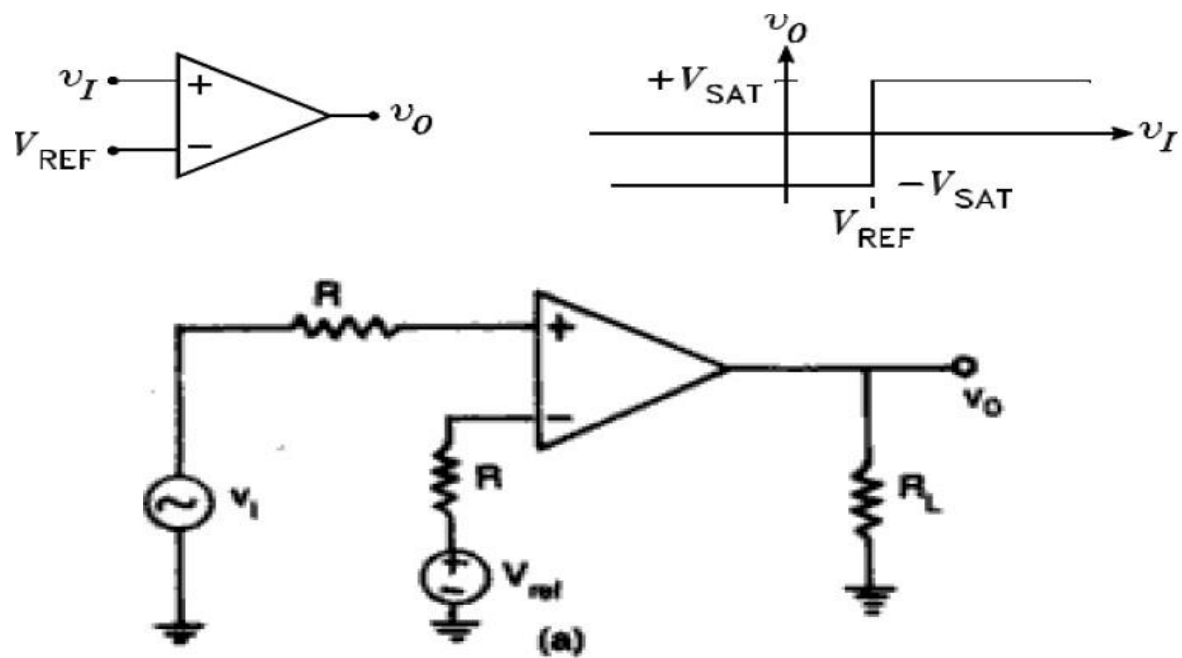
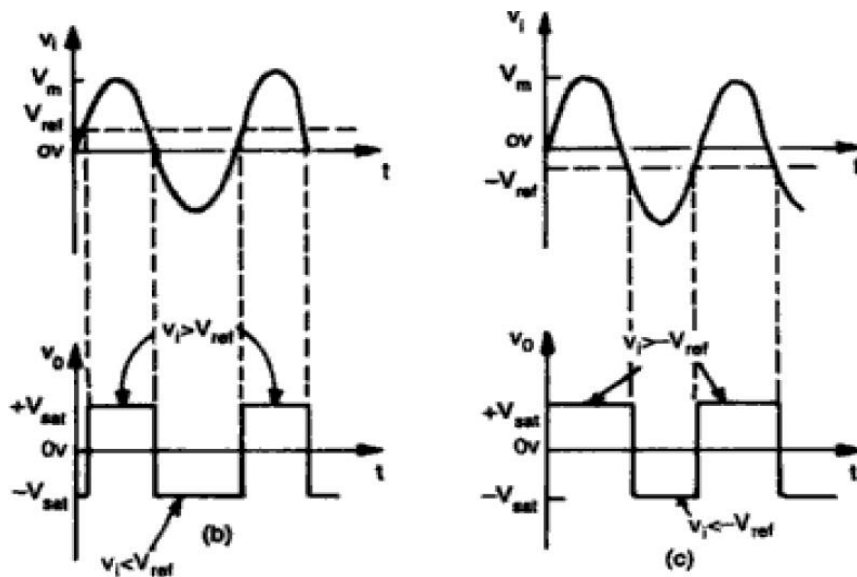


Fig. 5.1 The transfer characteristics (a) ideal comparator
(b) practical comparator

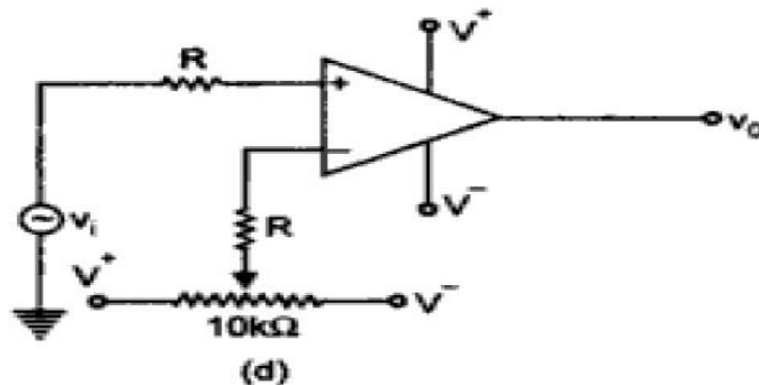
Non Inverting Comparator:



A fixed reference voltage V_{ref} is applied to (-) input and a time varying signal v_i is applied to (+) input. The output voltage is at $-V_{sat}$ for $v_i < V_{ref}$ And v_o goes to $+V_{sat}$ for $v_i > V_{ref}$.



Practical Non inverting Comparator

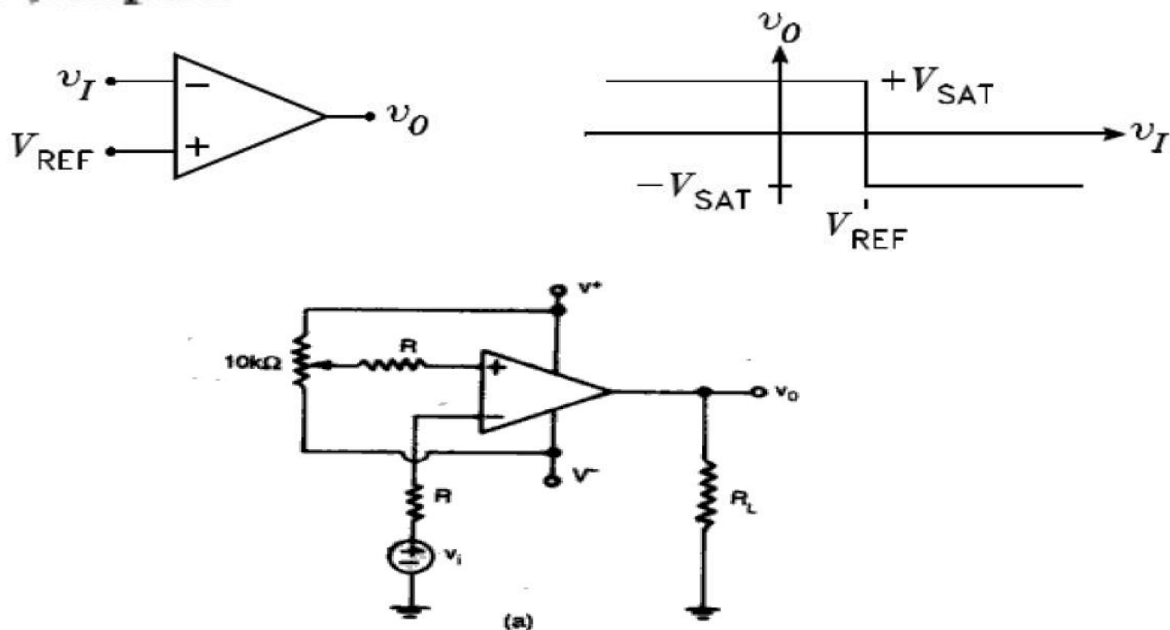


In a practical circuit V_{ref} is obtained by using a $10\text{ k}\Omega$ potentiometer which forms a voltage divider with the supply voltages V_+ and V_- with the wiper connected to $(-)$ input terminal.

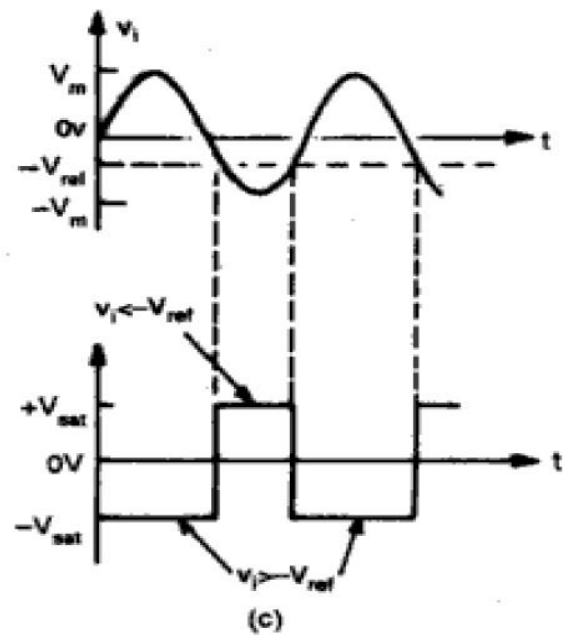
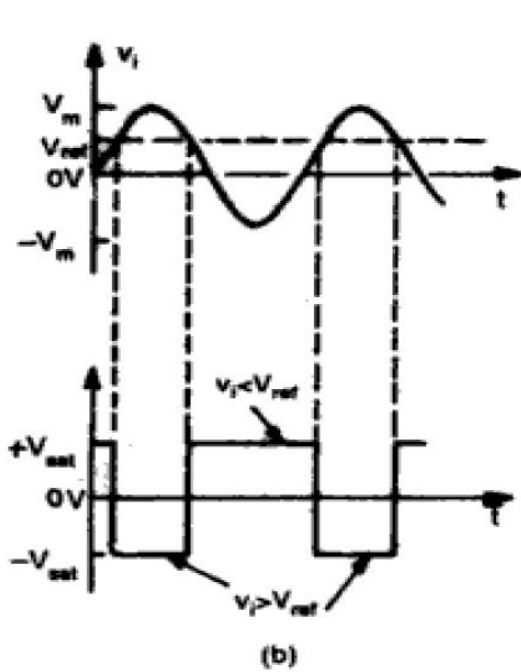
Thus a V_{ref} of desired amplitude and polarity can be obtained by simply adjusting the $10\text{ k}\Omega$ potentiometer.

Inverting Comparator:

Figure 5.3 (a) shows a practical inverting comparator in which the reference voltage V_{ref} is applied to the $(+)$ input and v_i is applied to $(-)$ input.



Input & Output wave forms:



Applications of Comparator:

1. Zero crossing detector
2. Window detector
3. Time marker generator
4. Phase detector

Zero crossing Detector:

A **zero crossing detector** or ZCD is a one type of voltage comparator, used to detect a sine waveform transition from positive and negative, that coincides when the i/p crosses the **zero** voltage condition.

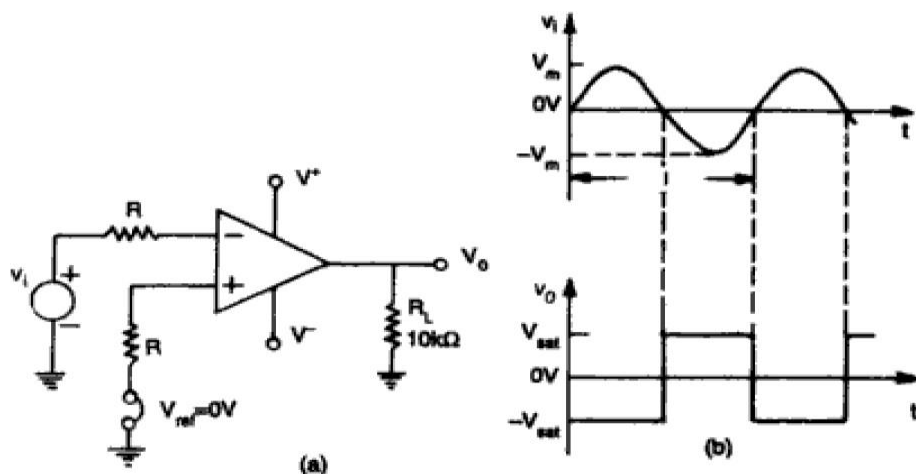


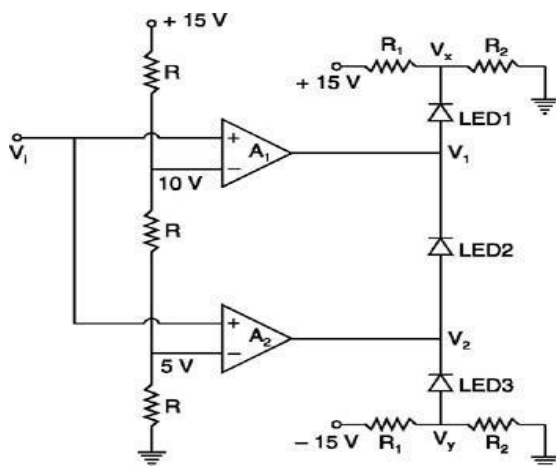
Fig. 5.4 (a) Zero crossing detector (b) Input and output waveforms

Window Detector:

A **window detector** determines when an unknown input is between two threshold levels.

There are three indicators: Yellow (LED 3) for input too low ($< 3V$), Green (LED 2) for safe input ($3 - 6V$) and Red (LED 1) for high input ($> 6V$). They are turned **on** and **off** as indicated in Table 5.1.

Input (volts)	Yellow LED 3	Green LED 2	Red LED 1
Less than 3 V	On	Off	Off
Between 3 V and 6 V	Off	On	Off
Greater than 6V	Off	Off	On



Schmitt Trigger:

Schmitt trigger is a **regenerative comparator**. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform. The input voltage is applied to the (-) input terminal and feedback v_o to the (+) input terminal. The i/p v_i triggers the output v_o levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}). The hysteresis width is the difference between these two threshold voltages i.e.

$$V_{UT} - V_{LT}$$

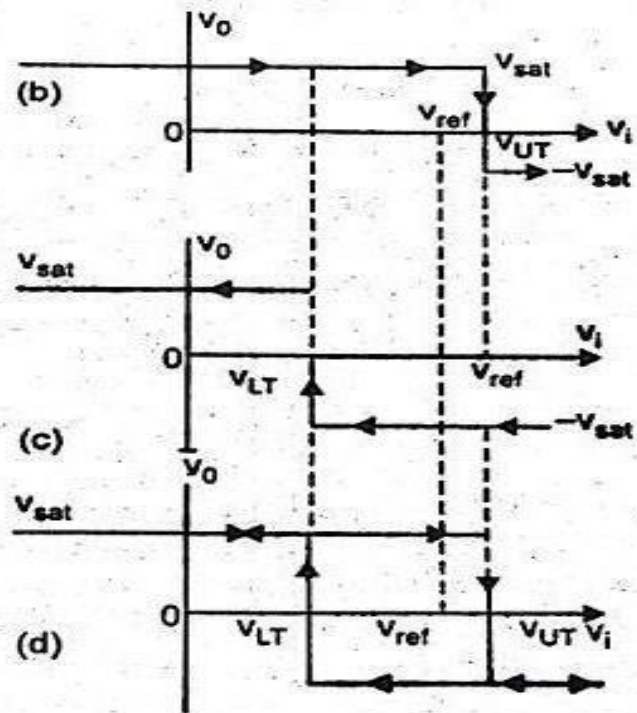
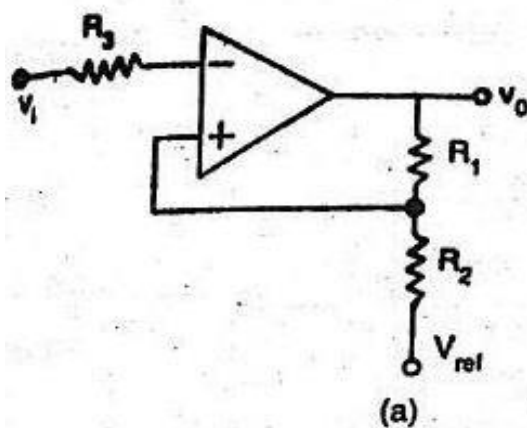


Fig. 5.8 (a) An inverting Schmitt trigger (b, c) Transfer characteristics for v_i increasing and v_i decreasing (d) composite input-output curve

These threshold voltages are calculated as,

- The output $v_o = +V_{sat}$. The voltage at (+) input terminal will be

$$V_{ref} + \frac{R_2}{R_1 + R_2} (V_{sat} - V_{ref}) = V_{UT} \quad \text{---(1)}$$

This voltage is called upper threshold voltage V_{UT} .

- For $v_0 = -V_{sat}$. The voltage at (+) input terminal will be

$$V_{ref} - \frac{R_2}{R_1 + R_2} (V_{sat} + V_{ref}) = V_{LT} \quad \dots\dots(2)$$

This voltage is referred to as lower threshold voltage V_{LT} .

$V_{LT} < V_{UT}$ and the difference between these two voltages is the hysteresis width V_H and can be written as

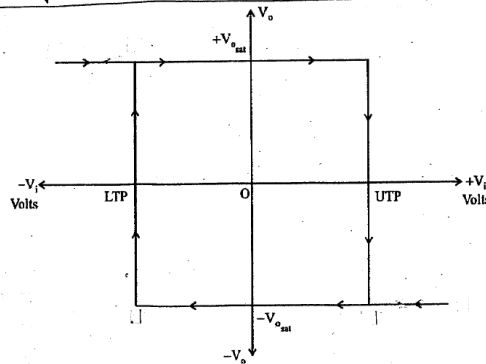
$$V_H = V_{UT} - V_{LT} = \frac{2 R_2 V_{sat}}{R_1 + R_2} \quad \dots\dots(3)$$

In the circuit of Fig.(a), V_{ref} is chosen as zero volt, it follows equ. 1 and 2 that

$$V_{UT} = -V_{LT} = R_2 V_{sat} / R_1 + R_2 \quad \dots\dots(4)$$

An input sinusoid of frequency $f = 1/T$ is applied to a comparator; a symmetrical square wave is obtained at the output.

Input / output characteristics or Transfer characteristics :



Schmitt trigger circuit design :-

- * The current I_2 flowing through the resistors R_1 & R_2 is chosen to be 100 times $I_B(max)$.

$$\text{i.e. } I_2 = 100 I_B(max)$$

- * $R_2 = \frac{\text{triggering voltage}}{I_2}$

- * $R_1 = \frac{V_o - \text{triggering voltage}}{I_2}$

NOTE : WKT. $V_{ref} = I_2 R_2$

$$* R_2 = \frac{V_{ref}}{I_2}$$

* Applying KVL from o/p V_0 , R_1 & R_2 , we get

$$V_0 - I_2 R_1 - V_{ref} = 0.$$

$$V_0 - V_{ref} = I_2 R_1.$$

$$\therefore R_1 = \frac{V_0 - V_{ref}}{I_2}$$

FORMULAE :-

for equal UTP & LTP i.e., $UTP = LTP$

1) let $I_2 = 100 \times I_{B(max)}$

2) $UTP = V_{R2}$

3) $R_2 = \frac{V_{R2}}{I_2}$

4) Applying KVL from V_0 , R_1 & R_2

$$V_0 - I_2 R_1 - I_2 R_2 = 0$$

$$V_0 - I_2 R_1 - V_{R2} = 0.$$

$$I_2 R_1 = V_0 - V_{R2}$$

$$R_1 = \frac{V_0 - V_{R2}}{I_2}$$

$$V_0 = +V_{sat}$$

$$R_1 = \frac{V_{sat} - V_{R2}}{I_2}$$

1) Using a 741 op-amp with a supply of $\pm 12V$, design an INV-Schmitt triggering circuit to have trigger points of $\pm 2V$.

Given:- $V_{cc} = +12V$, $V_{sat} = 12V$, $UTP = LTP = 2V$.

sol:- for 741 op-amp: $I_B(max) = 500nA$

* let $I_2 = 100 \times I_B(max) = 100 \times 500nA$

$$I_2 = 50\mu A$$

* $V_{R2} = UTP = 2V$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{2V}{50\mu A} = 40K\Omega$

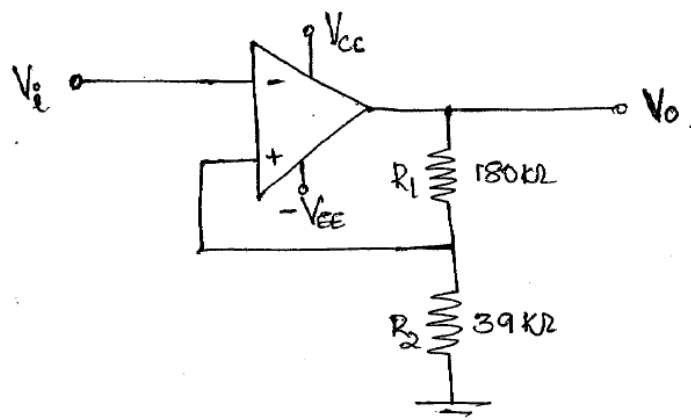
choose $R_2 = 39K\Omega$

Now, $I_2 = \frac{V_{R2}}{R_2} = \frac{2V}{39K\Omega}$

$$I_2 = 51.3\mu A$$

* $R_1 = \frac{V_{sat} - V_{R2}}{I_2} = \frac{12 - 2}{51.3\mu A} = 175\Omega$

choose $R_1 = 180\Omega$

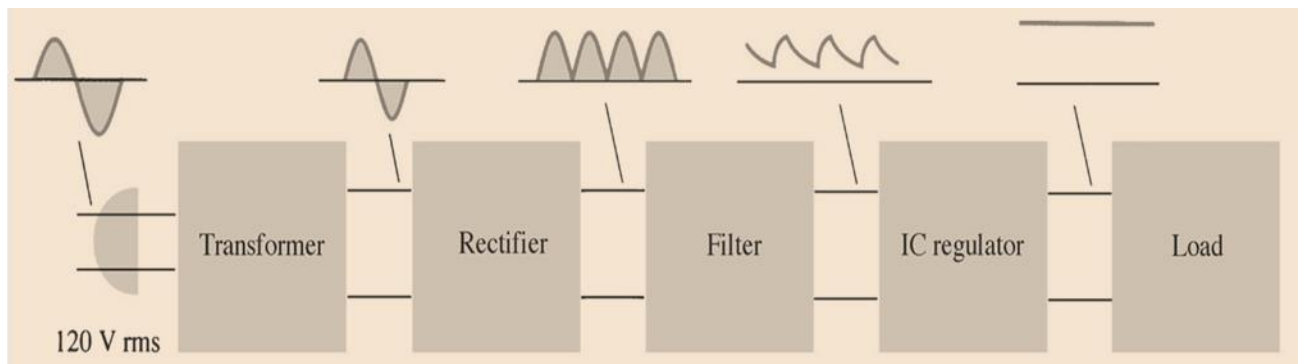


VOLTAGE REGULATORS

INTRODUCTION:

“A voltage regulator is an electronic circuit that provides a constant DC output voltage independent of the load current, temperature and ac line voltage variations.”

Batteries are often shown on a schematic diagram as the source of DC voltage but usually the actual DC voltage source is a power supply. There are many types of power supply. Most are designed to convert high voltage AC mains electricity to a suitable low voltage supply for electronic circuits and other devices. A more reliable method of obtaining DC power is to transform, rectify, filter and regulate an AC line voltage. A power supply can be broken down into a series of blocks, each of which performs a particular function.

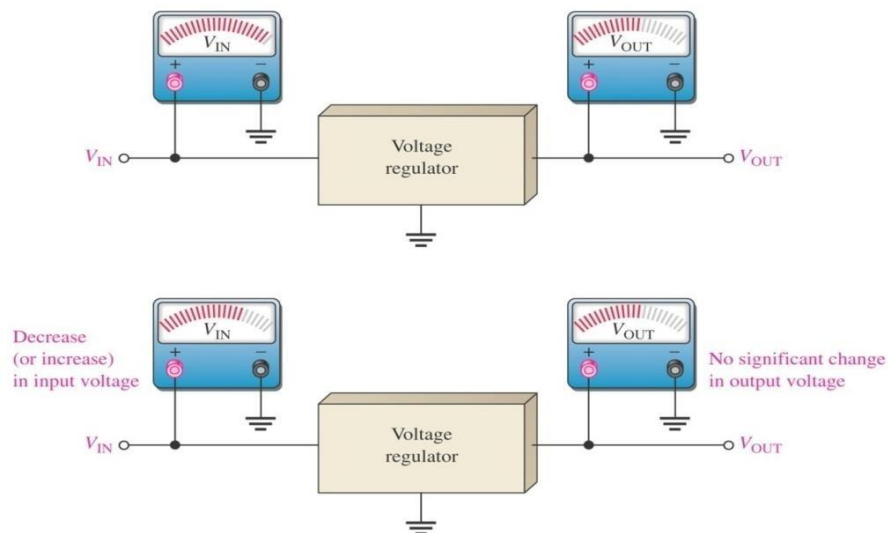


- **Power supply:** a group of circuits that convert the **standard ac voltage** (120 V, 60 Hz) provided by the wall outlet to **constant dc voltage**
- **Transformer :** a device that step up or step down the **ac voltage** provided by the wall outlet to a desired amplitude through the *action* of a *magnetic field*
- **Rectifier:** a diode circuits that converts the **ac input voltage** to a **pulsating dc voltage**
- The pulsating dc voltage is **only suitable** to be used as a battery charger, but **not good enough** to be used as a dc power supply in a radio, stereo system, computer and so on.
- There are two basic types of rectifier circuits:
 - Half-wave rectifier
 - Full-wave rectifier - Center-tapped & Bridge full-wave rectifier
- In summary, a full-wave rectified signal has **less ripple** than a half-wave rectified signal and is thus better to apply to a filter.

- **Filter:** a circuit used to reduce the fluctuation in the rectified output voltage or ripple. This provides a **steadier** dc voltage.
- **Regulator:** a circuit used to produce a **constant** dc output voltage by reducing the ripple to negligible amount. One part of power supply.

Voltage Regulation:

- Two basic categories of voltage regulation are:
 - ☐ line regulation
 - ☐ load regulation
- The purpose of **line regulation** is to maintain a nearly constant output voltage when the **input voltage** varies.
- The purpose of **load regulation** is to maintain a nearly constant output voltage when the **load** varies



Line regulation: A change in input (line) voltage does not significantly affect the output voltage of a regulator (within certain limits)

Line regulation can be defined as the percentage change in the output voltage for a given change in the input voltage.

$$\text{Line regulation} = \left(\frac{\Delta V_{OUT}}{\Delta V_{IN}} \right) \times 100\%$$

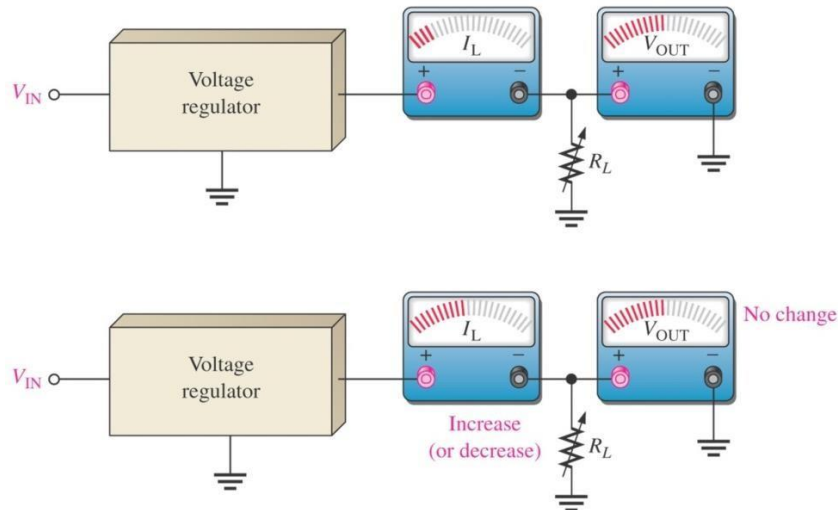
Δ means "a change in"

Line regulation can be calculated using the following formula:

$$\text{Line regulation} = \frac{(\Delta V_{OUT} / V_{OUT}) \times 100\%}{\Delta V_{IN}}$$

Load Regulation:

Load regulation: A change in load current (due to a varying R_L) has practically no effect on the output voltage of a regulator (within certain limits)



- Load regulation can be defined as the percentage change in the output voltage from no-load (NL) to full-load (FL).

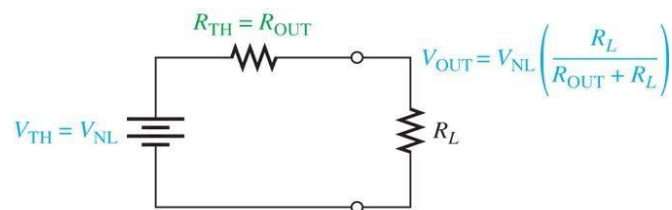
$$\text{Load regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}} \right) \times 100\%$$

Where:

V_{NL} = the no-load output voltage

V_{FL} = the full-load output voltage

- Sometimes power supply manufacturers specify the equivalent output resistance (R_{out}) instead of its load regulation.



- R_{FL} equal the smallest-rated load resistance, then V_{FL} :

$$V_{FL} = V_{NL} \left| \left(\frac{R_{FL}}{R_{OUT} + R_{FL}} \right) \right|$$

Rearrange the equation:

$$V_{NL} = V_{FL} \left(\frac{R_{OUT} - R_{FL}}{R_{FL}} \right)$$

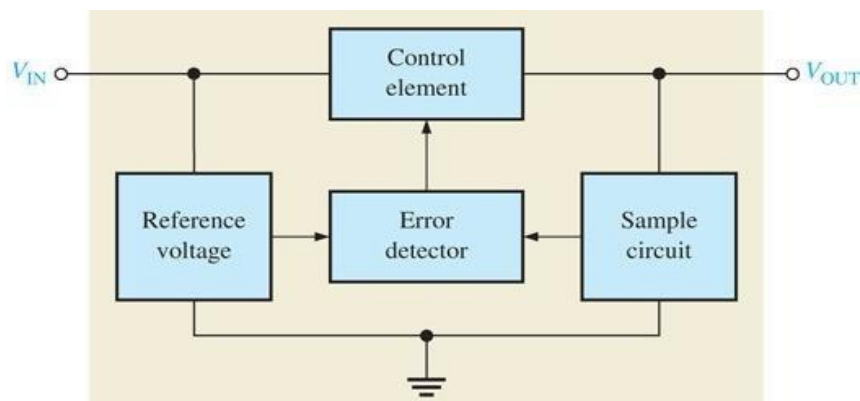
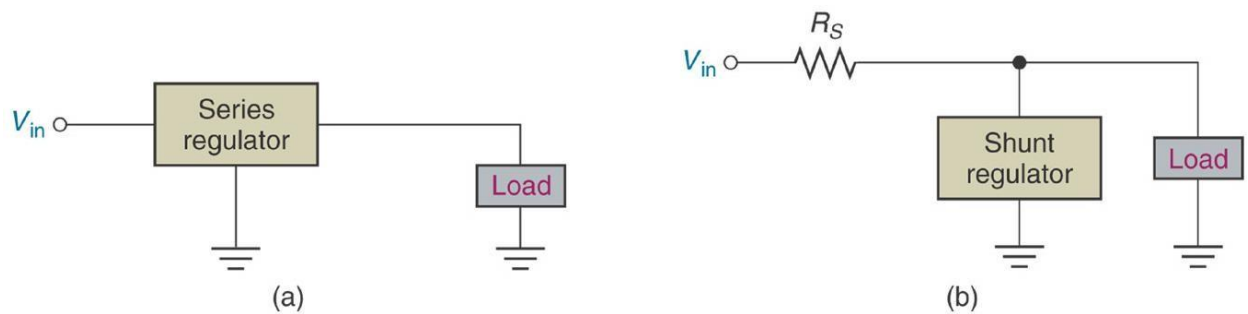
$$\text{Load regulation} = \frac{V_{FL} \left(\frac{R_{OUT} - R_{FL}}{R_{FL}} \right) - V_{FL}}{-V_{FL}} \times 100\%$$

$$\text{Load regulation} = \left(\frac{R_{OUT} - R_{FL}}{R_{FL}} - 1 \right) \times 100\%$$

$$\text{Load regulation} = \left(\frac{R_{OUT}}{R_{FL}} \right) \times 100\%$$

Types of Regulator:

- Fundamental classes of voltage regulators are **linear regulators** and **switching regulators**.
- Two basic types of linear regulator are the **series regulator** and the **shunt regulator**.
- The series regulator is connected in series with the load and the shunt regulator is connected in parallel with the load.



- **Control element** in series with load between input and output.
- Output **sample circuit** senses a change in output voltage.
- **Error detector** compares sample voltage with reference voltage $\rightarrow$ causes control element to compensate in order to maintain a constant output voltage.

Op-Amp Series Regulator:

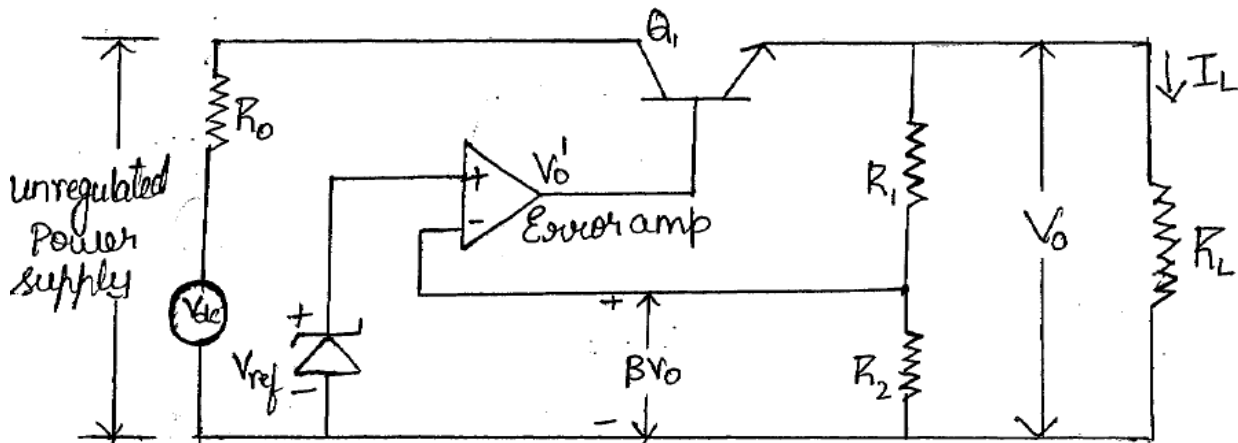


fig ① shows a regulated power supply. The ckt consists of four major components.

- 1) Reference voltage ' V_{ref} ' [Zener diode]
- 2) Error amplifier [Difference amplifier]
- 3) Series pass transistor [Q_1]
- 4) Feedback network [R_1 & R_2]

The power transistor Q_1 is in series with the unregulated dc voltage ' V_{in} ' and the regulated o/p voltage ' V_o '. Any variation in o/p voltage is absorbed by this transistor.

• The transistor Q_1 connected as an emitter follower and therefore provide sufficient current gain to drive the load.

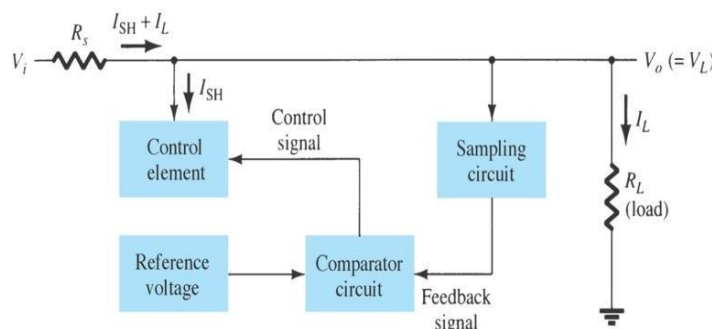
The o/p voltage is sampled by potential divider R_1 and R_2 [feedback $N(w)$] and fed back to the INV input terminal of the op-amp error amplifier.

• The sampled voltage is compared with the reference voltage V_{ref} . The o/p ' V_o ' of the error amplifier drives the series transistor Q_1 .

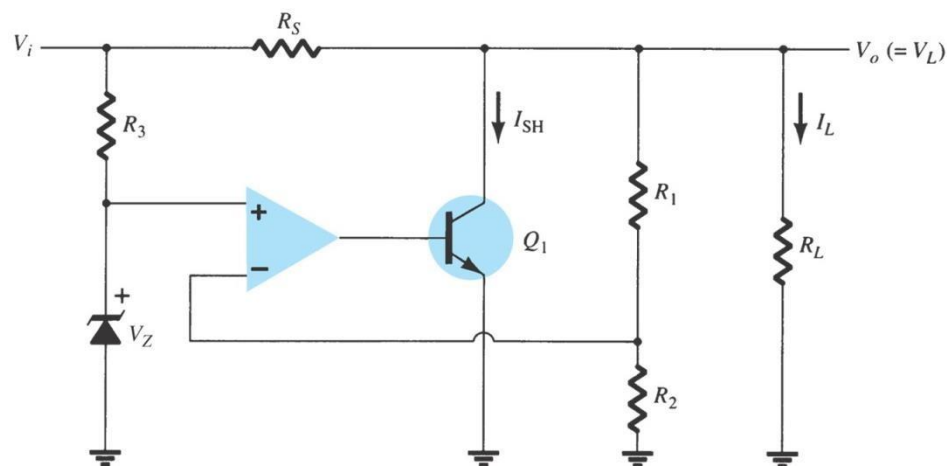
- The error amplifier compares the feedback voltage with a Zener diode reference voltage.
- The resulting difference voltage causes the transistor Q_1 controls the conduction to compensate the variation of the output voltage.
- The output voltage will be maintained at a constant value of:

$$V_o = \left(1 + \frac{R_1}{R_2}\right) V_Z$$

Shunt Regulator Circuit



- The unregulated input voltage provides current to the load.
- Some of the current is pulled away by the **control element**.
- If the load voltage tries to change due to a change in the load resistance, the **sampling circuit** provides a feedback signal to a **comparator**.
- The resulting difference voltage then provides a control signal to vary the amount of the current shunted away from the load to maintain the regulated output voltage across the load.



- When the output voltage tries to decrease due to a change in input voltage or load current caused by a change in load resistance, the decrease is sensed by R_1 and R_2 .
- A feedback voltage obtained from voltage divider R_1 and R_2 is applied to the op-amp's non-inverting input and compared to the Zener voltage to control the drive current to the transistor.

The current through resistor R_S is thus controlled to drop a voltage across R_S so that the output voltage is maintained

Features of 723 Regulators:

- It has wide variety of applications such as series, shunt, switching and floating regulators.
- Relative simplicity with power supply can be designed.
- It has small in size and lower in cost.
- Input voltage is maximum 40 V.
- Output voltage adjustable from 2 V to 37 V.
- Output current up to 150 mA without external pass transistor.

- Load and line regulations of 0.03%.
- It operates in positive or negative supply operation.
- It has choice of supply voltage.
- Low standby current gain.
- Very low temperature drift and high ripple rejection.
- Built in fold back current limiting.

Three terminal Voltage Regulator:

* IC voltage regulator replaces discrete component CKTs op-amp regulator with IC, which gives low cost, high reliability, reduction in size & excellent performance.

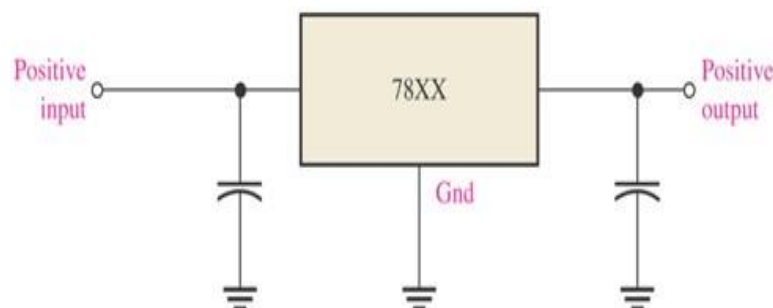
Eg: i) 78XX / 79XX Fixed voltage series regulators
 ii) 723 general purpose regulators.

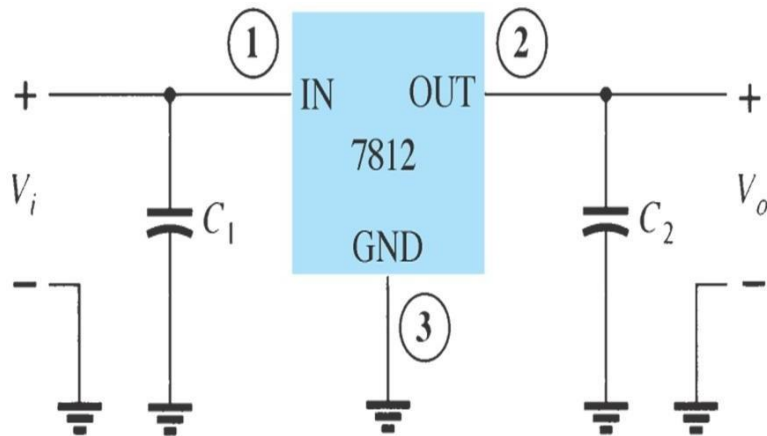
Fixed Voltage Series Regulator:

The fixed voltage regulator has an unregulated dc input voltage V_i applied to one input terminal, a regulated output dc voltage V_o from a second terminal, and the third terminal connected to ground.

Fixed-Positive Voltage Regulator:

The series 78XX regulators are the three-terminal devices that provide a fixed positive output voltage.





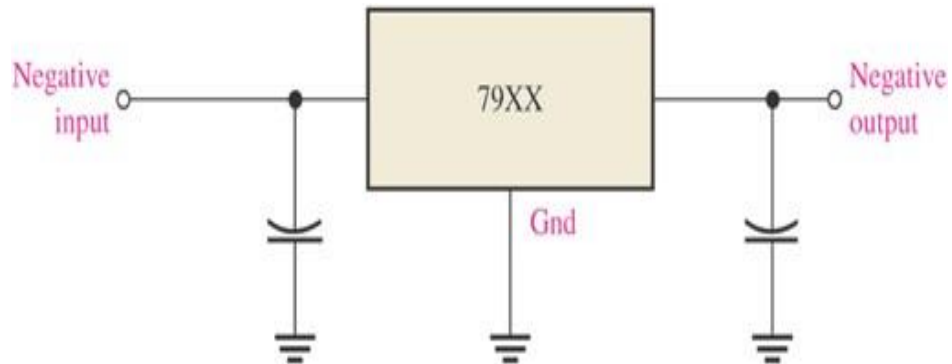
- An unregulated input voltage V_i is filtered by a capacitor C_1 and connected to the IC's IN terminal.
- The IC's OUT terminal provides a regulated +12 V, which is filtered by capacitor C_2 .
- The third IC terminal is connected to ground (GND)

Positive-Voltage Regulators in the 78XX Series:

IC Part	Output Voltage (V)	Minimum V_i (V)
7805	+5	+7.3
7806	+6	+8.3
7808	+8	+10.5
7810	+10	+12.5
7812	+12	+14.5
7815	+15	+17.7
7818	+18	+21.0
7824	+24	+27.1

Fixed-Negative Voltage Regulator

- The series 79XX regulators are the three-terminal IC regulators that provide a fixed negative output voltage.
- This series has the same features and characteristics as the series 78XX regulators except the pin numbers are different.

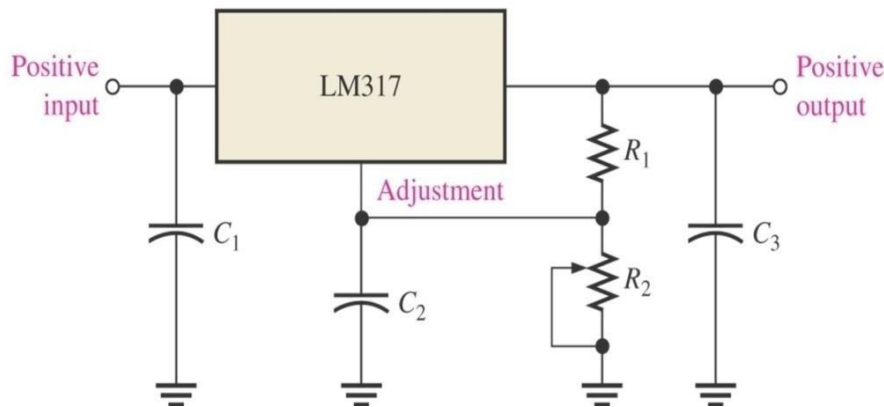


Negative-Voltage Regulators in the 79XX Series:

IC Part	Output Voltage (V)	Minimum V_i (V)
7905	-5	-7.3
7906	-6	-8.4
7908	-8	-10.5
7909	-9	-11.5
7912	-12	-14.6
7915	-15	-17.7
7918	-18	-20.8
7924	-24	-27.1

Adjustable-Voltage Regulator:

- Voltage regulators are also available in circuit configurations that allow to set the output voltage to a desired regulated value.
- The LM317 is an example of an adjustable-voltage regulator, can be operated over the range of voltage from 1.2 to 37 V.



Characteristics of IC integrators:

There are four characteristics of three terminal IC regulators:

1) V_o : [Regulated o/p voltage]

The regulated o/p voltage is fixed at a value as specified by the manufacturer.

There are various models available with different o/p voltages.

Eg: 78XX series has o/p voltage at 5, 6, 8, 12, 15, 18V etc

3) $|V_{in}| \geq |V_o| + 2 \text{ volts}$:

The unregulated input voltage must be at least 2V more than the regulated o/p voltage.

for example, if $V_o = 5V$, then $V_{in} = 7V$

3) Maximum o/p current ' $I_o(\text{max})$ ':

The load current may vary from '0' to rated maximum o/p current. The IC is usually provided with a heat sink, otherwise it may not provide the rated maximum o/p current.

4) Thermal Shutdown:

The IC has a built-in temperature sensor which turn-off the IC when it becomes too hot. The o/p current will drop and remains there until the IC has cooled significantly.

Limitations:

1) No short ckt protection

2) O/p voltage is fixed

Advantages of IC voltage Regulators:

• Easy to use

• simplifies power supply design

• Low cost

• conveniently used for local regulations.

• over-current protection

• Thermal overload protection.

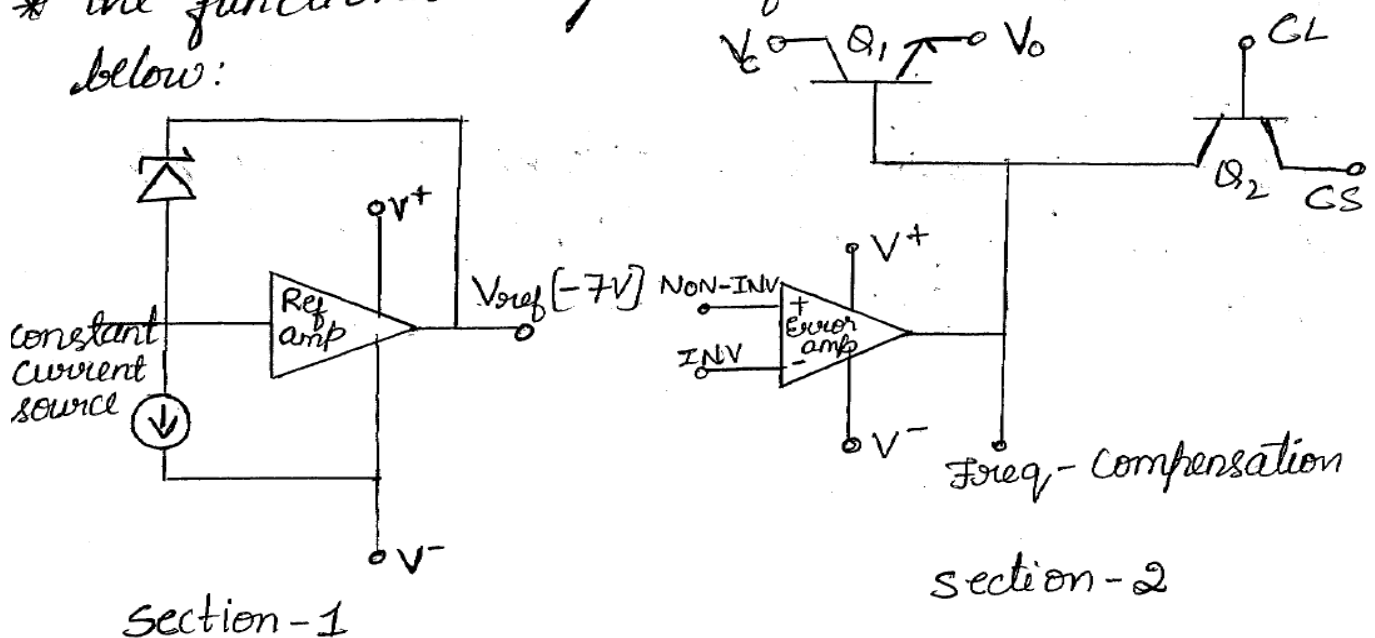
Demerits of 3-terminal IC regulators.

The three terminal IC regulators have the following limitation [drawback or demerits]

- > No short circuit protection
- > Output voltage is fixed [either +ve or -ve]

723 General purpose regulator :

- * IC 723 is a general purpose regulator, which can be adjusted over a wide range of both +ve & -ve regulated o/p voltage.
- * IC 723 has a limitation that it has no inbuilt thermal protection. It also has no short circuit limits
- * The functional diagram of IC 723 is as shown below:



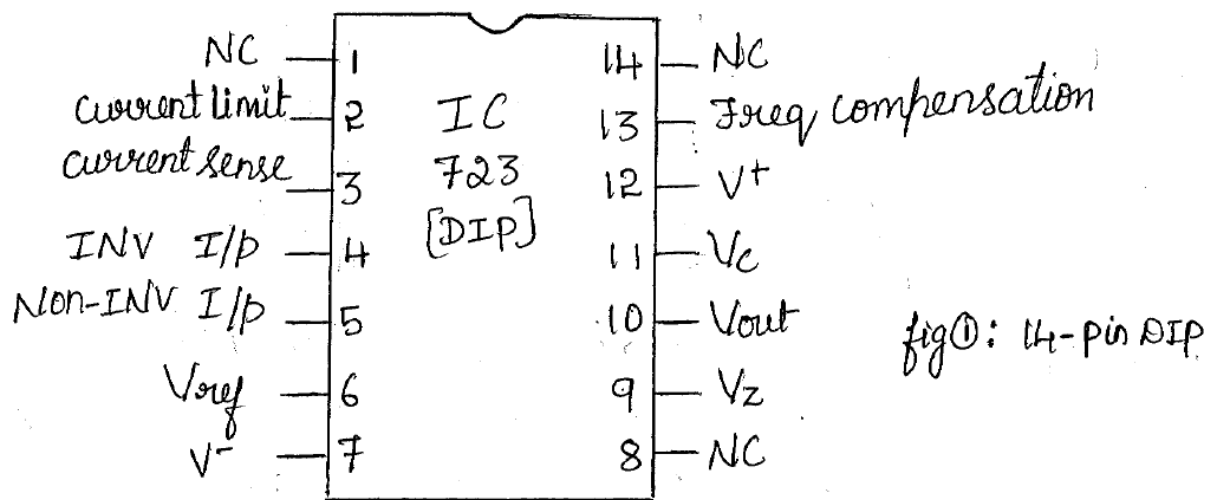
IC 723 has two sections. The section 1 has Zener diode, a constant current source & reference amplifier produces a fixed voltage of $7V$ at V_{ref} terminal.

The constant current source forces the Zener to operate at fixed point so that the Zener o/p's a fixed voltage.

The section-2 consists of an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2 .

The error amplifier compares a sample of the i/p voltage applied at the INV terminal with that of reference voltage [V_{ref}] applied at the Non-INV terminal.

The error signal controls the conduction of Q_1 . These two sections are internally not connected but are available for 723 IC regulator.



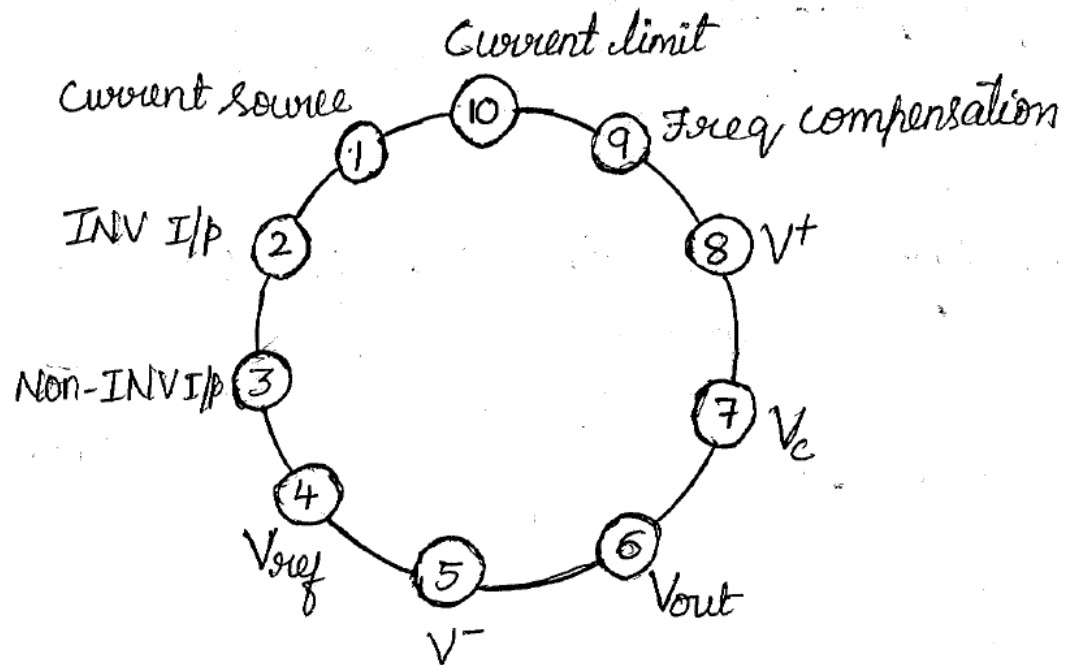


fig ②: 10-pin metal-can package

UNIT-II

OP-AMP, IC-555 & IC 565 APPLICATIONS

Introduction to Active Filters, Characteristics of Band pass, Band reject and All Pass Filters. Analysis of 1st order LPF & HPF Butterworth Filters, waveform Generators - Triangular, Sawtooth, Square wave.

IC555 Timer – Functional Diagram, Mono stable and Astable Operations, Applications. **IC565 PLL** - Block Schematic, Description of Individual Blocks, applications.

Introduction to Active Filters:

Filters are circuits that are capable of passing signals within a band of frequencies while rejecting or blocking signals of frequencies outside this band. This property of filters is also called “frequency selectivity”.

There are two broad categories of filters:

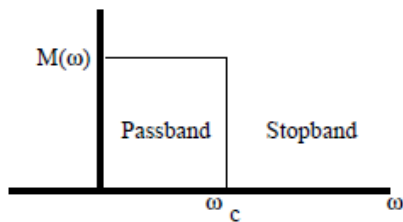
- An *analog filter* processes continuous-time signals
- A *digital filter* processes discrete-time signals.

The analog or digital filters can be subdivided into four categories:

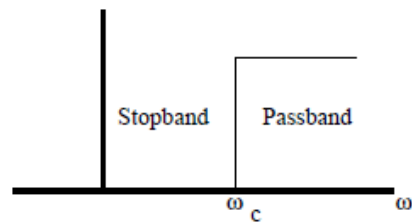
1. Lowpass Filters
2. Highpass Filters
3. Bandstop Filters
4. Bandpass Filters

Ideal Filters:

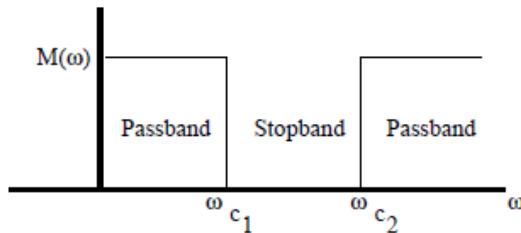
Lowpass Filter



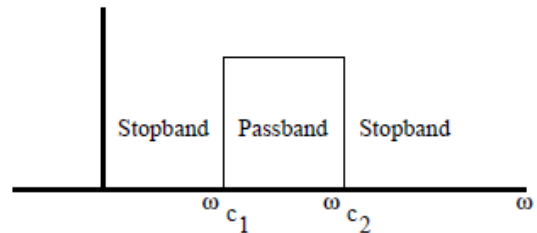
Highpass Filter



Bandstop Filter



Bandpass Filter



Filter can be also be categorized as passive or active:

Passive filters: The circuits built using RC, RL, or RLC circuits.

Active filters: The circuits that employ one or more op-amps in the design in addition to resistors and capacitors.

Passive filters use resistors, capacitors, and inductors (RLC networks). To minimize distortion in the filter characteristic, it is desirable to use inductors with high quality factors. Practical inductor includes a series resistance. They are particularly non-ideal, they are bulky and expensive.

Active filters overcome these drawbacks and are realized using resistors, capacitors, and active devices (usually op-amps) which can all be integrated: Active filters replace inductors using op-amp based equivalent circuits.

Advantages of active RC filters include:

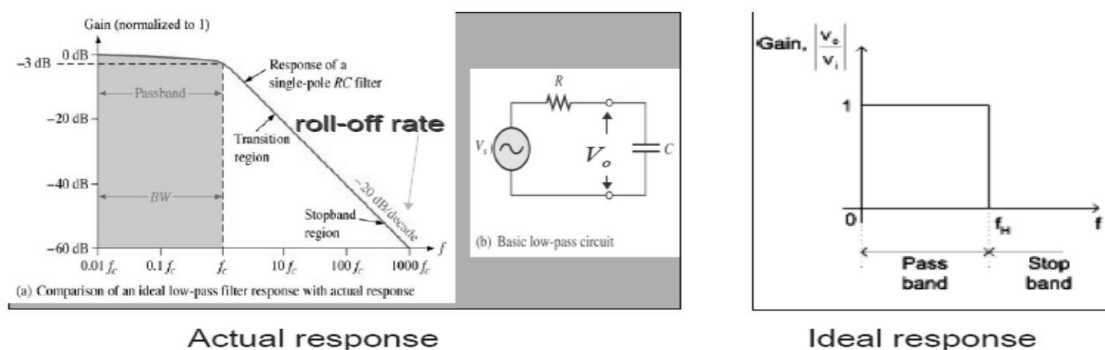
- Reduced size and weight
- Increased reliability and improved performance
- Simpler design than for passive filters and can realize a wider range of functions as well as providing voltage gain
- In large quantities, the cost of an IC is less than its passive counterpart.

Active RC filters also have some disadvantages:

- Limited bandwidth of active devices limits the highest attainable frequency (passive RLC filters can be used up to 500 MHz)
- Require power supplies (unlike passive filters)
- Increased sensitivity to variations in circuit parameters caused by environmental changes compared to passive filters.

Low pass filter:

A low-pass filter is a filter that passes frequencies from 0Hz to critical frequency, f_c and significantly attenuates all other frequencies.



The **bandwidth** of an **ideal** low-pass filter is equal to f_c :

$$BW = f_c$$

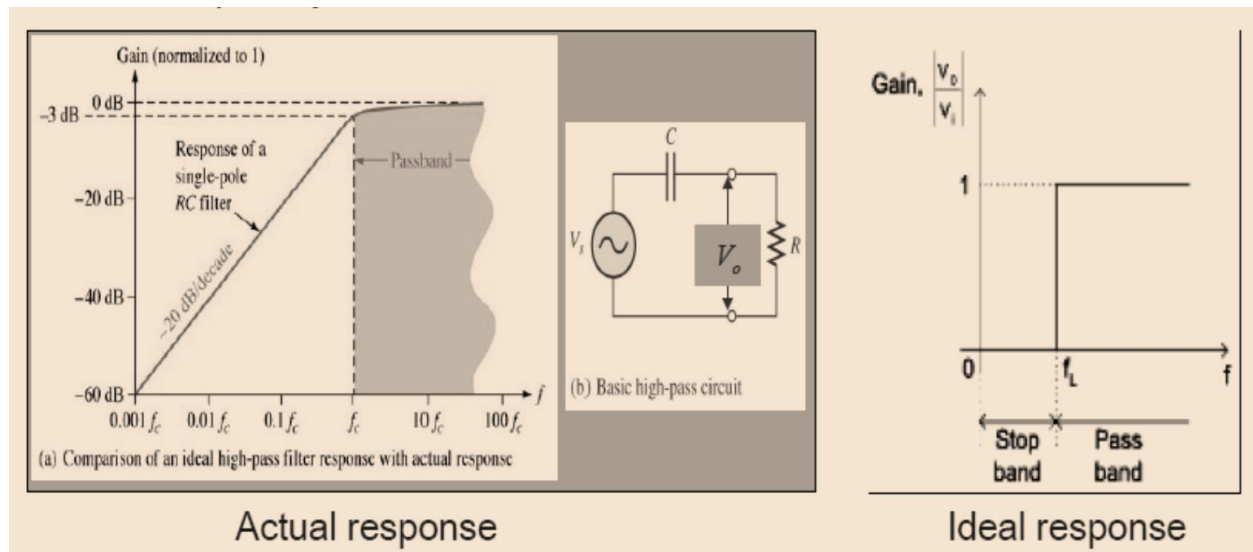
The critical frequency of a low-pass RC filter occurs when

$X_c = R$ and can be calculated using the formula below:

$$f_c = \frac{1}{2\pi RC}$$

High Pass Filter:

A high-pass filter is a filter that significantly attenuates or rejects all frequencies below f_c and passes all frequencies above f_c . The pass band of a high-pass filter is all frequencies above the critical frequency.



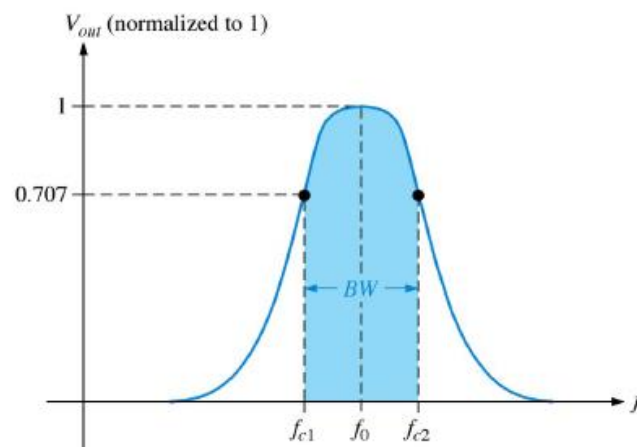
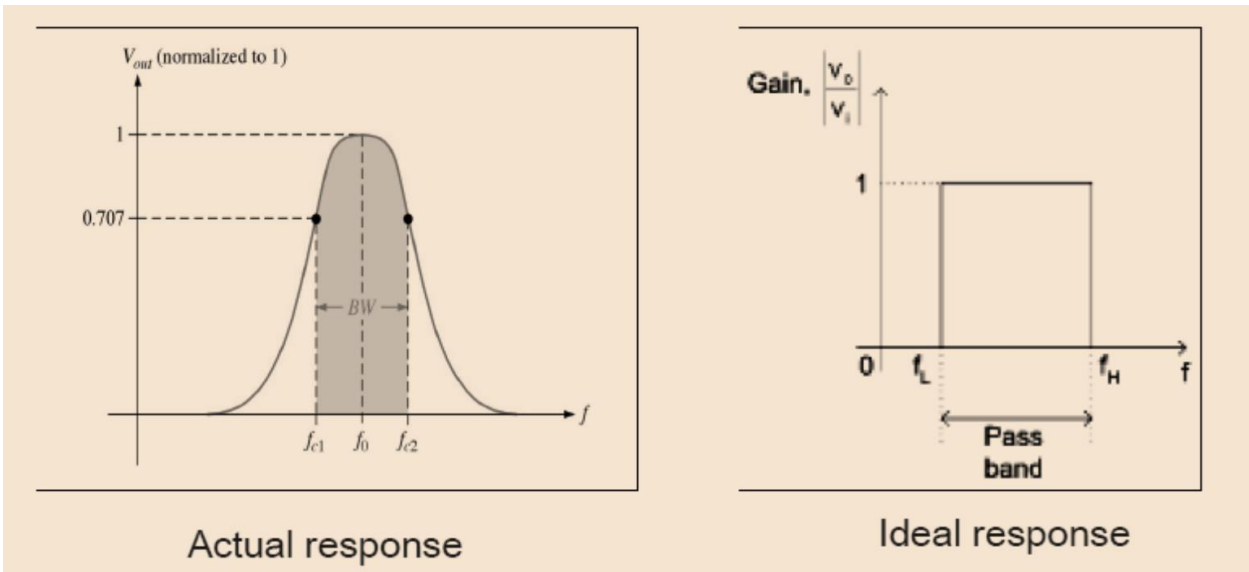
The critical frequency of a high-pass RC filter occurs when

$X_c = R$ and can be calculated using the formula below:

$$f_c = \frac{1}{2\pi RC}$$

Band Pass Filter:

A band-pass filter passes all signals lying within a band between a lower-frequency limit and upper-frequency limit and essentially rejects all other frequencies that are outside this specified band.



The bandwidth (BW) is defined as the difference between the upper critical frequency (f_{c2}) and the lower critical frequency (f_{c1}).

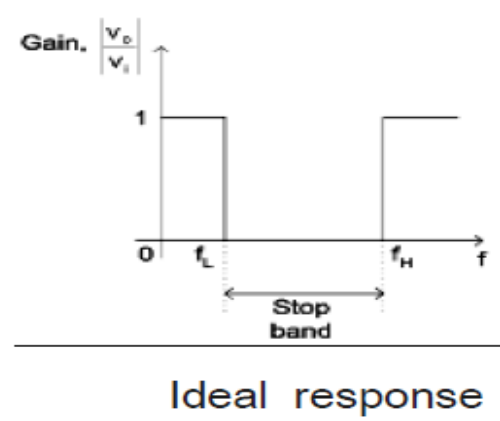
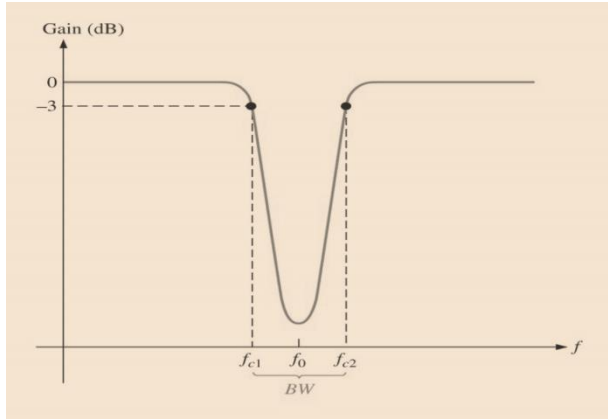
$$BW = f_{c2} - f_{c1}$$

The frequency about which the pass band is centered is called the center frequency, f_0 and defined as the geometric mean of the critical frequencies.

$$f_o = \sqrt{f_{c1}f_{c2}}$$

Band Stop Filter:

Band-stop filter is a filter which its operation is opposite to that of the band-pass filter because the frequencies within the bandwidth are rejected, and the frequencies above f_{c1} and f_{c2} are passed.



First order Low pass Butterworth Filter:

Butterworth filter is a type of filter whose frequency response is flat over the pass band region. Low-pass filter (LPF) provides a constant output from DC up to a cutoff frequency $f_{(H)}$ and rejects all signals above that frequency.

The first order low pass butter worth filter is realized by R-C circuit used along with an op-amp, used in the non inverting configuration.

The circuit diagram is shown in Fig. This also called one pole low pass butter worth filter.

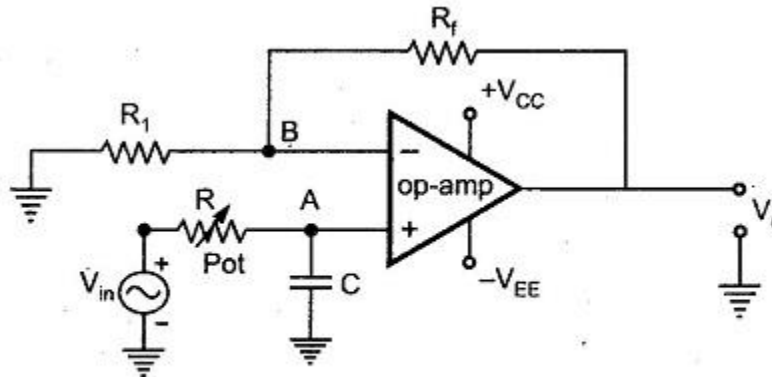


Fig. 2.74 First order low pass butterworth filter

Analysis of the Filter Circuit:

The impedance of the capacitor C is $-j X_c$ where X_c is the capacitive reactance given by

$$X_c = \frac{1}{2\pi f C}$$

By the potential divider rule, the voltage at the non inverting input terminal A which is the voltage across capacitor C is given by,

$$V_A = \frac{-j X_c}{R - j X_c} \cdot V_{in} \quad \dots (1)$$

$$\begin{aligned} V_A &= \frac{-j \left(\frac{1}{2\pi f C} \right)}{R - j \left(\frac{1}{2\pi f C} \right)} \cdot V_{in} = \frac{-j}{2\pi f R C - j} \cdot V_{in} \\ &= \frac{V_{in}}{1 - \frac{2\pi f R C}{j}} \end{aligned}$$

$$-j = \frac{1}{j} \quad \text{and} \quad -\frac{1}{j} = j$$

$$V_A = \frac{V_{in}}{1 + j 2\pi f R C} \quad \dots (2)$$

As the op-amp is in the non inverting configuration,

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_A \quad \dots (3)$$

$$V_o = \left(1 + \frac{R_f}{R_i}\right) \frac{V_{in}}{(1 + j 2 \pi f R C)}$$

$$\frac{V_o}{V_{in}} = \frac{A_F}{1 + j \left(\frac{f}{f_H}\right)} \quad (4)$$

$$A_F = \left(1 + \frac{R_f}{R_i}\right) = \text{gain of filter in pass band} \quad \dots (5)$$

$$f_H = \frac{1}{2 \pi R C} = \text{high cut off frequency of filter} \quad \dots (6)$$

f = operating frequency

$\frac{V_o}{V_{in}}$ is the transfer function of the filter and can be expressed in the polar V in – form as,

$$\frac{V_o}{V_{in}} = \left| \frac{V_o}{V_{in}} \right| \angle \phi$$

$$\left| \frac{V_o}{V_{in}} \right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} \quad \dots (7)$$

$$\phi = -\tan^{-1} \left(\frac{f}{f_H} \right) \quad \dots (8)$$

The phase angle Φ is in degrees. The equation (7) describes the behavior of the low pass filter.

1. At very low frequencies, $f < f_H$

$$\left| \frac{V_o}{V_{in}} \right| \cong A_F \text{ i.e. constant}$$

2. At $f = f_H$,

$$\left| \frac{V_o}{V_{in}} \right| = \frac{A_F}{\sqrt{2}} = 0.707 A_F \text{ i.e. 3 dB down to the level of } A_F.$$

3. At $f > f_H$

$$\left| \frac{V_o}{V_{in}} \right| < A_F$$

Thus, for the range of frequencies, $0 < f < f_H$, the gain is almost constant equal to A_F which is high cut off frequency. At $f = f_H$, gain reduces to $0.707 A_F$ i.e. 3 dB down from A_F . And as the frequency increases than f_H , the gain decreases at a rate of 20dB/decade. The rate 20 dB/decade means decrease of 20 dB in gain per 10 times change in frequency.

The frequency f_H is called cut off frequency, break frequency, — 3dB frequency or corner frequency. The frequency response is shown in the Fig..

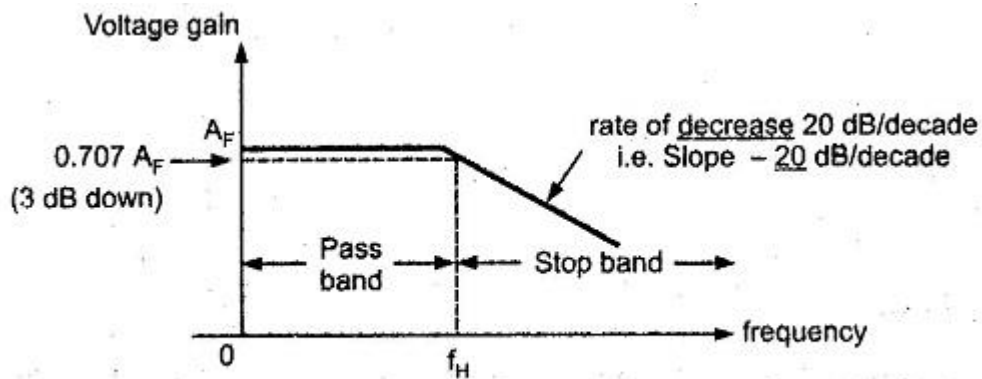


Fig. 2.75 Frequency response

The rate of decrease in gain is 20 dB/decade i.e. the decrease can be indicated by a negative slope in the frequency response, as -20 dB/decade.

The design steps for the first order low pass Butterworth filter are

- 1) Choose the cut off frequency, f_H .
- 2) Choose the capacitance C usually between 0.01 and $1 \mu F$. Generally, it is selected as $1 \mu F$ or less than that. For better performance, Mylar or tantalum capacitors are selected.

3) Now, for the RC circuit,

$$f_H = \frac{1}{2\pi RC}$$

Hence, as f_H and C are known, calculate the value of R .

- 4) The resistances R_f and R_1 can be selected depending on the required gain in the pass band.

$$A_F = 1 + \frac{R_f}{R_1}$$

Frequency Scaling:

Once the filter is designed, sometimes, it is necessary to change the value of cut-off frequency f_H . The method used to change the original cut-off frequency f_H to a new cut-off frequency f_{H1} is called as frequency scaling.

To achieve such a frequency scaling, the standard value capacitor C is selected first. The required cut-off frequency can be achieved by calculating corresponding value of resistance R . But to achieve frequency scaling a potentiometer is used as shown in Fig. 2.75. Thus, the resistance R is generally a potentiometer with which required cut-off frequency f_H can be adjusted and changed later on if required.

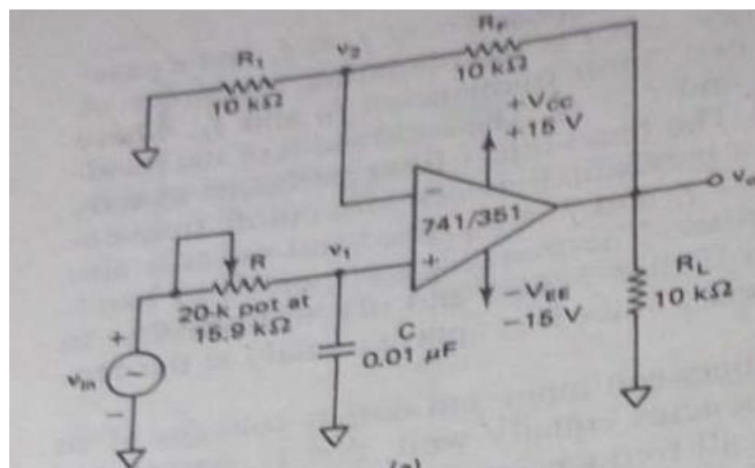
EXAMPLE 7-1

Design a low-pass filter at a cutoff frequency of 1 kHz with a passband gain of 2.

SOLUTION

Follow the preceding design steps.

1. $f_H = 1 \text{ kHz}$.
2. Let $C = 0.01 \mu\text{F}$.
3. Then $R = 1/(2\pi)(10^3)(10^{-8}) = 15.9 \text{ k}\Omega$. (Use a 20-k Ω potentiometer.)
4. Since the passband gain is 2, R_1 and R_F must be equal. Therefore, let $R_1 = R_F = 10 \text{ k}\Omega$. The complete circuit with component values is shown in Fig.



EXAMPLE 7-2

Using the frequency scaling technique, convert the 1-kHz cutoff frequency of the low-pass filter of Example 7-1 to a cutoff frequency of 1.6 kHz.

SOLUTION

To change a cutoff frequency from 1 kHz to 1.6 kHz, we multiply the 15.9-k Ω resistor by

$$\frac{\text{original cutoff frequency}}{\text{new cutoff frequency}} = \frac{1 \text{ kHz}}{1.6 \text{ kHz}} = 0.625$$

Therefore, new resistor $R = (15.9 \text{ k}\Omega)(0.625) = 9.94 \text{ k}\Omega$. However, 9.94 k Ω is not a standard value. Therefore, use $R = 10 \text{ k}\Omega$ potentiometer and adjust it to 9.94 k Ω . Thus the new cutoff frequency is

$$f_H = \frac{1}{(2\pi)(0.01 \mu\text{F})(9.94 \text{ k}\Omega)} = 1.6 \text{ kHz}$$

EXAMPLE 7-3

Plot the frequency response of the low-pass filter of Example 7-1.

SOLUTION

To plot the frequency response, we have to use Equation (7-2a). The data of Table 7-1 are, therefore, obtained by substituting various values for f in this equation. Equation (7-2a) will be repeated here for convenience:

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}}$$

where $A_F = 2$ and $f_H = 1 \text{ kHz}$. The data of Table 7-1 are plotted as shown in Figure 7-3.

TABLE 7-1 Frequency Response Data for Example 7-3.

Input frequency, f (Hz)	Gain magnitude, $ v_o/v_{in} $	Magnitude (dB) = $20 \log v_o/v_{in} $
10	2	6.02
100	1.99	5.98
200	1.96	5.85
700	1.64	4.29
1,000	1.41	3.01
3,000	0.63	-3.98
7,000	0.28	-10.97
10,000	0.20	-14.02
30,000	0.07	-23.53
100,000	0.02	-33.98

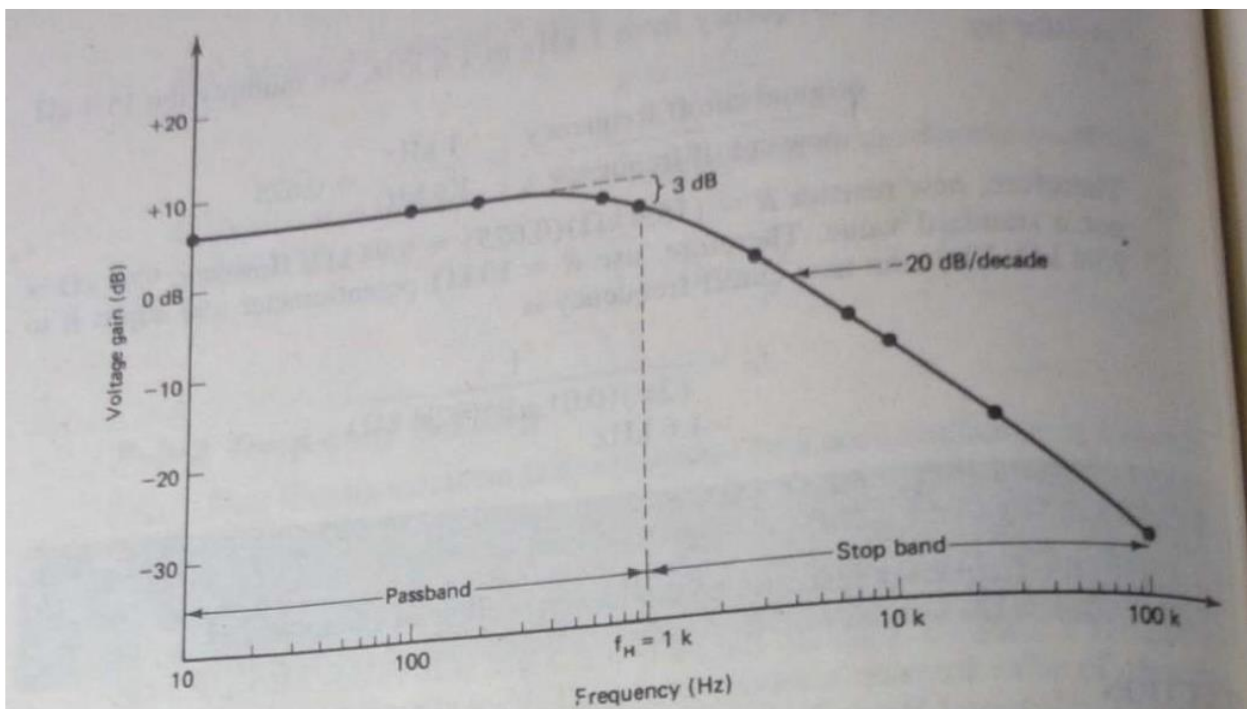


FIGURE 7-3 Frequency response for Example 7-3.

First Order High Pass Butterworth Filter:

A high pass filter is a circuit that attenuates all the signals below a specified cut off frequency denoted as f_L . Thus, a high pass filter performs the opposite function to that of low pass filter. Hence, the First Order High Pass Butterworth Filter circuit can be obtained **by interchanging frequency determining resistances and capacitors in low pass filter circuit.**

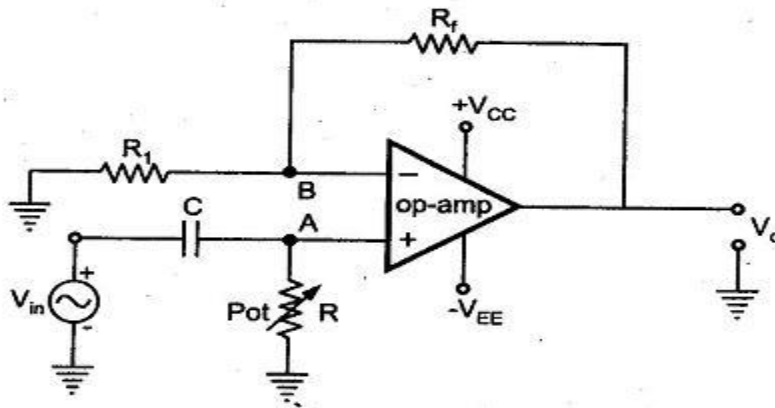


Fig. 2.79 First order high pass Butterworth filter

The first order high pass filter can be obtained by interchanging the elements R and C in a first order low pass filter circuit. The Fig. 2.79 shows the first order high pass Butterworth filter.

It can be observed that as compared to first order low pass filter (Fig. 2.74), the positions of R and C are changed in the high pass circuit shown in Fig. 2.79.

The frequency at which the gain is 0.707 times the gain of filter in pass band is called as low cut off frequency, and denoted as f_L . So, all the frequencies greater than f_L is allowed to pass but the maximum frequency which is allowed to pass is determined by the closed loop bandwidth of the op—amp used.

Analysis of the Filter Circuit:

The impedance of the capacitor is $-jX_C = -j \left(\frac{1}{2\pi fC} \right)$

where f is the input i.e. operating frequency.

By the voltage divider rule, the potential of the non inverting terminal of the op—amp is

$$V_A = V_{in} \left[\frac{R}{R - jX_C} \right] \quad \dots (1)$$

$$V_A = V_{in} \left[\frac{R}{-jX_C \left(\frac{R}{-jX_C} + 1 \right)} \right] \quad \text{taking } -jX_C \text{ outside}$$

$$-\frac{1}{j} = j, \text{ we can write,}$$

$$\frac{1}{-jX_C} = \frac{j}{X_C} = \frac{j}{\left(\frac{1}{2\pi fC} \right)} \\ = j 2\pi fC \quad \dots (2)$$

Substituting in the above expression of V_A ,

$$V_A = V_{in} \left[\frac{\left(-\frac{R}{jX_C} \right)}{\left(-\frac{R}{jX_C} \right) + 1} \right] \\ V_A = V_{in} \left[\frac{j 2\pi fRC}{1 + j 2\pi fRC} \right] \quad \dots (3)$$

This can be represented as

$$\therefore V_A = V_{in} \left[\frac{j \left(\frac{f}{f_L} \right)}{1 + j \left(\frac{f}{f_L} \right)} \right]$$

$$\text{where } f_L = \frac{1}{2\pi RC} = \text{low cut off frequency} \quad \dots (4)$$

Now, for the op-amp in non-inverting configuration,

$$V_o = A_F V_A$$

where

V_A = Voltage at the non inverting input

and

$A_F = \left(1 + \frac{R_f}{R_1}\right)$ = gain of op-amp in pass band

$$\therefore V_o = A_F V_{in} \left[\frac{j \left(\frac{f}{f_L} \right)}{1 + j \left(\frac{f}{f_L} \right)} \right]$$

$$\frac{V_o}{V_{in}} = A_F \left[\frac{j \left(\frac{f}{f_L} \right)}{1 + j \left(\frac{f}{f_L} \right)} \right] \quad \dots (5)$$

This is the required expression for the transfer function of the filter. For the frequency response, we require the magnitude of the transfer function which is given by,

$$\left| \frac{V_o}{V_{in}} \right| = \frac{A_F \left(\frac{f}{f_L} \right)}{\sqrt{1 + \left(\frac{f}{f_L} \right)^2}} \quad \dots (6)$$

The equation (6) describes the behavior of the high pass filter.

1) At low frequencies, i.e. $f < f_L$

$$\left| \frac{V_o}{V_{in}} \right| < A_F$$

2) At $f = f_L$,

$$\left| \frac{V_o}{V_{in}} \right| = 0.707 A_F \text{ i.e. 3 dB down from the level of } A_F$$

3) At $f > f_L$ i.e. high frequencies, 1 can be neglected as compared to $\left(\frac{f}{f_L} \right)$ from denominator.

$$\left| \frac{V_o}{V_{in}} \right| \cong A_F \text{ i.e. constant}$$

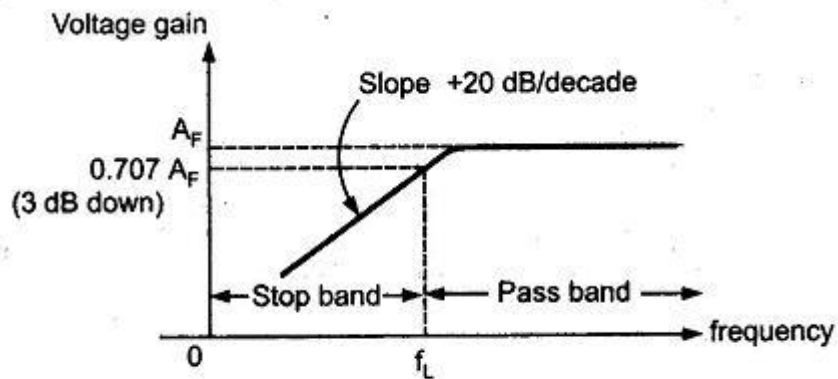


Fig. 2.80 Frequency response

Thus, the circuit acts as high pass filter with a pass band gain as A_F . For the frequencies, $f < f_L$, the gain increases till $f = f_L$ at a rate of $+20$ dB/decade. Hence, the slope of the frequency response in stop band is $+20$ dB/decade for first order high pass filter. The frequency response is shown in the Fig. 2.80.

Note: As high pass filter is basically a low pass filter circuit with positions of R and C interchanged, the design steps and the frequency scaling method discussed earlier for low pass filter is equally applicable to the first order high pass Butterworth filter.

EXAMPLE 7-5

- Design a high-pass filter at a cutoff frequency of 1 kHz with a passband gain of 2.
- Plot the frequency response of the filter in part (a).

SOLUTION

- Use the same values of R and C that were determined for the low-pass filter of Example 7-1, since $f_L = f_H = 1$ kHz. That is, $C = 0.01 \mu\text{F}$ and $R = 15.9 \text{ k}\Omega$. Similarly, use $R_1 = R_F = 10 \text{ k}\Omega$, since $A_F = 2$.
- The data for the frequency response plot can be obtained by substituting for the input frequency f values from 100 Hz to 100 kHz in Equation (7-6). These data are included in Table 7-3. Equation (7-6) is repeated here for convenience:

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_F(f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

where $A_F = 2$ and $f_L = 1$ kHz. The frequency response data of Table 7-3 are plotted in Figure 7-7. In the stopband (from 100 Hz to 1 kHz) the gain increases at the rate of 20 dB/decade. However, in the passband (after $f = f_L = 1$ kHz) the gain remains constant at 6.02 dB. Moreover, the upper-frequency limit of the passband is set by the closed-loop bandwidth of the op-amp.

High-Pass Filter of Example 7-5.

upper frequency
of the op-amp.

TABLE 7-3 Frequency Response Data for the First-Order High-Pass Filter of Example 7-5.

Frequency, f (Hz)	Gain magnitude, $ v_o/v_{in} $	Magnitude (dB) = $20 \log v_o/v_{in} $
		-14.02
	0.20	-8.13
100	0.39	-2.58
200	0.74	1.19
400	1.15	3.01
700	1.41	5.56
1,000	1.90	5.93
3,000	1.98	5.98
7,000	1.99	6.02
10,000	2	6.02
30,000	2	
100,000		

High-Pass Butterworth Filter

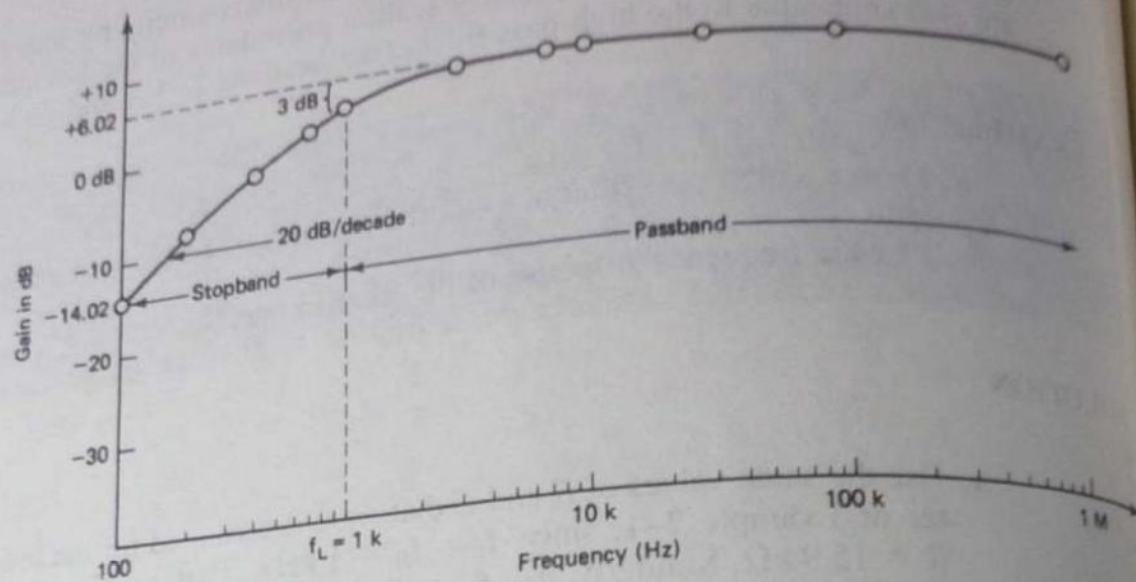


FIGURE 7-7 Frequency response for Example 7-5.

Band Pass Filter:

A Band Pass Filter Circuit designed to pass signals only in a certain band of frequencies while rejecting all signals outside this band.

There are basically two types of Band Pass Filter Circuit,

1. Wide band pass filter
2. Narrow band pass filter

A Band Pass Filter Circuit is defined as a wide band pass if its figure of merit or quality factor $Q < 10$. While there is no firm dividing line between the two, if $Q > 10$, the filter is a narrow Band Pass Filter Circuit. Hence Q is a measure of selectivity meaning the higher the value of Q , the more selective is the filter, or the narrower is the band width.

The relationship between Q , 3 db band width and the centre frequency f_c is given by

$$Q = \frac{f_c}{BW} = \frac{f_c}{f_H - f_L} \quad (15.31)$$

For the wide Band Pass Filter Circuit, the centre frequency can be defined as

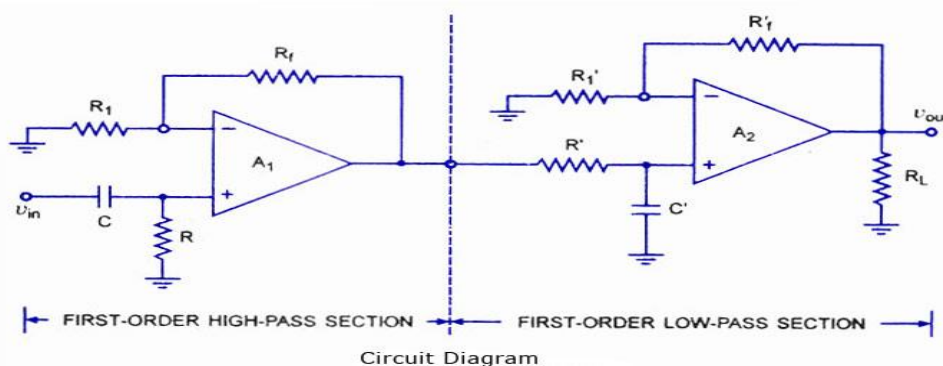
$$f_c = \sqrt{f_H f_L} \quad (15.32)$$

where f_H = high cutoff frequency, f_L = low cutoff frequency of the wide bandpass

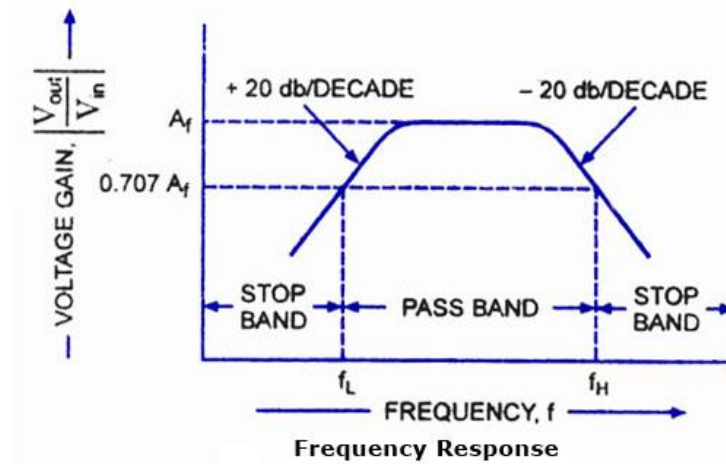
Wide Bandpass Filter:

A wide bandpass filter can be formed by simply cascading high-pass and low-pass sections and is generally the choice for simplicity of design and performance though such a circuit can be realized by a number of possible circuits.

To form a ± 20 db/ decade bandpass filter, a first-order high-pass and a first-order low-pass sections are cascaded; It means that, the order of the bandpass filter is governed by the order of the high-pass and low-pass filters it consists of.



Wide Band Pass Filter



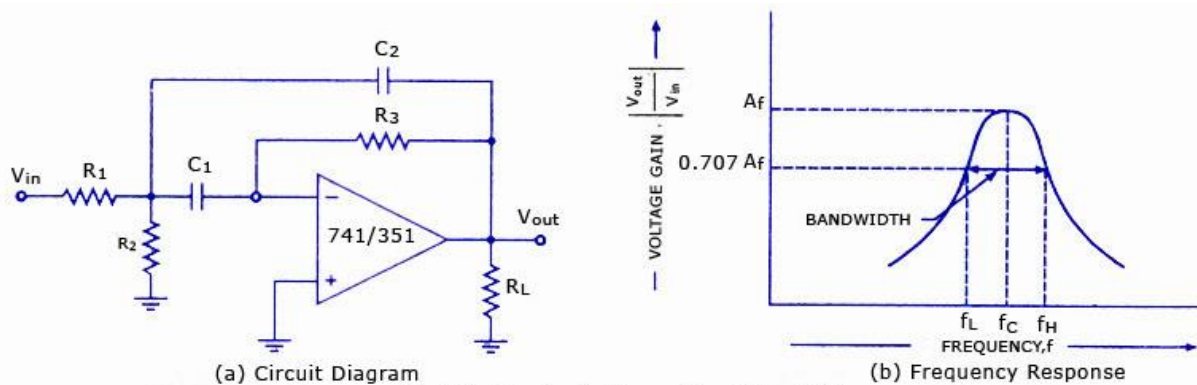
Frequency Response wide bandpass filter

www.CircuitsToday.com

Narrow BandPass Filter:

A narrow bandpass filter employing multiple feedback is depicted in figure. This filter employs only one op-amp, as shown in the figure. In comparison to all the filters discussed so far, this filter has some unique features that are given below.

1. It has two feedback paths, and this is the reason that it is called a multiple-feedback filter.
2. The op-amp is used in the inverting mode.



(a) Circuit Diagram

Multiple Feedback Narrow Band-Pass Filter

(b) Frequency Response

Narrow Bandpass Filter

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To simply use

$$R_1 = \frac{Q}{2\pi f_C C A_F}$$

$$R_2 = \frac{Q}{2\pi f_C C (2Q^2 - A_F)}$$

$$R_3 = \frac{Q}{\pi f_C C}$$

where A_F is the gain at f_C , given by

$$A_F = \frac{R_3}{2R_1} :$$

The gain A_F , however, must satisfy the condition

$$A_F < 2Q^2$$

Another advantage of the multiple feedback filter of Figure 7-13 is that its center frequency f_C can be changed to a new frequency f'_C without changing the gain or bandwidth. This is accomplished simply by changing R_2 to R'_2 so that

$$R'_2 = R_2 \left(\frac{f_C}{f'_C} \right)^2 \quad (7-15)$$

EXAMPLE 7-8

- Design the bandpass filter shown in Figure 7-13(a) so that $f_C = 1$ kHz, $Q = 3$, and $A_F = 10$.
- Change the center frequency to 1.5 kHz, keeping A_F and the bandwidth constant.

SOLUTION

- a. Choose the values of C_1 and C_2 first and then calculate the values of R_1 , R_2 , and R_3 from Equations (7-11) through (7-13). Let $C_1 = C_2 = C = 0.01 \mu\text{F}$.

$$R_1 = \frac{3}{(2\pi)(10^3)(10^{-8})(10)} = 4.77 \text{ k}\Omega$$

$$R_2 = \frac{3}{(2\pi)(10^3)(10^{-8})[2(3)^2 - 10]} = 5.97 \text{ k}\Omega$$

$$R_3 = \frac{3}{(\pi)(10^3)(10^{-8})} = 95.5 \text{ k}\Omega$$

Use $R_1 = 4.7 \text{ k}\Omega$, $R_2 = 6.2 \text{ k}\Omega$, and $R_3 = 100 \text{ k}\Omega$.

b)

on (7-15), the
1 kHz to 1.5 kHz is

$$R'_2 = (5.97 \text{ k}\Omega) \left(\frac{1(10^3)}{1.5(10^3)} \right)^2 = 2.65 \text{ k}\Omega$$

Band Reject Filter:

In this Band Reject Filter Circuit, frequencies are attenuated in the stop band and passed outside it, Types of Band Reject Filter Circuit,

1. Narrow band reject filter
2. Wide band reject filter

Narrow band reject filter:

The narrow band reject filter is also called the notch filter. Because of its higher Q which is greater than 10, the bandwidth of the narrow band reject filter is much smaller than that of the wide band reject filter.

The band reject filter is also called a band stop or band elimination filter because it eliminates a certain band of frequencies.

The narrow band reject filter, often called the notch filter, is commonly used for the attenuation of a single frequency. For example, it may be necessary to attenuate 60 Hz or 400 Hz noise or hum signals in a circuit.

The most commonly used notch filter is the Twin T network, shown in Fig. 15.21(a), which is a passive filter composed of two T shaped networks.

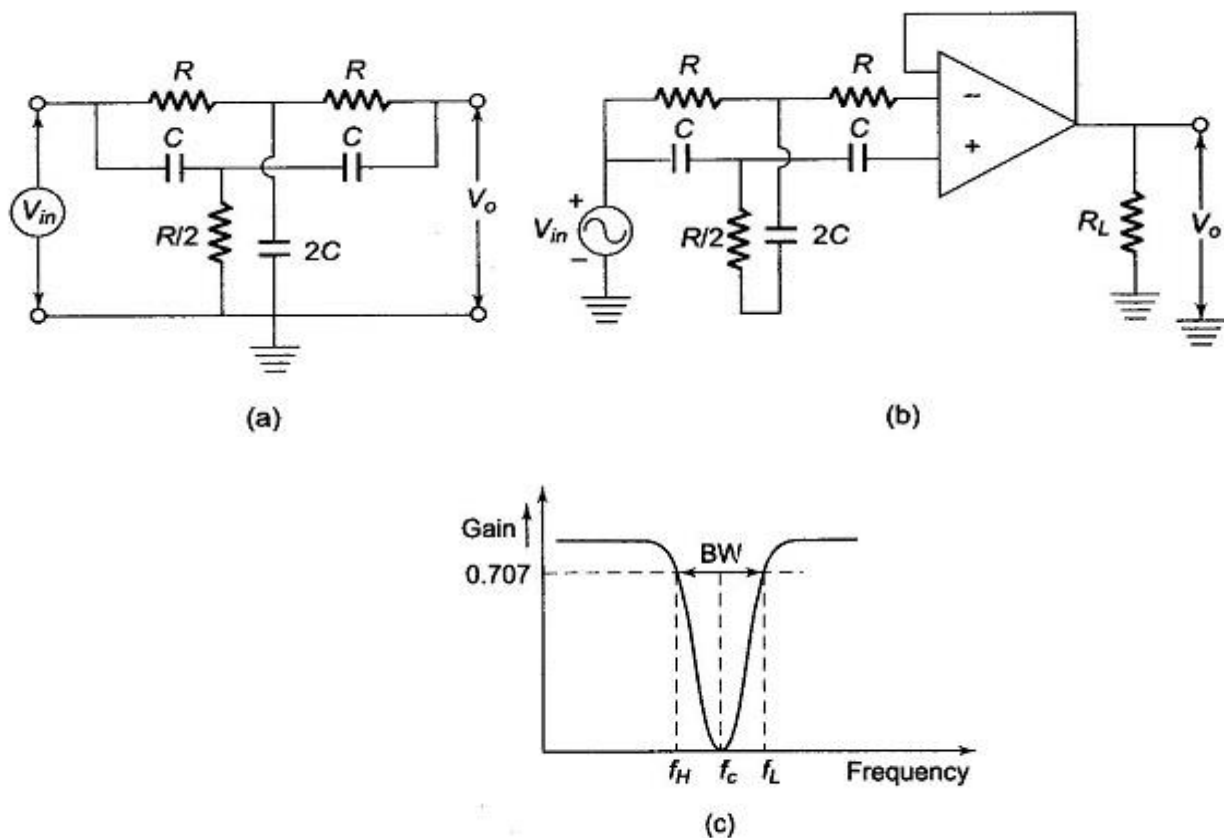


Fig. 15.21 (a) Twin-T Notch Filter (b) Active Notch Filter
(c) Frequency Response of a Notch Filter

One T network is made up of two resistors and a capacitor, while the other is made of two capacitors and a resistor. The frequency at which maximum attenuation occurs is called the notch-out frequency, given by

$$f_N = \frac{1}{2\pi RC} \quad (15.50)$$

One disadvantage of the passive twin T network is that it has a relatively low figure of merit, Q . As discussed earlier, the higher the value of Q , the more selective is the filter. Therefore, to increase the Q of the twin T network significantly, it should be used with a voltage follower, as shown in Fig. 15.21(b). Figure 15.21(c) shows the frequency response of a notch filter.

The Notch filters are used in communications, biomedical instruments, etc. where the elimination of certain frequencies is necessary.

EXAMPLE 7-10
Design a 60-Hz active notch filter.

SOLUTION
Let $C = 0.068 \mu\text{F}$. Then, from Equation (7-16), the value of R is

$$R = \frac{1}{2\pi f_N C} = \frac{1}{(2\pi)(60)(68)(10^{-9})} = 39.01 \text{ k}\Omega$$

(Use 39 k Ω .) For $R/2$, parallel two 39-k Ω resistors; for the $2C$ component, parallel two 0.068- μF capacitors.

Wide band Reject Filter:

Figure (a) shows wide band reject filter using a low pass filter, a high pass filter and a summing amplifier. For a proper band reject response, the low cutoff frequency f_L of the high pass filter must be larger than the high cutoff frequency f_H of the low pass filter.

Also, the pass band gain of both high pass and low pass sections must be equal.

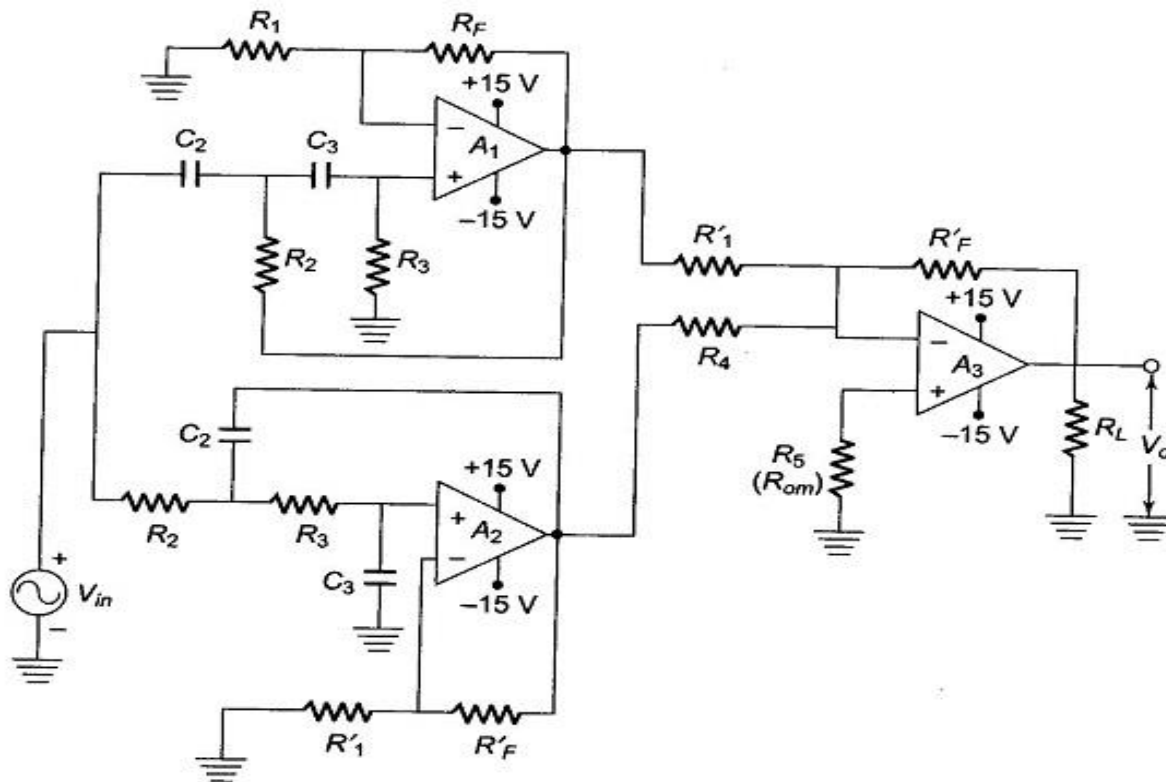


Fig. 15.20 (a) Wide Band Reject Filter Using a Low Pass, High Pass and Summing Amplifier

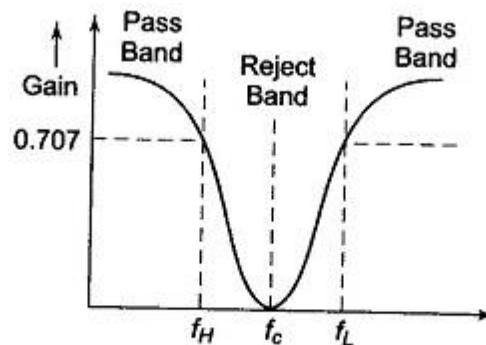


Fig. 15.20 (b) Frequency Response of a Wide Band Reject Filter

All Pass Filter:

The All Pass Filter Design is one that passes all frequency components of the input signal without attenuation. Any ordinary wire can be used to perform this characteristic but the most important factor in an all pass filter is that it provides predictable phase shifts for different frequencies of the input signal.

These filters are widely used in communications. For example, when signals are transmitted over transmission lines, such as telephone wires, from one point to another, they undergo a change in phase. All pass filters are used to compensate for these phase changes. They are also called delay equalizers or phase correctors.

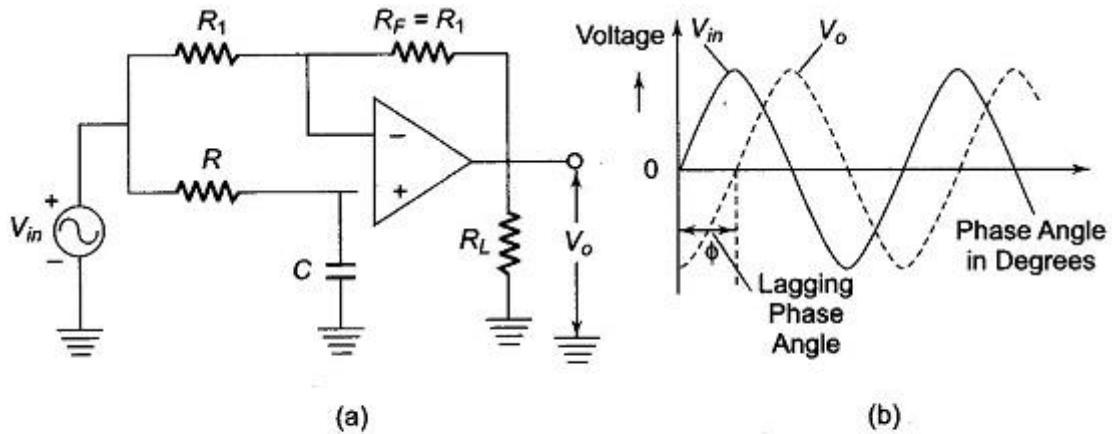


Fig. 15.22 (a) All Pass Filter Circuit (b) Input-Output Waveform Relation of an All Pass Filter (lagging)

Figure 15.22 shows an all pass filter with the output lagging the input. The output voltage V_o of the filter can be obtained by using the superposition theorem, as follows. From Fig. 15.22(a), we see that

$$V_o = -V_{in} + \frac{-jX_c}{R - jX_c} \times V_{in} \times 2 \quad (15.51)$$

Where

$$V_o = -V_{in} + \frac{\frac{1}{2\pi fC} \times V_{in} \times 2}{jR + \frac{1}{2\pi fC}}$$

$$V_o = -V_{in} + \frac{2V_{in}}{j2\pi fCR + 1}$$

$$V_o = -V_{in} \left(-1 + \frac{2}{j2\pi fCR + 1} \right)$$

$$V_o = -V_{in} + \frac{\frac{1}{2\pi fC} \times V_{in} \times 2}{jR + \frac{1}{2\pi fC}}$$

$$V_o = -V_{in} + \frac{2V_{in}}{j2\pi fCR + 1}$$

$$V_o = -V_{in} \left(-1 + \frac{2}{j2\pi fCR + 1} \right)$$

$$\text{Therefore } V_o = V_{in} \left(\frac{1 - j2\pi fCR}{1 + j2\pi fCR} \right) \quad (15.52)$$

The above equation indicates that the amplitude of V_o/V_{in} is unity that is $|V_o| = |V_{in}|$ throughout the useful frequency range and the phase shift between V_o and V_{in} is a function of input frequency. The phase angle Φ is given by

where Φ = phase in degrees f = frequency in Hz R = resistance in Ω C = capacitance in F

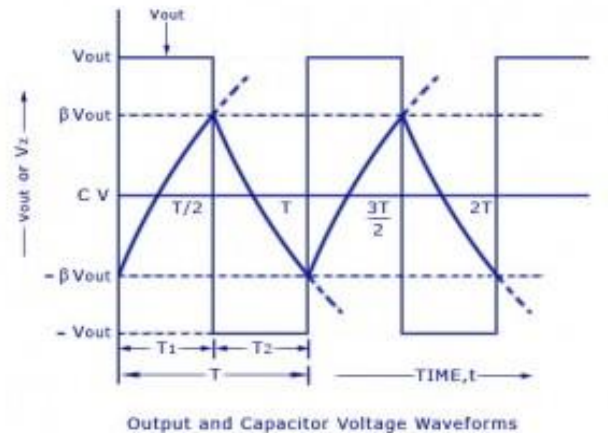
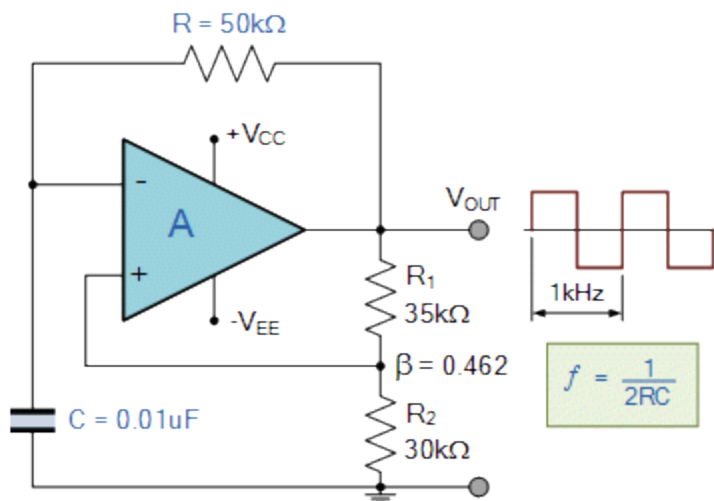
Referring to Fig. 15.22(a), if the positions of R and C are interchanged, the phase shift between input and output becomes positive. That is, output V_o leads input V_{in} .

Wave form Generators:

Three types: 1. Square Wave Generator, 2. Triangular Wave Generator, 3. Saw tooth Wave Generator

Square Wave Generator:

The Square Wave Generator Using Op amp means the astable multivibrator circuit using op-amp, which generates the square wave of required frequency.



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Astable multivibrator is also called as free-running multivibrator ($\because$ it has no I/p). The op voltage continuously switches between high & low levels without any I/p. It has no stable state.

The op-amp resistors R_1 and R_2 constitutes an INV schmitt trigger circuit. The I/p voltage to the schmitt trigger circuit is the voltage across the capacitor C .

Operation:

Let the capacitor voltage be initially zero i.e. $V_c = 0$ and let $V_o = +V_{sat}$. Due to positive feedback, the potential at point B in fig ① is given by

$$V_B = \frac{R_2}{R_1 + R_2} V_{sat} = UTP$$

When the capacitor voltage V_c just crosses the UTP voltage, the o/p V_o rapidly changes from $+V_{sat}$ to $-V_{sat}$. Now o/p voltage $V_o = -V_{sat}$. The voltage at point B is given by:

$$V_B = \frac{R_2}{R_1 + R_2} - V_{sat} = LTP$$

Analysis:

The charging of capacitor is exponential & in capacitor voltage at any instant is given by:

$$V_{c1} = V_f + (V_i - V_f) e^{-t/\tau} \rightarrow \textcircled{1}$$

Where $\tau = RC$ time constant of charging.

V_f = final value of capacitor voltage.

$\therefore V_f = +V_{sat}$ in the interval $0 < t < T/2$

V_i = Initial value of the capacitor voltage

$$\therefore V_i = -\frac{R_2}{R_1 + R_2} V_{sat}$$

$$\left(\text{where } \beta = \frac{R_2}{R_1 + R_2} \right)$$

$$V_i = -\beta V_{sat}$$

Now eq (1) becomes.

$$\begin{aligned} V_{c1} &= +V_{sat} + [-\beta V_{sat} - V_{sat}] e^{-\frac{t}{R_1 C_1}} \\ &= +V_{sat} + [-V_{sat} (1 + \beta)] e^{-\frac{t}{R_1 C_1}} \end{aligned}$$

$$V_{c1} = +V_{sat} [1 - (1 + \beta) e^{-t/R_1 C_1}] \rightarrow \textcircled{2}$$

$$\text{At } t = T/2, \quad V_c = +\beta V_{sat}$$

Now eq (2) becomes

$$\beta V_{sat} = V_{sat} \left[1 - (1+\beta) e^{-\frac{T}{2RC}} \right]$$

$$\beta = 1 - (1+\beta) e^{-\frac{T}{2RC}}$$

$$(1+\beta) e^{-\frac{T}{2RC}} = 1 - \beta$$

$$\boxed{e^{-\frac{T}{2RC}} = \frac{(1-\beta)}{(1+\beta)}} \rightarrow (3)$$

Taking natural log on both sides of eq (3), we get,

$$-\frac{T}{2RC} = \ln \frac{(1-\beta)}{(1+\beta)}$$

$$T = -2RC \ln \left(\frac{1-\beta}{1+\beta} \right)$$

$$\boxed{T = +2RC \ln \left(\frac{1+\beta}{1-\beta} \right)} \rightarrow (4)$$

Now if $\beta = 0.47$ in eq (4), then

$$T = 2RC \ln \left(\frac{1+0.47}{1-0.47} \right)$$

$$T = 2RC \ln (2.77)$$

$$T = 2RC(1)$$

$$T = 2RC$$

$$\boxed{f = \frac{1}{2RC}}$$

WKT $\boxed{f = \frac{1}{T}}$

Triangular Waveform Generator:

The output of integrator is a Triangular Wave Generator Using Op amp if its input is a square wave. This means that a Triangular Wave Generator Using Op amp can be formed by simply connecting an integrator to the square wave generator as shown in the Fig.

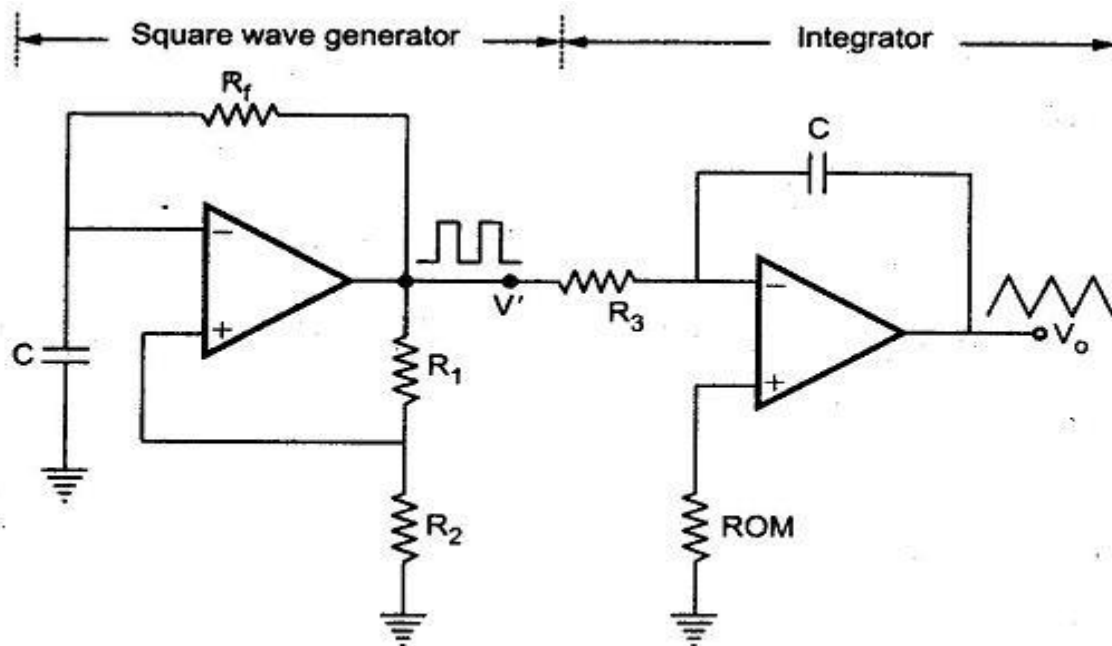


Fig. 2.85 Triangular wave generator

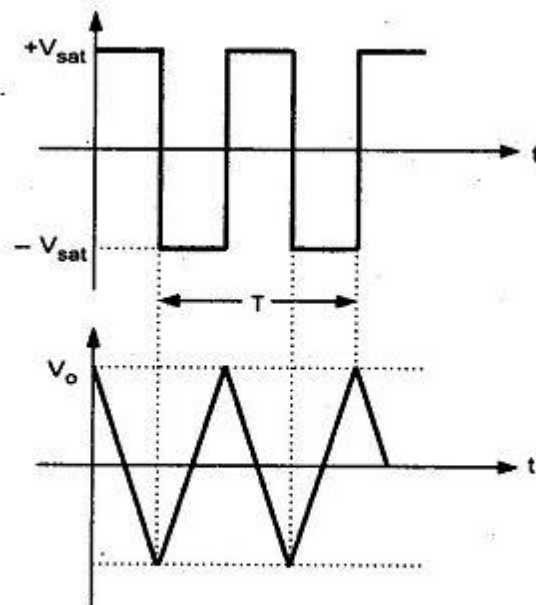


Fig. 2.86 Waveforms of triangular wave generator

Basically, triangular wave is generated by alternatively charging and discharging a capacitor with a constant current. This is achieved by connecting integrator circuit at the output of square wave generator.

Assume that V' is high at $+V_{sat}$. This forces a constant current ($+V_{sat}/R_3$) through C (left to right) to drive V_o negative linearly. When V' is low at $-V_{sat}$, it forces a constant current ($-V_{sat}/R_3$) through C (right to left) to drive V_o positive, linearly. The frequency of the triangular wave is same as that of square wave. This is illustrated in Fig. 2.86.

Although the amplitude of the square wave is constant ($\pm V_{sat}$), the amplitude of the triangular wave decreases with an increase in its frequency, and vice versa. This is because the reactance of capacitor decreases at high frequencies and increases at low frequencies.

In practical circuits, resistance R_4 is connected across C to avoid the saturation problem at low frequencies as in the case of practical integrator as shown in the Fig. 2.87.

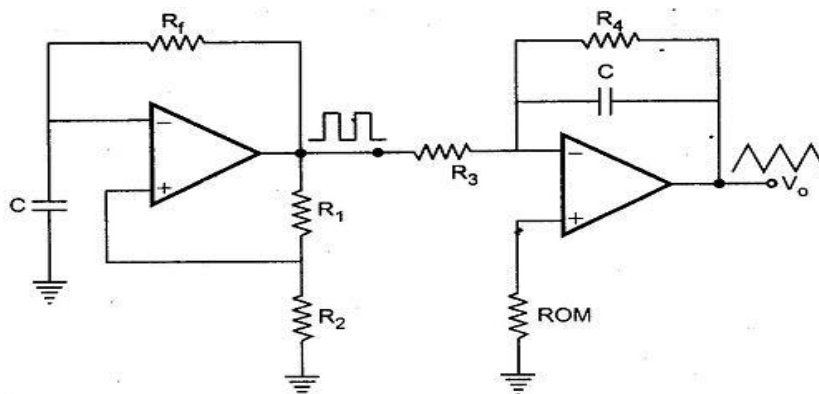


Fig. 2.87 Waveforms for practical triangular wave generator

Triangular Waveform Generator using lesser components:

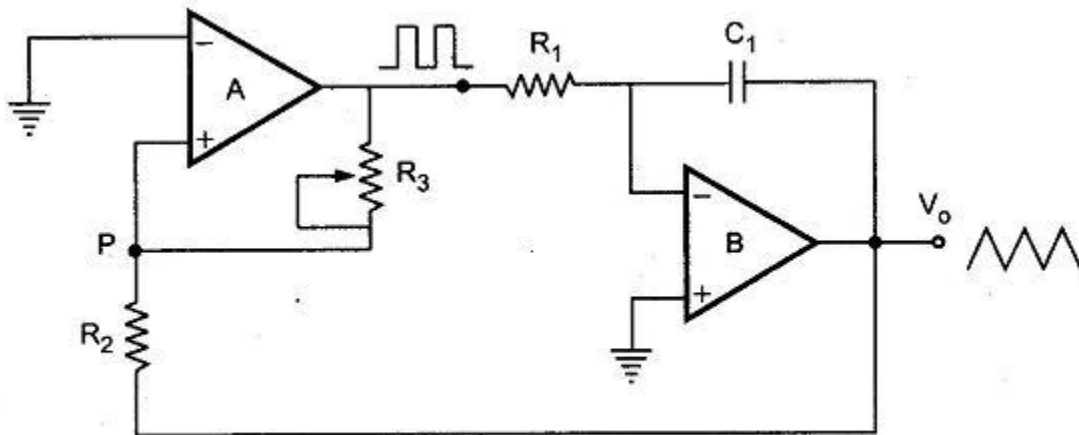


Fig. 2.88 Triangular wave generator

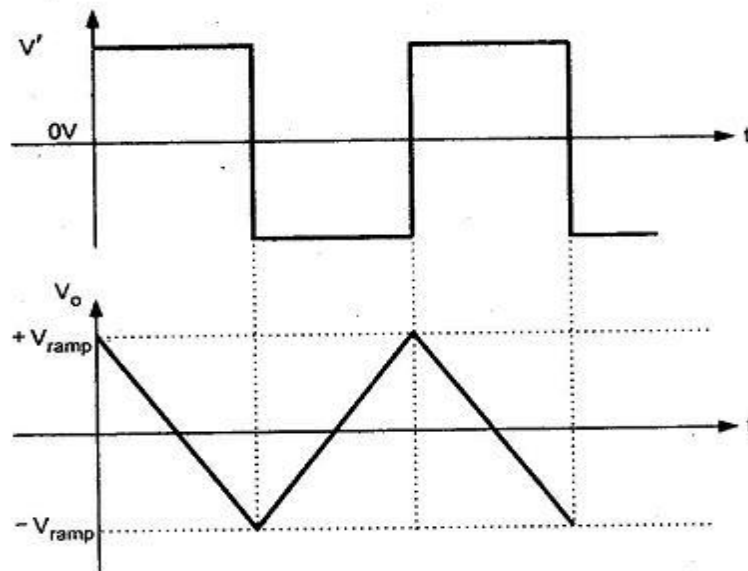


Fig. 2.89 Waveforms of triangular wave generator

It consists of a comparator (A) and an integrator (B). The output of comparator A is a square wave of amplitude $\pm V_{sat}$ and is applied to the inverting (—) input terminal of the integrator B. The output of integrator is a triangular wave and it is feedback as input to the comparator A through a voltage divider $R_2 R_3$.

To understand circuit operation, assume that the output of comparator A is at $+V_{sat}$. This forces a constant current $(+V_{sat}/R_1)$ through C to give a negative going ramp at the output of the integrator, as shown in the Fig. 2.88. Therefore, one end of voltage divider is at a voltage $+V_{sat}$ and the other at the negative going ramp.

When the negative going ramp reaches a certain value — V_{ramp} , the effective voltage at point

As a result, the output of comparator A switches from positive saturation to negative saturation ($-V_{\text{sat}}$). This forces a reverse constant current (right to left) through C to give a positive going ramp at the output of the integrator, as shown in the Fig. 2.89.

When positive going ramp reaches $+V_{\text{ramp}}$, the effective voltage at point p becomes slightly above 0V. As a result, the output of comparator A switches from negative saturation to positive saturation ($+V_{\text{sat}}$). The sequence then repeats to give triangular wave at the output of integrator B.

Amplitude and Frequency Calculations:

The frequency and amplitude of the Triangular Wave Generator Using Op amp wave can be determined as follows : When comparator output is at $+V_{\text{sat}}$, the effective voltage at point P is given by

$$-V_{\text{ramp}} + \frac{R_2}{R_2 + R_3} [+V_{\text{sat}} - (-V_{\text{ramp}})] \quad \dots (1)$$

When effective voltage at P becomes equal to zero, we can write above equation

$$\begin{aligned} -V_{\text{ramp}} + \frac{R_2}{R_2 + R_3} [+V_{\text{sat}} - (-V_{\text{ramp}})] &= 0 \\ -V_{\text{ramp}} + \frac{R_2}{R_2 + R_3} (V_{\text{ramp}}) + \frac{R_2}{R_2 + R_3} (+V_{\text{sat}}) &= 0 \\ \frac{-R_3}{R_2 + R_3} (V_{\text{ramp}}) &= -\frac{R_2}{R_2 + R_3} (+V_{\text{sat}}) \\ \therefore -V_{\text{ramp}} &= \frac{-R_2}{R_3} (+V_{\text{sat}}) \quad \dots (2) \end{aligned}$$

Similarly, when comparator output is at $-V_{\text{sat}}$, we can write,

$$V_{\text{ramp}} = \frac{-R_2}{R_3} (-V_{\text{sat}}) \quad \dots (3)$$

The peak to peak amplitude of the triangular wave can be given as

$$\begin{aligned} V_{o(pp)} &= +V_{\text{ramp}} - (-V_{\text{ramp}}) \\ &= \frac{-R_2}{R_3} (-V_{\text{sat}}) - \left(\frac{-R_2}{R_3} \right) (+V_{\text{sat}}) \quad \dots (4) \end{aligned}$$

If $|+V_{\text{sat}}| = |-V_{\text{sat}}|$ then, we can write

$$V_{o(pp)} = \frac{R_2}{R_3} V_{\text{sat}} + \frac{R_2}{R_3} V_{\text{sat}} = \frac{2R_2}{R_3} V_{\text{sat}} \quad \dots (5)$$

The time taken by the output to swing from $-V_{\text{ramp}}$ to $+V_{\text{ramp}}$ (or from $+V_{\text{ramp}}$ to $-V_{\text{ramp}}$) is equal to half the time period $T/2$. Refer Fig. 2.89. This time can be calculated from the integrator output equation as follows :

$$V_{o(\text{pp})} = -\frac{1}{R_1 C_1} \int_0^{T/2} (-V_{\text{sat}}) dt = \left(\frac{V_{\text{sat}}}{R_1 C_1} \right) \frac{T}{2} \quad \dots (6)$$

$$T = \frac{2 R_1 C_1 V_{o(\text{pp})}}{V_{\text{sat}}} \quad \dots (7)$$

Substituting value of $V_{o(\text{pp})}$ we get, Triangular Wave Generator Using Op amp

$$T = \frac{2 R_1 C_1 \left(\frac{2 R_2}{R_3} V_{\text{sat}} \right)}{V_{\text{sat}}} = \frac{4 R_1 C_1 R_2}{R_3} \quad \dots (8)$$

Therefore, the frequency of oscillation can be given as,

$$f_o = \frac{1}{T} = \frac{R_3}{4 R_1 C_1 R_2} \quad \dots (9)$$

EXAMPLE 7-16

Design the triangular wave generator of Figure 7-23 so that $f_o = 2 \text{ kHz}$ and $v_{o(\text{pp})} = 7 \text{ V}$. The op-amp is a 1458/772 and supply voltages $= \pm 15 \text{ V}$.

SOLUTION

For the 1458, $V_{\text{sat}} = 14 \text{ V}$. Therefore, from Equation (7-29),

$$\frac{R_2}{R_3} = \frac{7}{(2)(14)}$$

$$R_2 = \frac{R_3}{4}$$

Let $R_2 = 10 \text{ k}\Omega$; then $R_3 = 40 \text{ k}\Omega$. (Use a 50-k Ω potentiometer.)

Now, from Equation (7-30c),

$$2 \text{ kHz} = \frac{40 \text{ k}\Omega}{(4)(R_1 C_1)(10 \text{ k}\Omega)}$$

Therefore, $R_1 C_1 = 0.5 \text{ ms}$. Let $C_1 = 0.05 \mu\text{F}$; then $R_1 = 10 \text{ k}\Omega$. Thus $R_1 = 10 \text{ k}\Omega$, $C_1 = 0.05 \mu\text{F}$, and $R_3 = 40 \text{ k}\Omega$ (50-k Ω potentiometer). [See Figure 7-23(a).]

Saw Tooth Waveform Generator:

A sawtooth waveform is used in [pulse width modulation](#) circuits and time-base generators. A potentiometer is used when the wiper moves toward negative voltage(-V); then the rise time becomes more than the fall time. When the wiper moves towards positive voltage(+V), then the rise time becomes less than the fall time.

When the comparator output goes negative saturation, a negative voltage is added to the inverting terminal, thereby the wiper moves to a negative supply. This causes a decrease in the potential difference across R1 and hence current through the capacitor and resistor decreases.

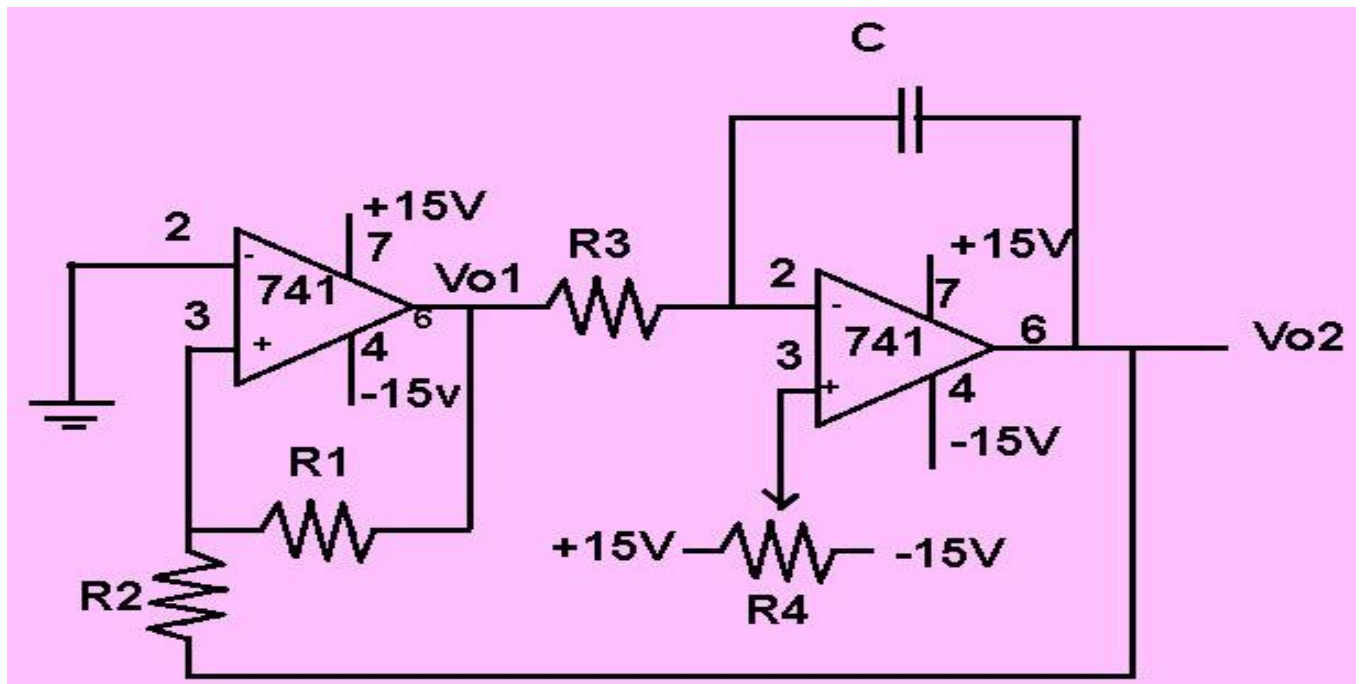
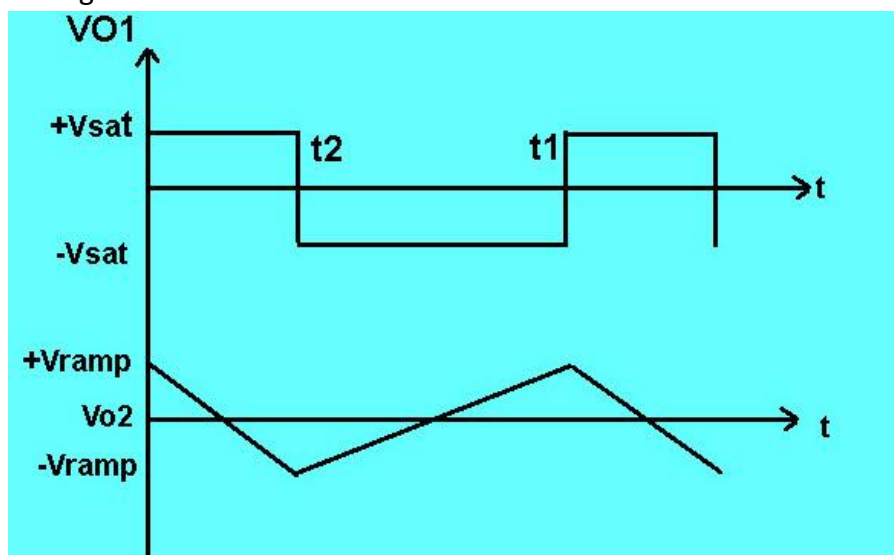


Fig.(a) Circuit Diagram



Then the slope decreases and rise time also decrease. When [the comparator](#) output is under positive saturation, the potential difference across the R1 increases and current through the capacitor resistor also increases. This is due to the presence of negative voltage at the inverting terminal. Then the slope increases and fall time decreases. And the output is obtained as a sawtooth waveform.

Applications:

- The sawtooth waveform is most common waveform used to create sounds with subtractive virtual and analog music synthesizers. Therefore, it is used in music.
- The sawtooth is the form of horizontal and vertical deflection signals that are used to generate a raster on monitor screens or CRT based television.
- The magnetic field suddenly gets collapsed on the wave's cliff, which causes the resting position of its electron beam as quickly as possible.
- The magnetic field produced by the deflection yoke drags the electron beam on the wave's ramp, creating a scan line.

IC 555 TIMER

Introduction:

The 555 Timer is one of the most popular and versatile integrated circuits ever produced! "Signetics" Corporation first introduced this device as the SE/NE 555 in early 1970.

IC 555 is a monolithic timing circuit that can produce accurate and highly stable time delays or oscillations. It is a combination of digital and analog circuits. It is known as the "time machine" as it performs a wide variety of timing tasks.

Features of IC 555 timer :

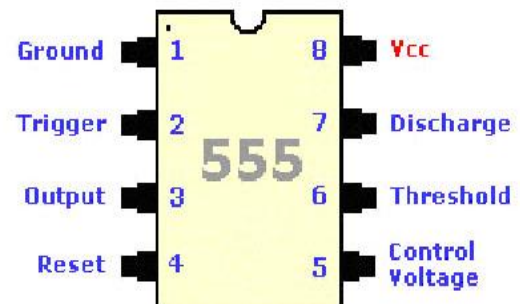
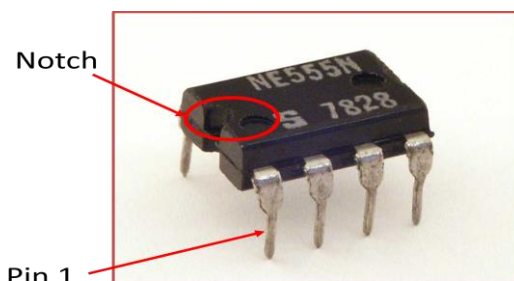
- It operates on +5V to +18V.
- It has adjustable duty cycle.
- High temperature stability.
- High current output. [200mA Sink @ Source]
- Low cost.
- Operated in two modes :
 - i) Monostable Multivibrator mode and
 - ii) Astable or free running mode.

Applications for the 555 Timer include:

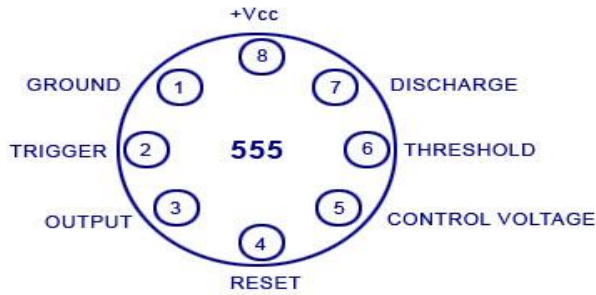
1. Ramp and Square wave generator
2. Frequency dividers
3. Voltage-controlled oscillators
4. Pulse generators and LED flashers
5. Burglar alarms
6. Traffic light control

555 timer- Pin Diagram:

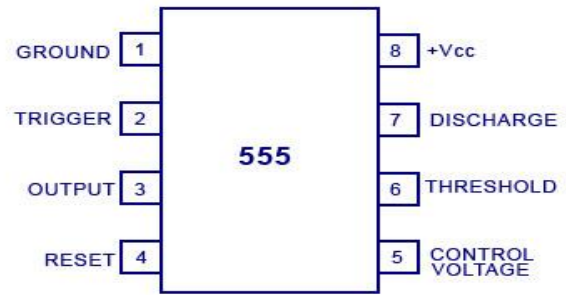
The 555 timer is an 8-Pin D.I.L. Integrated Circuit or 'chip'



555 TIMER IC



Top View Of Metal Can Package



8-Pin DIP

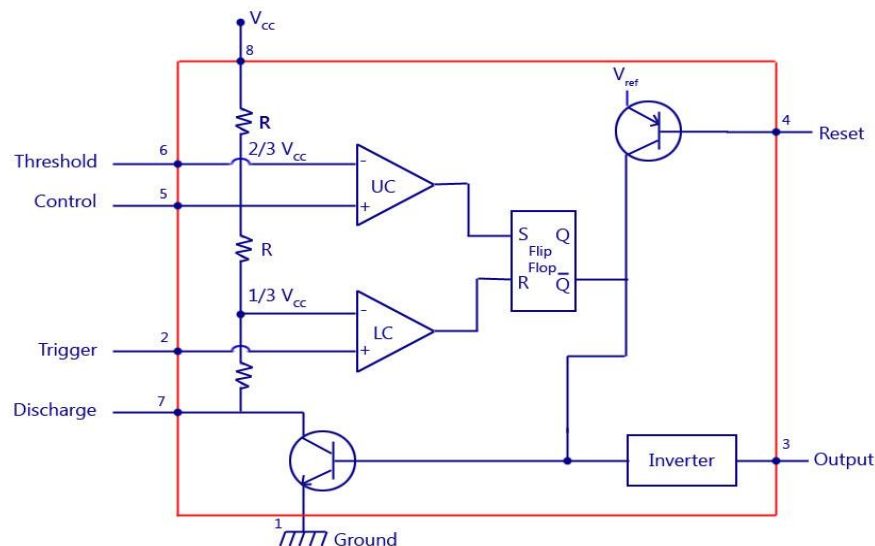
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555 timer- Pin Description:

Pin	Name	Purpose
1	GND	Ground, low level (0 V)
2	TRIG	OUT rises, and interval starts, when this input falls below $1/3 V_{CC}$.
3	OUT	This output is driven to approximately 1.7V below $+V_{CC}$ or GND.
4	RESET	A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides THR.
5	CTRL	"Control" access to the internal voltage divider (by default, $2/3 V_{CC}$).
6	THR	The interval ends when the voltage at THR is greater than at CTRL.
7	DIS	Open collector output; may discharge a capacitor between intervals. In phase with output.
8	V_+ , V_{CC}	Positive supply voltage is usually between 3 and 15 V.

Functional Block Diagram:

555 IC Timer Block Diagram



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Operation:

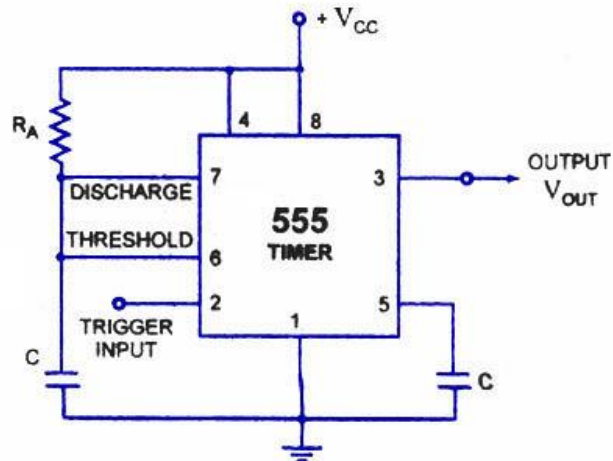
- The voltage divider has three equal 5K resistors. It divides the input voltage (V_{cc}) into three equal parts.
- The two comparators are op-amps that compare the voltages at their inputs and saturate depending upon which is greater.
 - The Threshold Comparator saturates when the voltage at the Threshold pin (pin 6) is greater than $(2/3)V_{cc}$.
 - The Trigger Comparator saturates when the voltage at the Trigger pin (pin 2) is less than $(1/3)V_{cc}$.
- The flip-flop is a bi-stable device. It generates two values, a “high” value equal to V_{cc} and a “low” value equal to 0V.
 - When the Threshold comparator saturates, the flip flop is Reset (R) and it outputs a low signal at pin 3.
 - When the Trigger comparator saturates, the flip flop is Set (S) and it outputs a high signal at pin 3.
- The transistor is being used as a switch, it connects pin 7 (discharge) to ground when it is closed.
 - When Q is low, Q bar is high. This closes the transistor switch and attaches pin 7 to ground.
 - When Q is high, Q bar is low. This opens the switch and pin 7 is no longer grounded.

555 Timer operating modes:

The 555 has three operating modes:

1. Monostable Multivibrator
2. Astable Multivibrator
3. Bistable Multivibrator

Monostable Multivibrator (Using 555 Timer):



Circuit of The Timer 555 as a Monostable Multivibrator

The circuit in Figure 1 is connected as a monostable multivibrator, the resistance R_A and the capacitor C are external to the chip, and their values determine the output pulse width. The three equal resistances R , inside the chip, establish the reference voltages $2/3 V_{CC}$ and $1/3 V_{CC}$ for comparators 1 and 2 of timer respectively. The value of R cannot be controlled precisely. However, IC fabrication techniques control resistance ratios accurately so that reference voltages are precise.

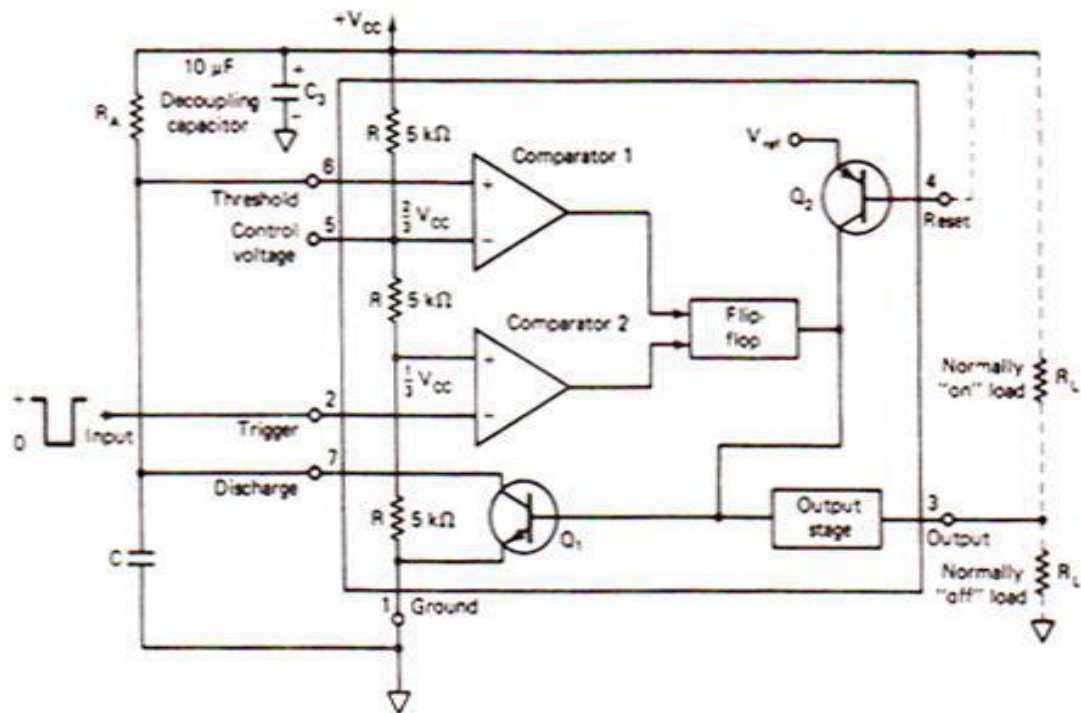
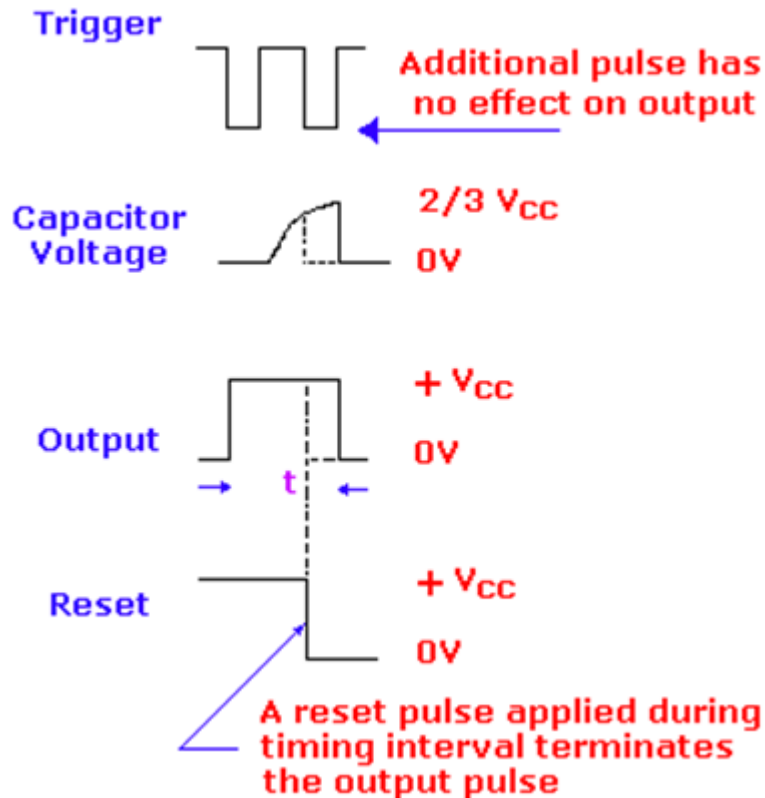


Figure 1

- In the standby state, FF holds transistor Q1 ON, thus clamping the external timing capacitor C to ground. The output remains at ground potential. i.e. Low.
- As the trigger passes through $V_{CC}/3$, the FF is set, i.e. $Q = 0$, then the transistor Q1 OFF and the short circuit across the timing capacitor C is released. As Q is low, output goes HIGH.

Wave Forms:



Derivation of Pulse width:

The voltage across capacitor increases exponentially and is given by:

$$V_c = V_{CC} \left[1 - e^{-t/R_{AC}} \right] \rightarrow \textcircled{1}$$

$$\text{at } t = T, V_c = \frac{2}{3} V_{CC}$$

Now eq (1) becomes

$$\frac{2}{3} V_{cc} = V_{cc} [1 - e^{-T/RAC}]$$

$$\frac{2}{3} = 1 - e^{-T/RAC}$$

$$\frac{2}{3} - 1 = - e^{-T/RAC}$$

$$\frac{2-3}{3} = - e^{-T/RAC}$$

$$-\frac{1}{3} = - e^{-T/RAC}$$

$$e^{-T/RAC} = \frac{1}{3}$$

$$e^{-T/RAC} = \frac{1}{3}$$

$$-\frac{T}{RAC} = \ln\left[\frac{1}{3}\right]$$

$$+\frac{T}{RAC} = +1.0996$$

$$\boxed{T = 1.0996 RAC}$$

$$\therefore \boxed{T \approx 1.1 RAC} \rightarrow (2)$$

Eq (2) indicates that the O/P Voltage waveform depends on the values of R_A & C and it is independent of V_{cc} .

1] Design a monostable multivibrator using 555 timer to obtain a pulse width of 10msec

Jan-10, 6M

Sol3 Given, $T = 10\text{msec}$

WKT, $T = 1.1 R_A C$

$$R_A C = \frac{T}{1.1}$$

$$R_A C = \frac{10\text{msec}}{1.1}$$

$$R_A C = 9.09\text{msec}$$

← 1M

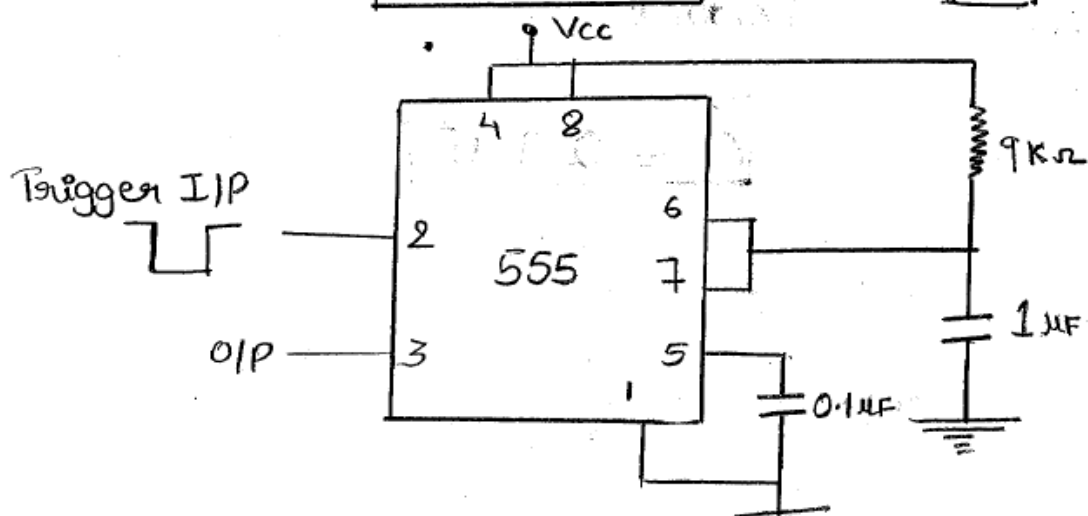
Assume $C = 1\mu\text{F}$

← 1M

$$R_A = \frac{9.09\text{msec}}{1\mu\text{F}} = 9.09\text{k}\Omega$$

$$\therefore R_A = 9.9\text{k}\Omega$$

← 2M



Applications in Monostable Mode:

1. Missing Pulse Detector.
2. Linear Ramp Generator.
3. Frequency Divider.
4. Pulse Width Modulation.

1. Missing Pulse Detector:

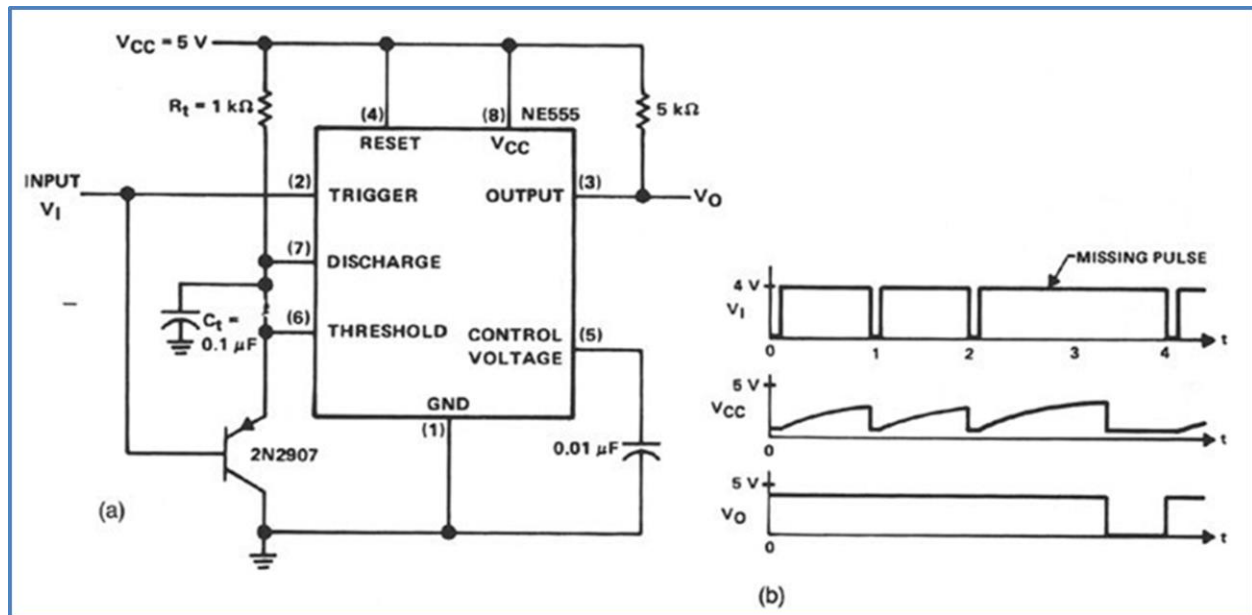


Fig (a) : A missing Pulse Detector Monostable Circuit

Fig (b) : Output of Missing Pulse Detector

- When input trigger is Low, emitter-base diode of Q is forward biased capacitor is clamped to 0.7V (of diode), output of timer is HIGH width of T o/p of timer > trigger pulse width.
- $T = 1.1RC$ select R & C such that $T >$ trigger pulse.
- Output will be high during successive coming of input trigger pulse. If one of the input trigger pulse missing trigger i/p is HIGH, Q is cut off, timer acts as normal monostable state.
- It can be used for speed control and measurement

2.Linear Ramp Generator:

3. Frequency Divider:

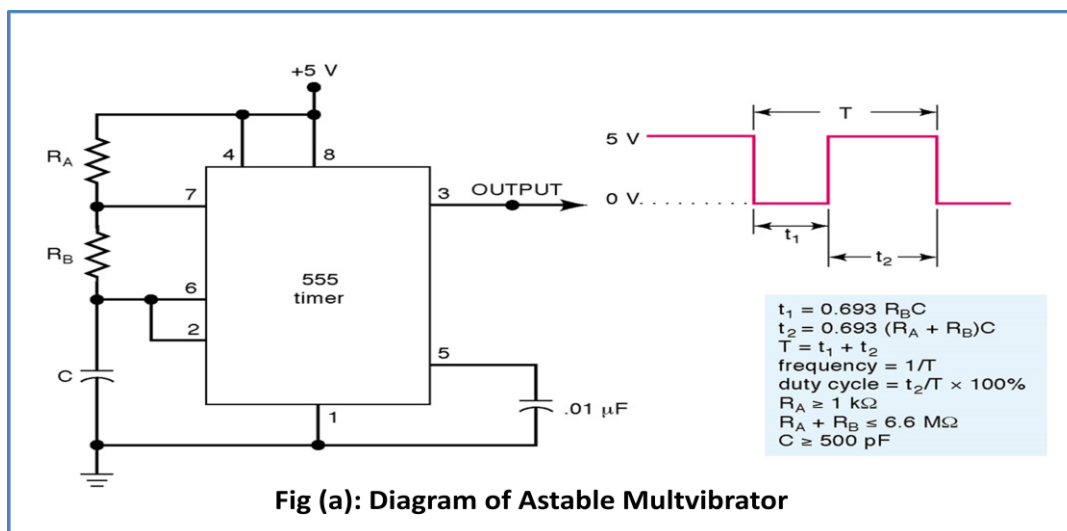
4. Pulse Width Modulation:

The charging time of capacitor is entirely depend upon $2V_{cc}/3$. When capacitor voltage just reaches about $2V_{cc}/3$ output of the timer is coming from HIGH to Low level. We can control this charging time of the capacitor by adding continuously varying signal at the pin-5 of the 555 timer which is denoted as control voltage point. Now each time the capacitor

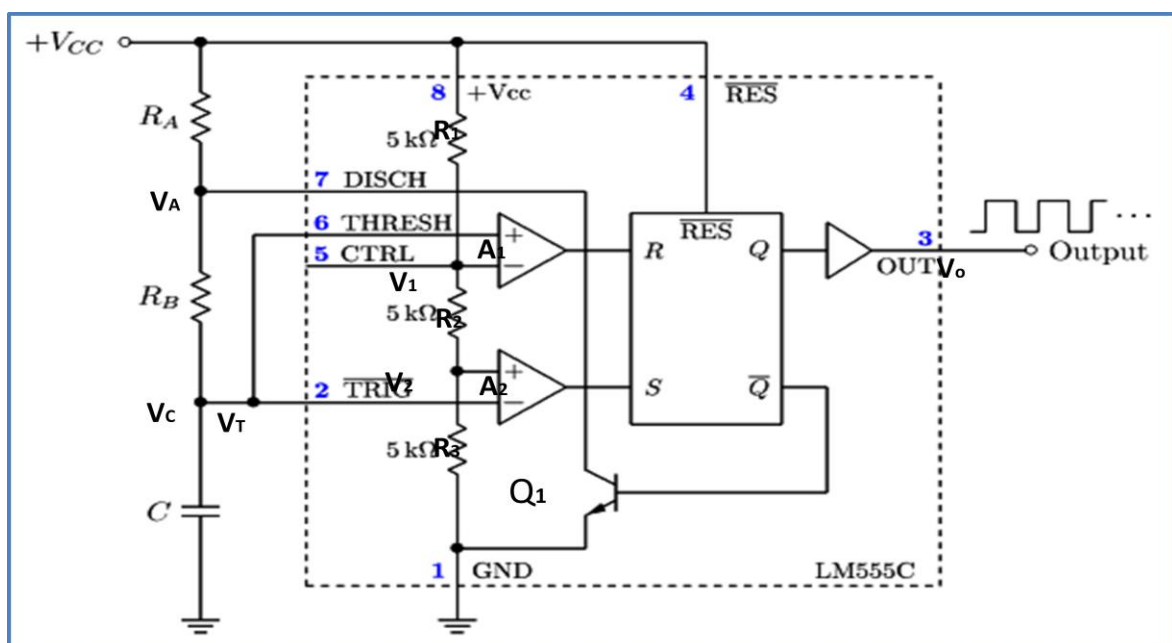
voltage is compared control voltage according to the o/p pulse width change. So o/p pulse width is changing according to the signal applied to control voltage point. So the output is pulse width modulated form.

Astable Multivibrator:

- Astable multivibrator is simply an oscillator. The astable multivibrator generates a continuous stream of rectangular off-on pulses that switch between two voltage levels.
- The frequency of the pulses and their duty cycle are dependent upon the RC network values.
- The capacitor C charges through the series resistors R_A and R_B with a time constant $(R_A + R_B)C$. The capacitor discharges through R_B with a time constant of $R_B C$



Functional Diagram of Astable Multivibrator using 555 Timer



- Connect external timing capacitor between trigger point (pin 2) and Ground.
- Split external timing resistor R into RA & RB, and connect their junction to discharge terminal (pin 7).
- Remove trigger input, monostable is converted to Astable multivibrator.
- This circuit has no stable state. The circuit changes its state alternately. Hence the operation is also called free running oscillator.

* Let us assume that initially the 555 O/P is high, the discharge transistor Q_1 is OFF & the capacitor 'C' starts charging towards V_{CC} through RA & RB.

* When Capacitor charging voltage equals to $\frac{2}{3} V_{CC}$, it causes the Comparator 1 O/P to go high. Hence the F/F O/P $Q=1$ and $\bar{Q}=0$. Thus, the O/P of timer is low.

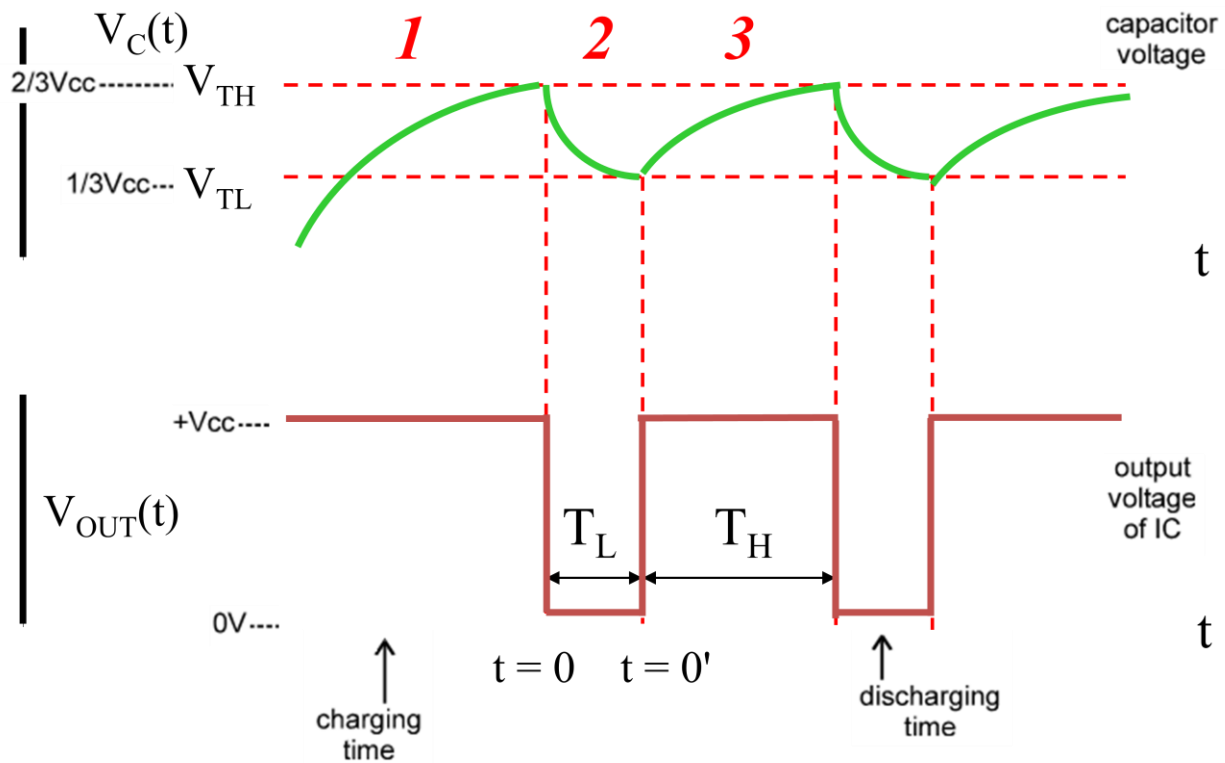
Now capacitor 'C' starts discharging through RB and transistor Q_1 .

* When the discharging voltage across the capacitor 'C' equals $\frac{V_{CC}}{3}$, Comparator 2 O/P goes to high and hence it resets the F/F. Then the cycle repeats. Thus Capacitor is periodically charged and discharged between $\frac{2V_{CC}}{3}$ to $\frac{V_{CC}}{3}$ respectively.

* The time during which the capacitor charges from $\frac{V_{CC}}{3}$ to $\frac{2V_{CC}}{3}$ is equal to the time the O/P is high.

||y The time during which the capacitor discharges from $\frac{2V_{CC}}{3}$ to $\frac{V_{CC}}{3}$ is equal to the time the O/P is low.

Timing Diagram of a 555 Astable:



The capacitor voltage for a low pass RC circuit subjected to a step input of V_{cc} volts is given by

$$v_c = V_{cc} (1 - e^{-t/RC})$$

The time t_1 taken by the circuit to charge from 0 to $(2/3) V_{cc}$ is,

$$(2/3) V_{cc} = V_{cc} (1 - e^{-t_1/RC}) \quad (8.9)$$

or, $t_1 = 1.09 RC$

and the time t_2 to charge from 0 to $(1/3) V_{cc}$ is,

$$(1/3) V_{cc} = V_{cc} (1 - e^{-t_2/RC}) \quad (8.10)$$

or, $t_2 = 0.405 RC$

So the time to charge from $(1/3) V_{cc}$ to $(2/3) V_{cc}$ is

$$t_{HIGH} = t_1 - t_2$$

$$t_{HIGH} = 1.09 RC - 0.405 RC = 0.69 RC$$

So, for the given circuit,

$$t_{HIGH} = 0.69 (R_A + R_B)C \quad (8.11)$$

The output is low while the capacitor discharges from $(2/3) V_{cc}$ to $(1/3) V_{cc}$ and the voltage across the capacitor is given by

$$(1/3) V_{cc} = (2/3) V_{cc} e^{-t/RC}$$

solving, we get $t = 0.69 RC$

So, for the given circuit, $t_{LOW} = 0.69 R_B C$ (8.12)

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or, $T = 0.69 (R_A + 2R_B) C$

So, $f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$ (8.13)

Duty Cycle,

$$\%D = \frac{t_{HIGH}}{T} \times 100 = \frac{0.69(R_A + R_B)C}{0.69(R_A + 2R_B)C} \times 100 = \frac{(R_A + R_B)}{(R_A + 2R_B)} \times 100$$

$$\%D = \frac{t_{LOW}}{T} \times 100 = \frac{0.69 R_B C}{0.69(R_A + 2R_B)C} \times 100 = \frac{R_B}{(R_A + 2R_B)} \times 100$$

Uses of the Astable Multivibrator:

- Flashing LED's
- Pulse Width Modulation
- Pulse Position Modulation
- Periodic Timers
- Uses include [LEDs](#), pulse generation, logic clocks, security alarms and so on.

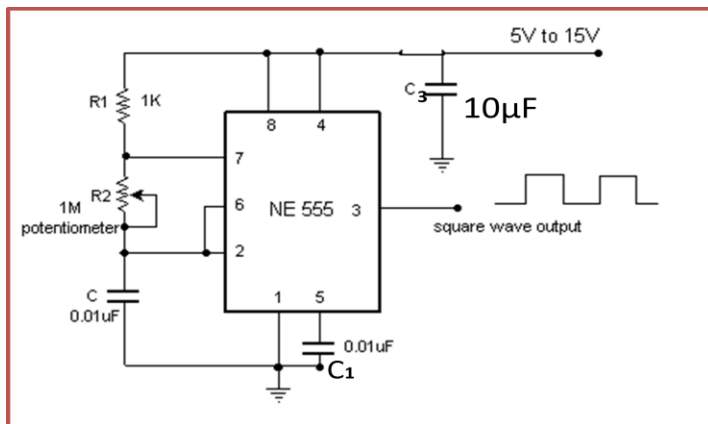
Applications in Astable Mode:

1. Square Generator

2. FSK Generator

3. Pulse Position Modulator

1. Square Generator



$$DutyCycle = \frac{(R_1 + R_2)}{(R_1 + 2R_2)} \times 100 = 50\%$$

Here $R_1 = 0$

- To avoid excessive discharge current through Q_1 when $R_1 = 0$ connect a diode across R_2 , place a variable R in place of R_1 .
- Charging path R_1 & D ; Discharging path R_2 & pin 7.

2. FSK Generator:

3. Pulse Position Modulator:

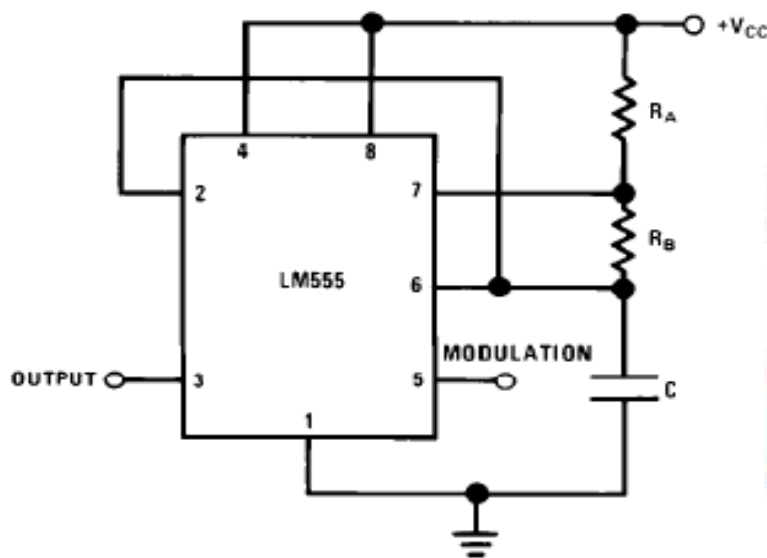


Fig (a): Pulse position Modulator

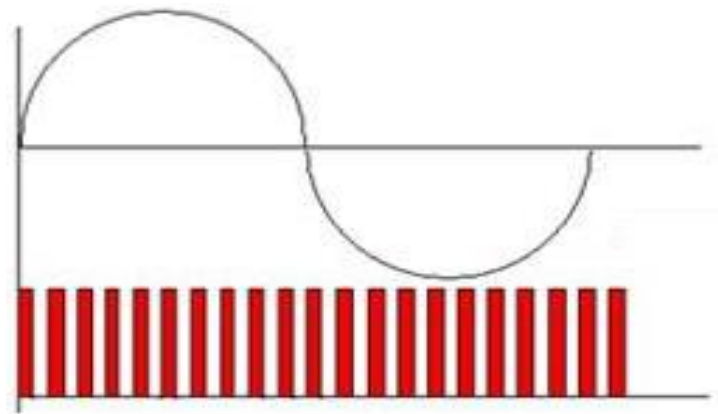


Fig (b): Output Wave Form of PPM

Description:

- The pulse position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation.
- The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.
- The output waveform that the frequency is varying leading to pulse position modulation.

Comparison of Multivibrator Circuits:

Phase Locked Loops (PLL)

Introduction:

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked loop (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

Block Diagram of PLL:

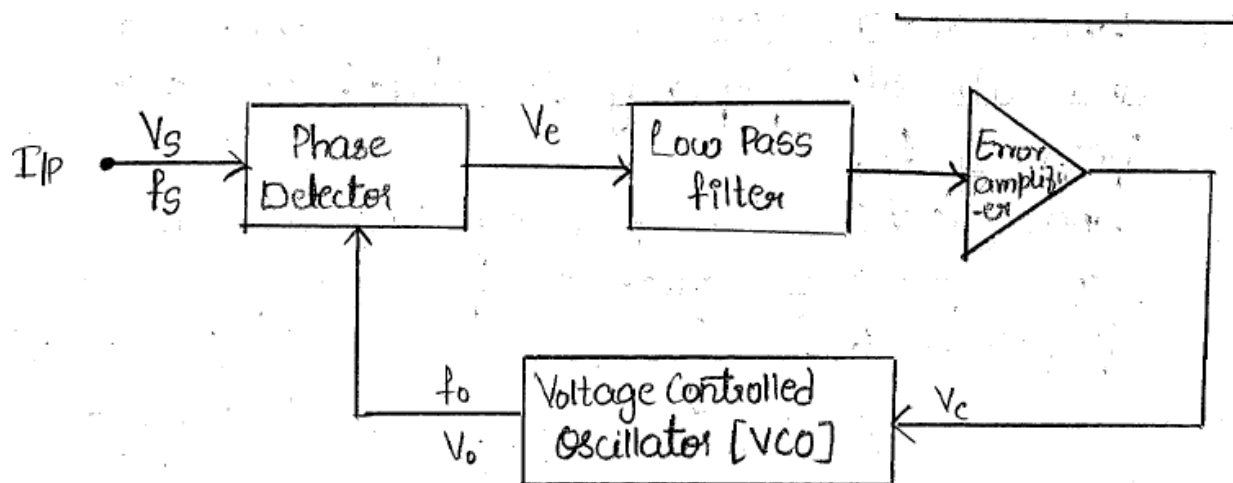


Fig ① : Block diagram of PLL

The phase-locked loop is a negative feedback system in which the frequency of an internal oscillator (vco) is matched to the frequency of an external waveform with some Pre-defined phase difference.

PLL is a feedback System Consists of :

- 1] Phase detector
- 2] Low-Pass filter
- 3] Error amplifier
- 4] Voltage Controlled Oscillator [VCO].

* The VCO is a free running multivibrator which operates at a frequency ' f_0 ' [determined by an external timing resistor and a external capacitor] called free running frequency.

k

* A VCO is an oscillator ckt in which the O/P frequency ' f_0 ' can be controlled by an externally applied voltage. The VCO provides the linear relationship between the applied voltage and the oscillator frequency. The applied voltage is called Control Voltage ' V_c '.

{ When $V_c = 0$, VCO is in free-running mode and its O/P frequency is called as Center frequency ' f_0 '.

When $V_c \neq 0$, VCO frequency will shift to some other frequency called ' f ' from a free running frequency ' f_0 '. }

* Let an input signal of amplitude ' V_s ' & frequency ' f_s ' be applied to the PLL. The phase detector compares the phase and frequency of the incoming signal to that of the O/P ' V_0 ' of the VCO.

* If there is a difference in either the frequency or in phase or in both, then phase detector generates an error voltage V_e .

The phase detector produces the sum [$f_s + f_0$] and differences [$f_s - f_0$] components at its O/P. The high

frequency component ($f_s + f_o$) is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage ' V_c ' at VCO.

* The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s & f_o . As soon as this happens, then PLL is said to be in capture range.

* The VCO continues to change frequency till its O/P frequency becomes equal to the IP signal frequency. The ckt is said to be locked.

Once the PLL is locked, the O/P frequency of VCO i.e. f_o is identical to f_s except for a finite phase difference ϕ .

* After achieving locking, the PLL then tracks the frequency changes in the input signal.

Thus, a PLL goes through three stages:

i] free running ii] Capture and iii] Locked or tracking

Some of the important definitions in relation to PLL are:

Lock-in Range: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which

the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_o , the VCO frequency.

Capture Range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o .

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

Salient Features of 565 PLL:

1. Operating frequency range = 0.01Hz to 500KHz
2. Operating voltage range = $\pm 6\text{V}$ to $\pm 12\text{V}$
3. Input level required for tracking:
10mv rms min to 3v peak to peak max
4. Input impedance = 10k Ω typically.
5. Output sink current : 1mA typically.
6. Output source current: 10mA typically
7. Drift in VCO Centre frequency: 300 PPM/ $^{\circ}\text{C}$
8. Drift in VCO Centre frequency with supply voltage: 1.5 percent/ V_{max}
9. Triangle wave amplitude: $2.4 V_{\text{pp}}$ at $\pm 6\text{V}$ supply voltage.
10. Square wave amplitude: $5.4 V_{\text{pp}}$ at $\pm 6\text{V}$ supply voltage.
11. Bandwidth adjustment range: $< \pm 1$ to $\pm 60\%$

PLL APPLICATIONS:

- Analog and digital modulation
- Frequency shift keying (FSK) decoders
- AM modulation / demodulation
- FM modulation / demodulation
- Frequency synthesis
- Frequency generation

Voltage Controlled Oscillator(IC 566):

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage

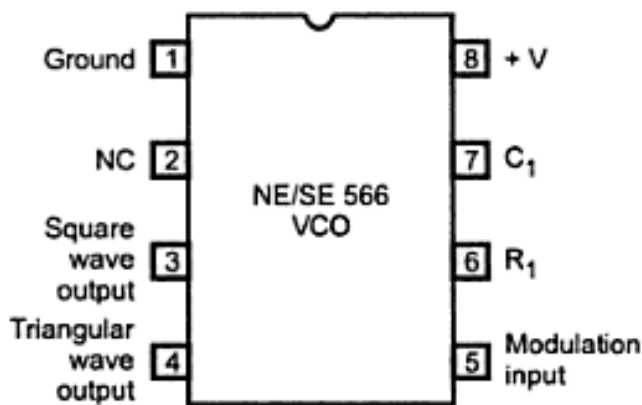


Fig. Pin diagram of IC 566 VCO

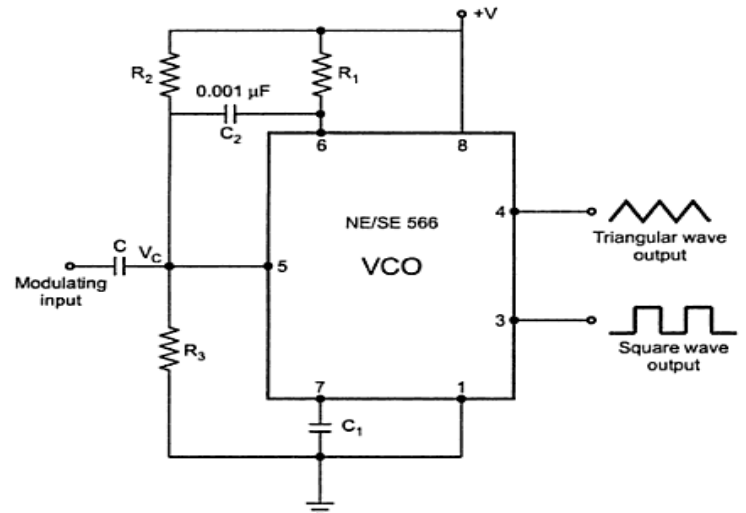


Fig. Typical connection diagram of 566 VCO

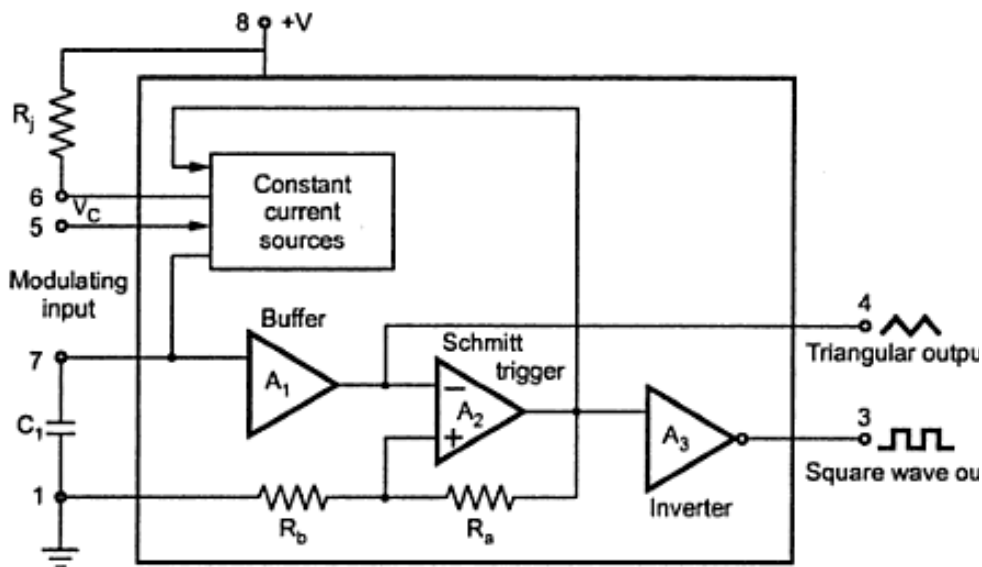


Fig. Block diagram of NE/SE 566 VCO

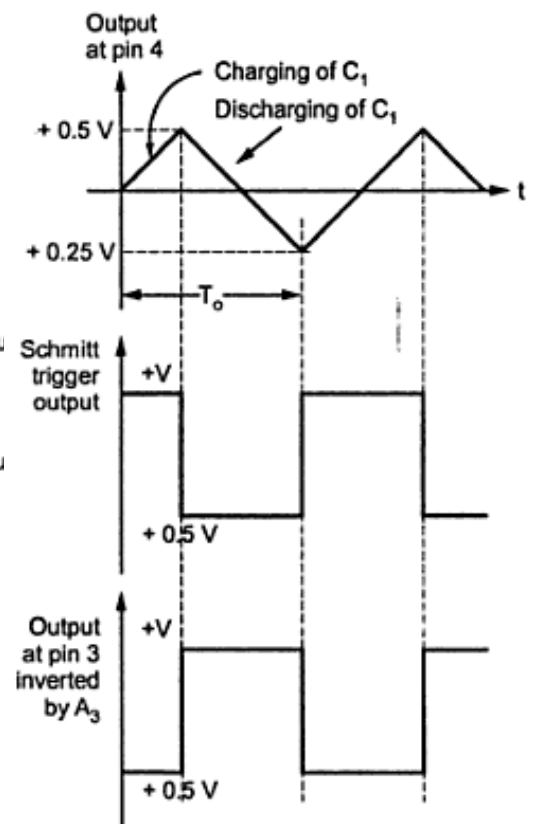


Fig. Waveforms for VCO

VCO Analysis:

Derivation of Voltage to Frequency Conversion Factor

The voltage to frequency conversion factor is an important factor of IC of 566. It is denoted as K_v , and defined as,

$$K_v = \frac{\Delta f_o}{\Delta V_C} \quad \dots(1)$$

Here ΔV_C is the change in control voltage producing corresponding change of Δf_o in the frequency.

Let f'_o = New frequency
 f_o = Original frequency ...(2)

$$\therefore \Delta f_o = f'_o - f_o$$

While V_C is changed by ΔV_C to achieve this,

From the expression of f_o ,

$$f'_o = \frac{2 [+V - (V_C - \Delta V_C)]}{C_1 R_1 (+V)} \quad \dots(3)$$

and $f_o = \frac{2 [+V - V_C]}{C_1 R_1 (+V)} \quad \dots(4)$

$$\therefore \Delta f_o = f_2 - f_1 = \frac{2 \Delta V_C}{R_1 C_1 (+V)} \quad \dots(5)$$

$$\therefore \Delta V_C = \frac{R_1 C_1 \Delta f_o (+V)}{2} \quad \dots(6)$$

With no modulating input voltage,

Control voltage $V_C = (7/8) (+V)$

if f_o is original frequency then,

$$f_o = \frac{2 \left[+V - \frac{7}{8} (+V) \right]}{R_1 C_1 (+V)} = \frac{0.25}{R_1 C_1} \quad \dots(7)$$

Using value of $R_1 C_1$ from equation (6) in equation (7),

$$f_o = \frac{0.25}{\frac{2 \Delta V_C}{\Delta f_o (+V)}}$$

$$\therefore K_v = \frac{\Delta f_o}{\Delta V_C} = \frac{f_o}{0.125 (+V)}$$

$$\therefore \boxed{K_v = \frac{8 f_o}{(+V)}} \text{ where } f_o = \text{original frequency}$$

This is the required voltage to frequency conversion factor.

Features of VCO:

Features of 566 VCO

1. Wide supply voltage range 10 V to 24 V.
2. Very linear modulation characteristics.
3. High temperature stability.
4. Excellent power supply rejection.
5. 10 to 1 frequency range with fixed C_1 .
6. The frequency can be controlled by means of current, voltage, resistor, or capacitor.

Applications of VCO:

The various applications of VCO are:

1. Frequency Modulation.
2. Signal Generation (Triangular or Square Wave)
3. Function Generation.
4. Frequency Shift Keying i.e. FSK demodulator.
5. In frequency multipliers.
6. Tone Generation.

Unit III

Data Converters

Introduction

- Most of the real world physical quantities such as voltage, current, temperature, pressure and time etc are available in analog form.
- Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store, or transmit the analog signal without introducing considerable error because of superimposition of noise as in the case of amplitude modulation.
- Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise.
- The operation of any digital communication system is based upon Analog to Digital (A/D) and Digital to Analog (D/A) conversion.
- Figure 10.1, highlights a typical application with in which A/D and D/A conversion is used.

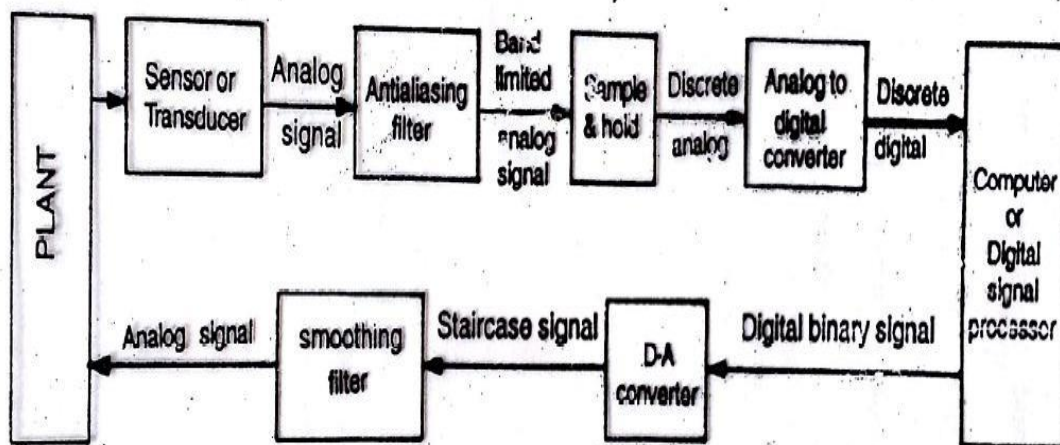


Fig. 10.1 Circuit showing application of A/D and D/A converter

- The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal.
- The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit.
- The ADC output is a sequence in binary digit. The micro-computer or Digital signal processor performs the numerical calculations of the desired control algorithm.
- The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal.
- The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit.
- The ADC output is a sequence in binary digit. The micro-computer or Digital signal processor performs the numerical calculations of the desired control algorithm.
- The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC.
- The output of a D/A converter is commonly a staircase. This staircase like output is passed through a smoothing filter to reduce the effect of quantization noise.

Applications of A/D and D/A conversion

- The scheme given in Figure 10.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multi meter, direct digital control, digital signal processing, microprocessor based instrumentation.

Basic DAC techniques

- The schematic of a DAC is shown in Figure 10.2.

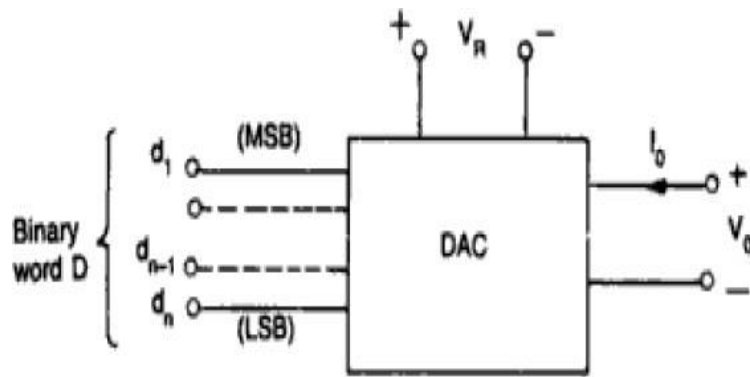


Fig. 10.2 Schematic of a DAC

- The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal.
- The output of a DAC can be either a voltage or current.
- For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = K V_{fs} (d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \dots + d_n 2^{-n}) \quad (1)$$

Where V_o = output voltage, V_{fs} = full scale output voltage

K = scaling factor usually adjusted to unity

$d_1 d_2 d_3 \dots d_n$ = n-bit binary fractional word

d_1 = MSB with weight of $V_{fs}/2$,

d_n = LSB with a weight of $V_{fs}/2^n$

- There are various ways to implement eq(1). Here we shall discuss the following resistive techniques only
 - Weighted resistor DAC
 - R-2R Ladder DAC
 - Inverted R-2R Ladder DAC

Weighted Resistor DAC:

- One of the simplest circuits shown in Figure 10.3a uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches $d_1, d_2, d_3, \dots, d_n$, controlled by Binary input word.

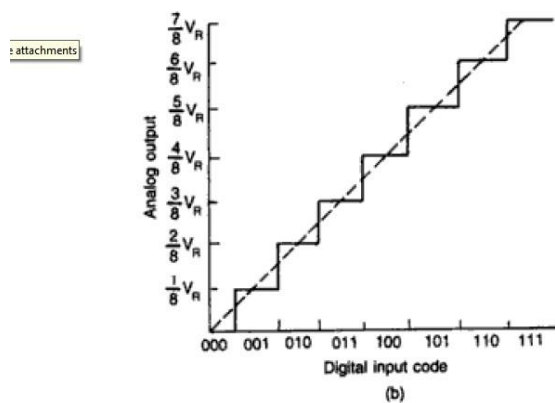
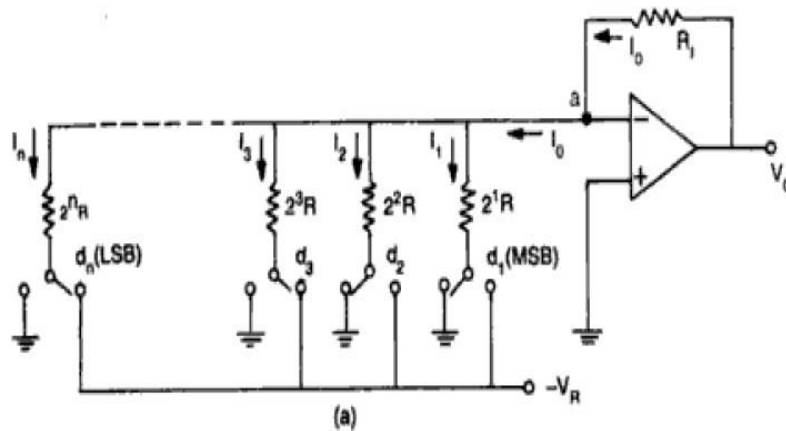


Fig. 10.3 (a) A simple weighted resistor DAC (b) Transfer characteristics of a 3-bit DAC

- These switches are single pole double throw (SPDT) type.
- If the Binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_r$). And if the input bit is zero, the switch connects the resistor to ground.
- From Figure 10.3a, the output current I_o for an ideal op-amp can be written as

$$\begin{aligned}
 I_o &= I_1 + I_2 + \dots + I_n \\
 &= (V_r / (2R)) d_1 + (V_r / (2^2 R)) d_2 + \dots + (V_r / (2^n R)) d_n \\
 &= V_r / R (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n})
 \end{aligned}$$

The output voltage

$$V_o = I_o R_f = V_r R_f / R (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}) \quad (2)$$

- Comparing eq(1) with eq(2), we get

if $R_f = R$, then $K=1$, and $V_{fs} = V_r$

- The circuit shown in Figure 10.3a uses a –ve reference voltage. The analog output voltage is therefore +ve staircase as shown in Figure 10.3b for a 3-bit weighted resistor DAC.
- It may be noted that
 - Although the op-amp in Figure 10.3a is connected in inverting mode, it can also be connected in non-inverting mode.
 - The op-amp is simply working as a current-to-voltage converter.
 - The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be +5V and the output will be –ve.

Problems with Weighted Resistor DAC

- The accuracy and stability of a DAC depends up on the accuracy of the resistors and tracking of each other with temperature.
- There are, however, a number of problems associated with this type of DAC.
- One of the disadvantages of Binary weighted resistor type DAC is the wide range of resistor values required.
- It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bits increases, the range of resistance value increases.
- For 8-bit DAC, the resistors required are $2^1 R$, $2^2 R$, -----, $2^8 R$. The largest resistor is 128 times the smallest one for only 8-bit DAC.
- For a 12-bit DAC, the largest resistance required is 5.12 M Ω if the smallest is 2.5K Ω .
- The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy.
- The choice of smallest resistor value as 2.5 K Ω is reasonable, otherwise loading effect will be there.
- The difficult of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8 bits.

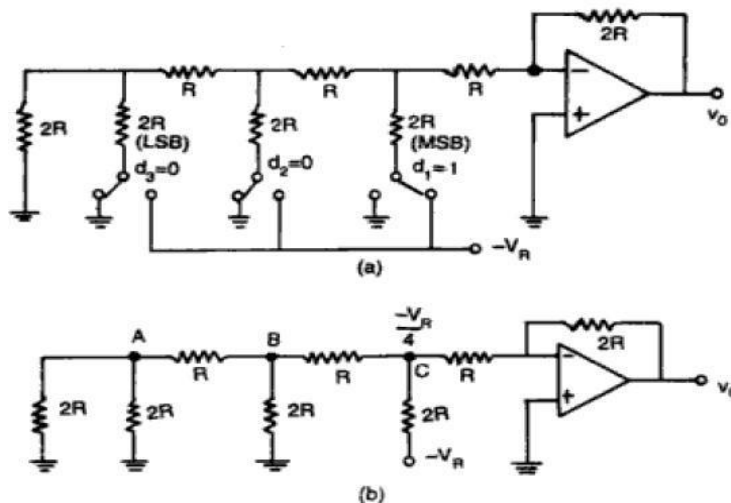
R-2R Ladder DAC:

- Wide range of resistors are required in Binary Weighted Resistor type DAC. This can be avoided by using R-2R Ladder type DAC where only two values of resistors are required.
- It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 KΩ to 10KΩ.
- For simplicity, consider a 3-bit DAC as shown in Figure 10.5a, where the switch position $d_1 d_2 d_3$ corresponds to the Binary word 100.
- The circuit can be simplified to the equation form of Figure 10.5b and finally to Figure 10.5c.
- Then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$-V_r ((2/3) R) / (2R + (2/3)R) = -V_r/4$$

- The output voltage

$$V_o = -2R/R(-V_r/4) = V_r/2 = V_{fs}/2$$



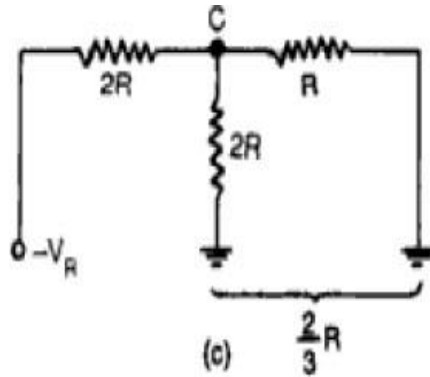


Fig. 10.5 (a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

A/D Converters

- The block schematic of ADC shown in Figure 10.9 provides the function just opposite to that of a DAC.

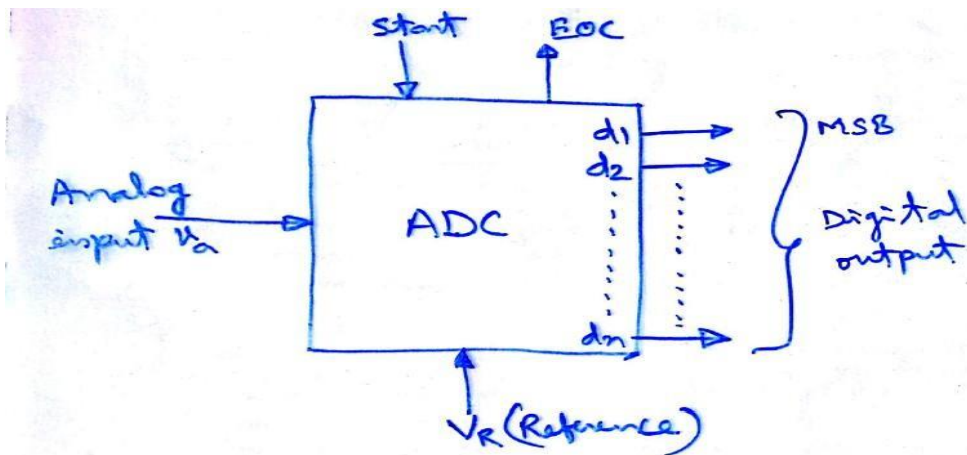


Fig 10.9 Functional diagram of ADC.

- It accepts an analog input voltage V_a and produces an output binary word $d_1 d_2 \dots d_n$ of functional value D , so that

$$D = d_1 2^{n-1} + d_2 2^{n-2} + \dots + d_n 2^0$$

where d_1 is the MSB and d_n is the LSB.

- An ADC usually has two additional control lines: the START input to tell the ADC when to start the conversion and EOC (end of conversion) output to announce when the conversion is complete.
- Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.
- ADCs are classified broadly into two groups according to their conversion technique
 - Direct type ADCs
 - Integrating type ADCs
- Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes
 - Flash (comparator) type converter
 - Counter type converter
 - Tracking or servo converter
 - Successive approximation type converter
- Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:
 - Charge balancing ADC
 - Dual slope ADC

Successive Approximation Converter

- The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods.
- For example, an 8-bit converter would require eight clock pulses to obtain a digital output. Figure 10.13 shows an 8-bit converter.

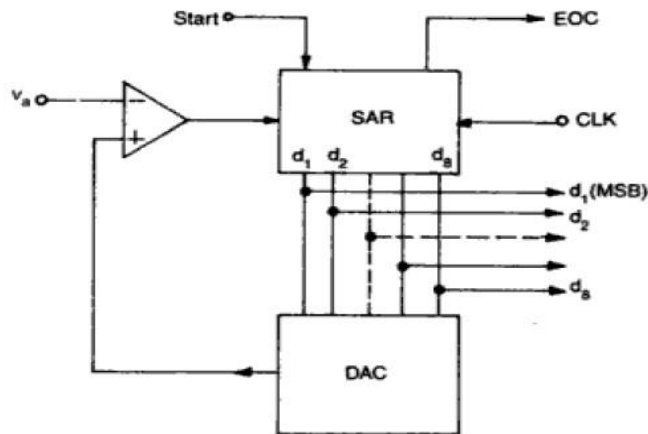


Fig. 10.13 Functional diagram of the successive approximation ADC

- The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error.

Circuit Operation:

- With the arrival of the START command the SAR sets the MSB $d_1=1$, with all other bits to zero so that the trial code is 10000000.
- The output V_d of the DAC is now compared with analog input V_a .
- If V_a is greater than the DAC output V_d , then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.
- However, if V_a is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to zero and go on to the next lower significant bit.
- This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested.
- Whenever the DAC output crosses V_a , the comparator changes state and this can be taken as the end of conversion (EOC) command.
- Figure 10.14a shows a typical conversion sequence and Figure 10.14b shows the associated waveforms.

Correct digital representation	Successive approximation register output V_d at different stages in the conversion	Comparator output
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 10.14 (a) Successive approximation conversion sequence for a typical analog input

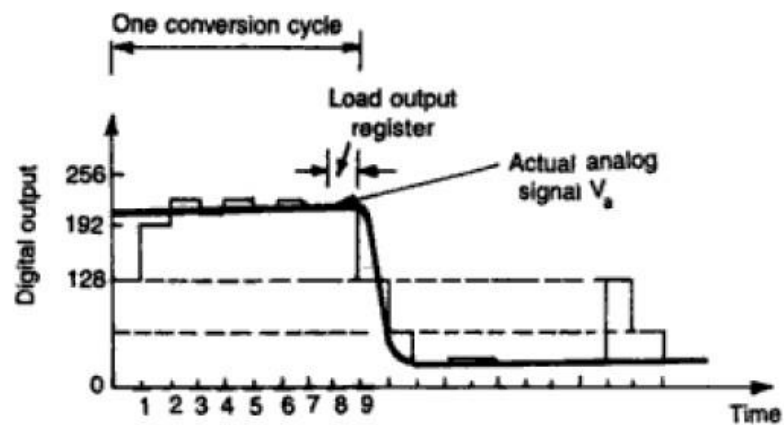
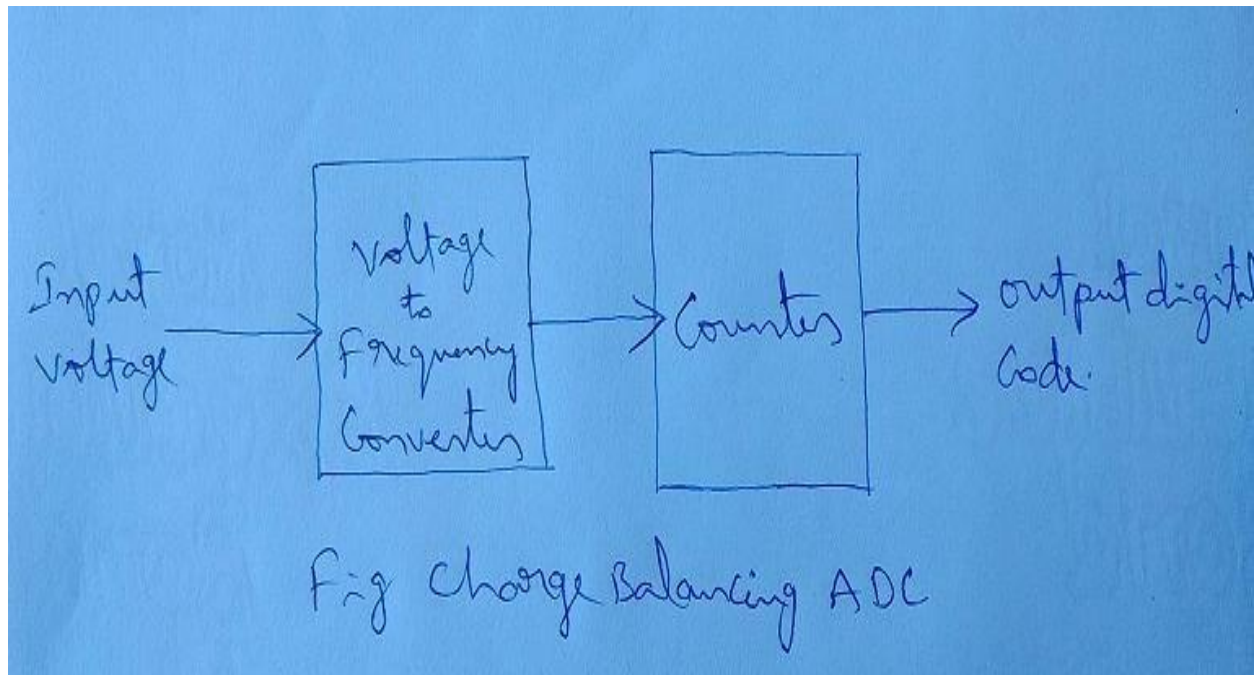


Fig. 10.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

- It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage.
- It requires 8 pulses to establish the accurate output regardless of the value of the analog input.
- However, one additional clock pulse is used to load the output register and reinitialize the circuit.
- The AD7592 (Analog Devices Co.), a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.

Charge Balancing ADC

- The figure showing this type of conversion is shown below.



- The principle of charge balancing ADC is to first convert the input signal to a frequency using a voltage to frequency converter.
- This frequency is then measured by a counter and converted to an output code proportional to the analog input.
- The main advantage of these converters is that it is possible to transmit frequency even in noisy environment or in isolated form.
- However the limitation of the circuit is that the output of V/F converter depends upon an RC product whose value cannot be easily maintained with temperature and time.
- The drawback of the charge balancing ADC is eliminated by the Dual slope conversion.

DAC/ADC Specifications

- Both D/A and A/D converters are available with wide range of specifications.

- The various important specifications of converters generally specified by the manufacturers are analyzed
- The specifications are Resolution, Linearity, Accuracy, Monotonicity, settling time and stability.

Resolution:

- The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter.
- For example, an 8-bit D/A converter has $2^8 - 1 = 255$ equal intervals. Hence the smallest change in output voltage is $1/255$ of the full scale output range. In short, the resolution is the value of the LSB.

$$\text{Resolution (in volts)} = V_{fs} / ((2^n) - 1)$$

Linearity:

- The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics.
- In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear.

Accuracy:

- Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.
- Relative accuracy is the maximum deviation after gain and offset errors have been removed.

Monotonicity:

- A monotonic DAC is the one whose analog output increases for an increase in digital input.
- A monotonic characteristic is essential in control applications, otherwise oscillations can result.

Settling time:

- The most important dynamic parameter is the settling time.
- It represents the time it takes for the output to settle within a specified band $\pm \frac{1}{2}$ LSB of its final value following a code change at the input (usually a full scale change).
- Settling time ranges from 100 ns to 10 μ s depending on word length and type of circuit used.

Stability:

- The performance of converter changes with temperature, age and power supply variations.
- So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

UNIT-IV

DIGITAL INTEGRATED CIRCUITS

Classification of Integrated Circuits, Combinational Logic ICs – Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs, Code Converters Decoders & Encoders, Priority Encoders, Multiplexers, Demultiplexers Parity Generators/Checkers, Parallel Binary Adder/ Subtractor, Magnitude Comparators.

Classification of Integrated Circuits:

Normally bipolar junction transistors, diodes and field effect transistors are commonly used electronics component in electronic circuit. These components are interconnected along with required resistors and capacitors to form an electronic circuit. This type of circuit is known as discrete circuit as each of the components can be separated from the circuit as when required. Nowadays there is a new trend of producing electronic circuit where on a semiconductor wafer numbers of diodes, transistors, and capacitors are permanently fabricated.

As the components in this type of electronic circuit are not separable that is integrated on the semiconductor wafer, this circuit is commonly referred to as an **Integrated Circuit**. **IC** is also popularly known as chip or microchip. The number of transistors that we have been able to fit into an IC has rapidly increased since their creation, doubling approximately every 2 years. This phenomenon is known as Moore's Law, and is often cited as an explanation for the exponential growth of technology over the last 50 years.

History of Integrated Circuits

This technology was invented in the year of 1950 the by **Jack Kilby** of Texas Instruments USA and **Robert Noyce** of Fairchild Semiconductor USA. The first costumer to this new invention was the US Air Force. In the year 2000 **Jack Kilby** won the Nobel Prize in Physics for miniaturized electronic circuits. One and a half years after Kilby demonstrated his **IC** design, **Robert Noyce** of Fairchild Semiconductor Limited came up with his own **integrated circuit**. His model solved many practical problems which Kilby's device had. It was made up of silicon where as Kilby's was made up of germanium. Jack Kilby and Robert Noyce both received US patents for their part of work on integrated circuits. After several years of legal issues both companies wisely decided to cross license their technology and created a huge global market.

Classification of ICs (Integrated Circuits)

Below is the classification of **different types of ICs** basis on their chip size.

- **SSI:** Small scale integration. 3 – 30 gates per chip.
- **MSI:** Medium scale integration. 30 – 300 gates per chip.
- **LSI:** Large scale integration. 300 – 3,000 gates per chip.
- **VLSI:** Very large scale integration. More than 3,000 gates per chip.

Types of ICs (Integrated Circuits)

Based on the method or techniques used in manufacturing them, *types of ICs* can be divided into three classes:

- Thin and thick film ICs
- Monolithic ICs
- Hybrid or multichip ICs

Below is the simple explanation of different types of ICs as mentioned above.

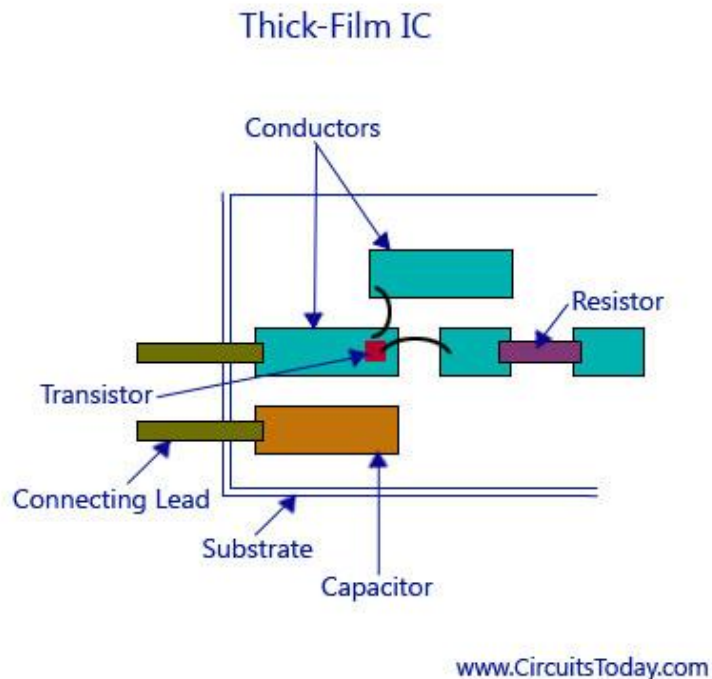
Thin and Thick ICs:

Thick and thin film IC's are comparatively larger than monolithic IC's and smaller than discrete circuits. They find their use in high power applications. Though it is a little large in size, these IC's cannot be integrated with transistors and diodes. Such devices have to be externally connected on to its corresponding pins. Passive components like resistors and capacitors can be integrated. Both thick and thin film IC's are explained in detailed below. Though both the IC's have similar appearance, properties, and general characteristics, the main difference between the two of them is the manner in which the film is deposited on to the IC.

Thin Film Integrated Circuits This IC is fabricated by depositing films of conducting material on the surface of a glass or ceramic base. The resistors are fabricated by controlling the width and thickness of the films and by using different materials selected for their resistivity. For capacitors, a film of insulating oxide is sandwiched between two conducting films. A spiral form of film is deposited onto the IC to create an inductor. Mainly two methods are used for producing thin films. One method, called vacuum evaporation is used in which vaporized material is deposited on a substrate contained in a vacuum. The other method is

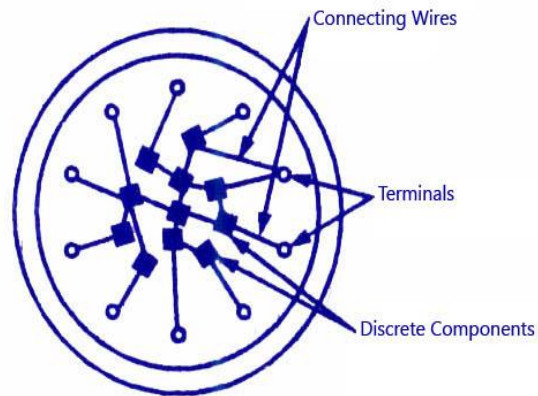
called cathode sputtering in which atoms from a cathode made of the desired film material are deposited on a substrate located between a cathode and an anode.

Thick Film Integrated Circuits They are also commonly called as printed thin film circuits. The desired circuit pattern is obtained on a ceramic substance by using a manufacturing process called silk-screen printing technique. The inks used for printing are usually materials that have resistive, conductive, or dielectric properties. They are selected accordingly by the manufacturer. The screens are actually made of fine stainless steel wire mesh. The films are fused to the substrate after printing by placing them in hot high temperature furnaces. The fabrication techniques used for thin film passive components are adopted for thick films as well. As with thin-film circuits, active components are added as separate devices. A portion of thick-film circuit is given in the figure below.



Hybrid or Multi-chip Integrated Circuits:

As the name suggests, the circuit is fabricated by interconnecting a number of individual chips. Hybrid ICs are mostly used for high power audio amplifier applications from 5 Watts to more than 50 Watts. The active components are diffused transistors or diodes. The passive components may be group of diffused resistors or capacitors on a single chip, or they may be thin-film components. Interconnection between the individual chips is made by wiring process or a metallized pattern.



Hybrid or Multichip IC

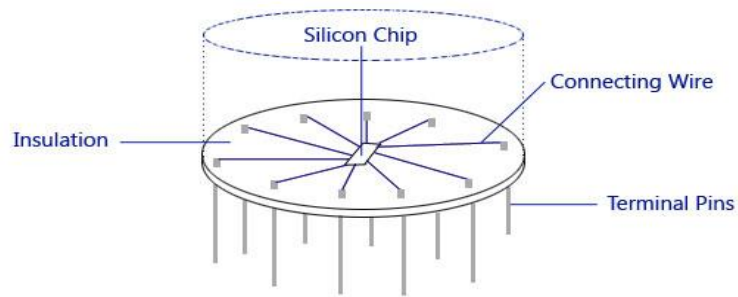
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The diagram of a hybrid or multi-chip IC is shown in the figure above. Hybrid IC's are also known to provide a better performance than monolithic IC's. Although the process is too expensive for mass production, multi-chip techniques are quite economical for small quantity production and are more often used as prototypes for monolithic ICs. Based upon the active devices employed the ICs can be classified as bipolar ICs using bipolar active devices (BJT) and unipolar IC's using unipolar active devices like FET.

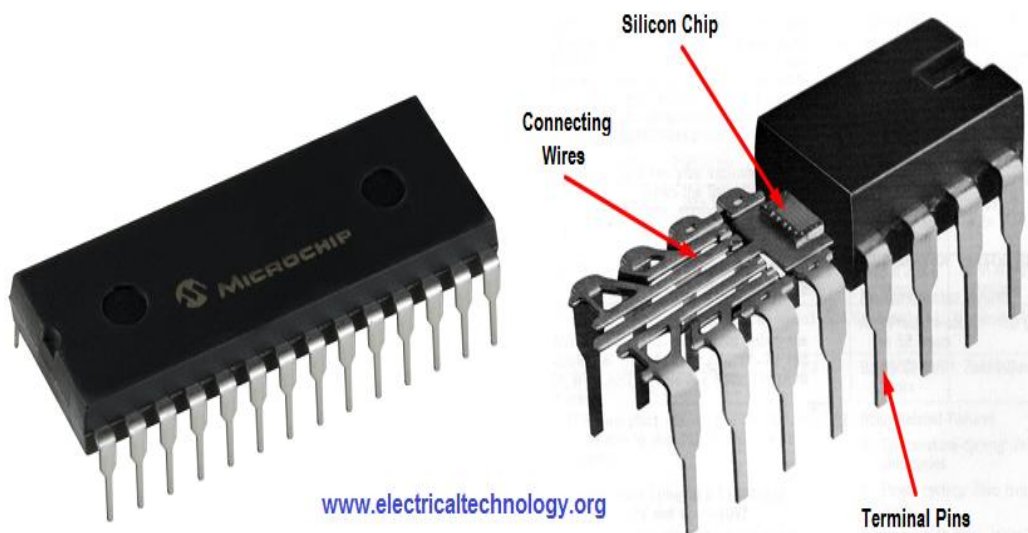
Monolithic ICs

The word 'monolithic' comes from the Greek words 'monos' and 'lithos' which means 'single' and 'stone'. As the name suggests, monolithic IC's refer to a single stone or a single crystal. The single crystal refers to a single chip of silicon as the semiconductor material, on top of which all the active and passive components needed are interconnected. This is the best mode of manufacturing IC' as they can be made identical, and produces high reliability. The cost factor is also low and can be manufactured in bulk in very less time. They have been found applicable for C's used for AM receivers, TV circuits, computer circuits, voltage regulators, amplifiers and so on. A detailed article explaining the concept and fabrication process of different components and monolithic IC production process is explained here – Monolithic Integrated Circuit.

Monolithic-IC in Can-Type Enclosure



www.CircuitsToday.com



Monolithic IC in Plastic Package (DIP)

Being as it is, monolithic IC's have some limitations as well. 1. Monolithic IC's have low power rating. They cannot be used for low power applications as they cannot have a power rating of more than 1 watt. 2. The isolation between the components inside the IC is poor. 3. Components like inductor cannot be fabricated to the IC. 4. The passive components that are fabricated inside the IC will be of small value. For higher values they have to be connected externally to the IC pins. 5. It is difficult to make a circuit flexible for any kind of variation; a new set of masks is required.

IC family Properties	Monolithic IC	Thick-thin film	Hybrid IC
Substrate	Silicon	Glass, Ceramic	(i) Glass, Ceramic (ii) Silicon
Structure	Active and passive devices along with interconnections on a single chip.	Active and passive devices on an insulating substrate along with inter connection.	(i) Passive devices and interconnections on one insulating substrate with active devices wire wound. (ii) Active devices on a single chip while passive devices along with interconnections on thick-thin film.
Active devices	(i) BJT (ii) MOSFET	MOSFET	(i) BJT, MOSFET (ii) BJT, MOSFET
Passive devices	(i) Diffused resistors, oxide capacitor (ii) MOS resistor, oxide capacitor	Metal film resistor, oxide capacitor	(i) Metal film resistor, cement resistor, oxide capacitor (ii) Metal film resistor, oxide capacitor
Application	Linear and digital IC	Digital IC	(i) Linear and digital IC (ii) Linear and digital IC

Table 1.1

Advantages of Integrate Circuit or IC

1. It is quite small in size practically around 20,000 electronic components can be incorporated in a single square inch of IC chip.
2. Many complex circuits are fabricated in a single chip and hence this simplifies the designing of a complex electronic circuit. Also it improves the performance.
3. Reliability of ICs is high
4. These are available at low cost due to bulk production.
5. ICs consume very tiny power.
6. Higher operating speed due to absence of parasitic capacitance effect.
7. Very easily replaceable from the mother circuit.

Disadvantages of Integrate Circuit or IC

1. Because of its small size, IC is unable to dissipate heat in required rate when current in it increased. That is why ICs are often damaged due to over current flowing through them.
2. Inductors and Transformers cannot be incorporated in **ICs**.

Combinational Logic ICs – Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs

74 series families

The **74LS** (Low-power Schottky) family (like the original) uses TTL (Transistor-Transistor Logic) circuitry which is fast but requires more power than later families. The 74 series is often still called the 'TTL series' even though the latest ICs do not use TTL!

The **74HC** family has High-speed CMOS circuitry, combining the speed of TTL with the very low power consumption of the [4000 series](#). They are CMOS ICs with the same pin arrangements as the older 74LS family. Note that 74HC inputs cannot be reliably driven by 74LS outputs because the voltage ranges used for logic 0 are not quite compatible, use 74HCT instead.

The **74HCT** family is a special version of 74HC with 74LS TTL-compatible inputs so 74HCT can be safely mixed with 74LS in the same system. In fact 74HCT can be used as low-power direct replacements for the older 74LS ICs in most circuits. The minor disadvantage of 74HCT is a lower immunity to noise, but this is unlikely to be a problem in most situations.

For most new projects the 74HC family is the best choice. The 74LS and 74HCT families require a 5V supply so they are not convenient for battery operation.

74LS family TTL characteristics

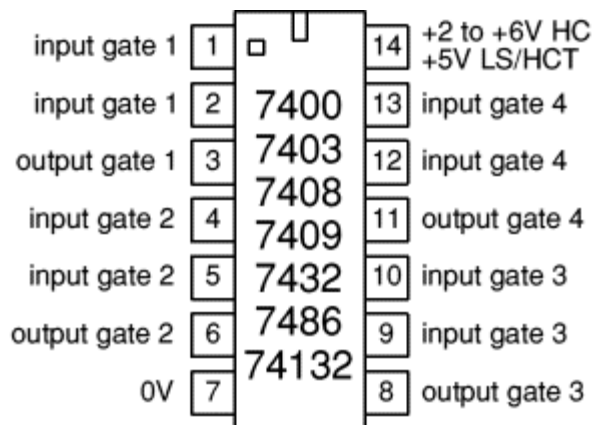
- **Supply:** 5V $\pm$ 0.25V, it must be very smooth, a regulated supply is best. In addition to the normal supply smoothing, a 0.1 μ F capacitor should be connected across the supply near the IC to remove the 'spikes' generated as it switches state, one capacitor is needed for every 4 ICs.

- **Inputs** 'float' high to logic 1 if unconnected, but do not rely on this in a permanent (soldered) circuit because the inputs may pick up electrical noise. 1mA must be drawn out to hold inputs at logic 0. In a permanent circuit it is wise to connect any unused inputs to +Vs to ensure good immunity to noise.
- **Outputs** can sink up to 16mA (enough to light an LED), but they can source only about 2mA. To switch larger currents you can connect a transistor.
- **Fan-out:** one output can drive up to 10 74LS inputs, but many more 74HCT inputs.
- **Gate propagation time:** about 10ns for a signal to travel through a gate.
- **Frequency:** up to about 35MHz (under the right conditions).
- **Power consumption** (of the IC itself) is a few mW.

74HC and 74HCT family characteristics

- The CMOS circuitry used in the **74HC** and **74HCT** series ICs means that they are static sensitive. Touching a pin while charged with static electricity (from your clothes for example) may damage the IC. In fact most ICs in regular use are quite tolerant and earthing your hands by touching a metal water pipe or window frame before handling them will be adequate. ICs should be left in their protective packaging until you are ready to use them.
- **74HC Supply:** 2 to 6V, small fluctuations are tolerated.
- **74HCT Supply:** 5V $\pm$ 0.5V, a regulated supply is best.
- **Inputs** have very high impedance (resistance), this is good because it means they will not affect the part of the circuit where they are connected. However, it also means that unconnected inputs can easily pick up electrical noise and rapidly change between high and low states in an unpredictable way. This is likely to make the IC behave erratically and it will significantly increase the supply current. To prevent problems **all unused inputs MUST be connected to the supply (either +Vs or 0V)**, this applies even if that part of the IC is not being used in the circuit!
Note that 74HC inputs cannot be reliably driven by 74LS outputs because the voltage ranges used for logic 0 are not quite compatible. For reliability use **74HCT** if the system includes some 74LS ICs.

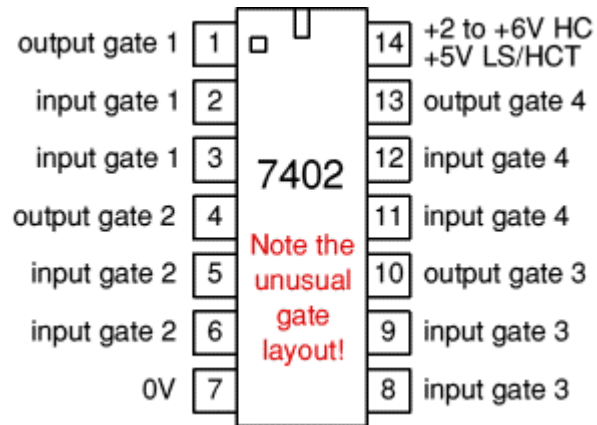
- **Outputs** can [sink and source](#) about 4mA if you wish to maintain the correct output voltage to drive logic inputs, but if there is no need to drive any inputs the maximum current is about 20mA. To switch larger currents you can [connect a transistor](#).
- **Fan-out:** one output can drive many inputs (50+), except 74LS inputs because these require a higher current and only 10 can be driven.
- **Gate propagation time:** about 10ns for a signal to travel through a gate.
- **Frequency:** up to 25MHz.
- **Power consumption** (of the IC itself) is very low, a few μW . It is much greater at high frequencies, a few mW at 1MHz for example.



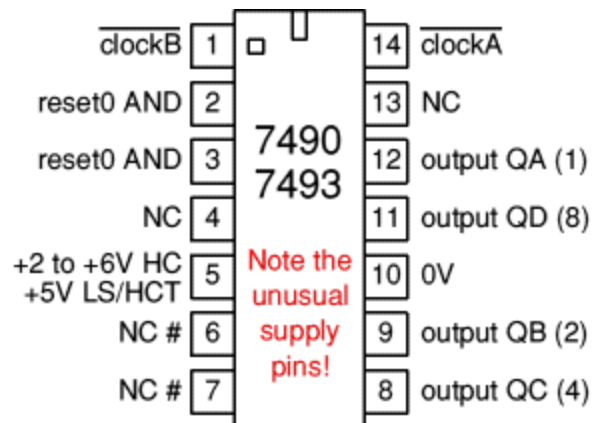
- 7400 quad 2-input NAND
- 7403 quad 2-input NAND with open collector outputs
- 7408 quad 2-input AND
- 7409 quad 2-input AND with open collector outputs
- 7432 quad 2-input OR
- 7486 quad 2-input EX-OR
- 74132 quad 2-input NAND with Schmitt trigger inputs

The 74132 has Schmitt trigger inputs to provide good noise immunity. They are ideal for slowly changing or noisy signals

7402 quad 2-input NOR



7490 decade (0-9) ripple counter



Code Converters

Numbers are usually **coded** in one form or another so as to represent or use it as required. For instance, a number 'nine' is coded in decimal using symbol (9)_d. Same is coded in natural-binary as (1001)_b. While digital computers all deal with binary numbers, there are situations wherein natural-binary representation of numbers is in-convenient or in-efficient and some other (binary) code must be used to process the numbers.

One of these other code is **gray-code**, in which any two numbers in sequence differ only by one bit **change**. This code is used in K-map reduction technique. The advantage is that when numbers are changing frequently, the logic **gates** are turning ON and OFF frequently and so are the transistors switching which characterizes power **consumption** of the circuit; since only one bit is changing from number to number, switching is reduced and hence is the power consumption.

Binary to Gray code converter

How to Convert Binary to Gray Code

1. The MSB (Most Significant Bit) of the gray code will be exactly equal to the first bit of the given binary number.
2. The second bit of the code will be exclusive-or (XOR) of the first and second bit of the given binary number, i.e if both the bits are same the result will be 0 and if they are different the result will be 1.
3. The third bit of gray code will be equal to the exclusive-or (XOR) of the second and third bit of the given binary number. Thus the binary to gray code conversion goes on. An example is given below to illustrate these steps.

Design of a 4-bit binary to gray code converter:

$$G_4 = \Sigma m(8, 9, 10, 11, 12, 13, 14, 15)$$

$$G_3 = \Sigma m(4, 5, 6, 7, 8, 9, 10, 11)$$

$$G_2 = \Sigma m(2, 3, 4, 5, 10, 11, 12, 13)$$

$$G_1 = \Sigma m(1, 2, 5, 6, 9, 10, 13, 14)$$

$$G_4 = B_4$$

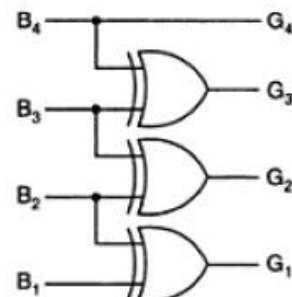
$$G_3 = \bar{B}_4 B_3 + B_4 \bar{B}_3 = B_4 \oplus B_3$$

$$G_2 = \bar{B}_3 B_2 + B_3 \bar{B}_2 = B_3 \oplus B_2$$

$$G_1 = \bar{B}_2 B_1 + B_2 \bar{B}_1 = B_2 \oplus B_1$$

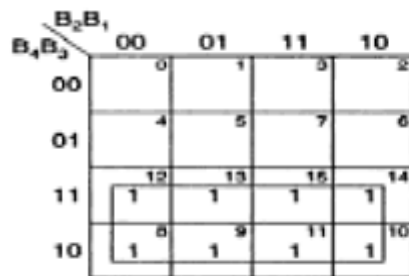
4-bit binary				4-bit Gray			
B ₄	B ₃	B ₂	B ₁	G ₄	G ₃	G ₂	G ₁
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

(a) Conversion table

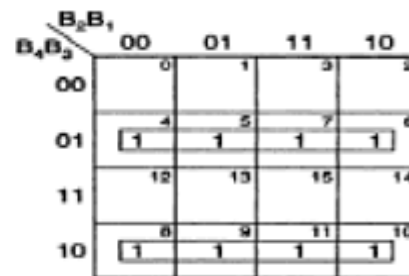


(c) Logic diagram

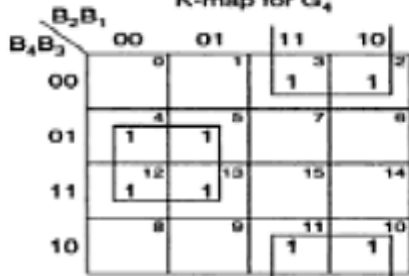
4-bit binary-to-Gray code converter



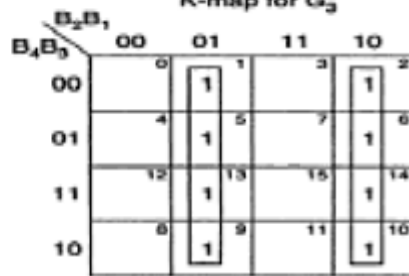
$G_4 = B_4$
K-map for G_4



$G_3 = B_4 \oplus B_3$
K-map for G_3



$G_2 = B_3 \oplus B_2$
K-map for G_2



$G_1 = B_2 \oplus B_1$
K-map for G_1

(b) K-maps

4-bit binary-to-Gray code converter.

Gray to Binary Code Converter:

Design of a 4-bit gray to Binary code converter:

$$B_4 = \Sigma m(12, 13, 15, 14, 10, 11, 9, 8) = \Sigma m(8, 9, 10, 11, 12, 13, 14, 15)$$

$$B_3 = \Sigma m(6, 7, 5, 4, 10, 11, 9, 8) = \Sigma m(4, 5, 6, 7, 8, 9, 10, 11)$$

$$B_2 = \Sigma m(3, 2, 5, 4, 15, 14, 9, 8) = \Sigma m(2, 3, 4, 5, 8, 9, 14, 15)$$

$$B_1 = \Sigma m(1, 2, 7, 4, 13, 14, 11, 8) = \Sigma m(1, 2, 4, 7, 8, 11, 13, 14)$$

$$B_4 = G_4$$

$$B_3 = \bar{G}_4 G_3 + G_4 \bar{G}_3 = G_4 \oplus G_3$$

$$B_2 = \bar{G}_4 G_3 \bar{G}_2 + \bar{G}_4 \bar{G}_3 G_2 + G_4 \bar{G}_3 \bar{G}_2 + G_4 G_3 G_2$$

$$= \bar{G}_4 (G_3 \oplus G_2) + G_4 (\bar{G}_3 \oplus \bar{G}_2) = G_4 \oplus G_3 \oplus G_2 = B_3 \oplus G_2$$

$$B_1 = \bar{G}_4 \bar{G}_3 \bar{G}_2 G_1 + \bar{G}_4 \bar{G}_3 G_2 \bar{G}_1 + \bar{G}_4 G_3 \bar{G}_2 G_1 + \bar{G}_4 G_3 G_2 \bar{G}_1 + G_4 \bar{G}_3 \bar{G}_2 G_1 + G_4 \bar{G}_3 G_2 \bar{G}_1 + G_4 G_3 \bar{G}_2 G_1 + G_4 G_3 G_2 \bar{G}_1$$

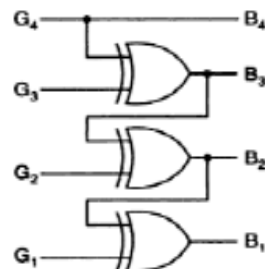
$$= \bar{G}_4 \bar{G}_3 (G_2 \oplus G_1) + G_4 G_3 (G_2 \oplus G_1) + \bar{G}_4 G_3 (\bar{G}_2 \oplus \bar{G}_1) + G_4 \bar{G}_3 (\bar{G}_2 \oplus \bar{G}_1)$$

$$= (G_2 \oplus G_1)(\bar{G}_4 \oplus G_3) + (\bar{G}_2 \oplus \bar{G}_1)(G_4 \oplus G_3)$$

$$= G_4 \oplus G_3 \oplus G_2 \oplus G_1$$

4-bit Gray				4-bit binary			
G_4	G_3	G_2	G_1	B_4	B_3	B_2	B_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

(a) Conversion table



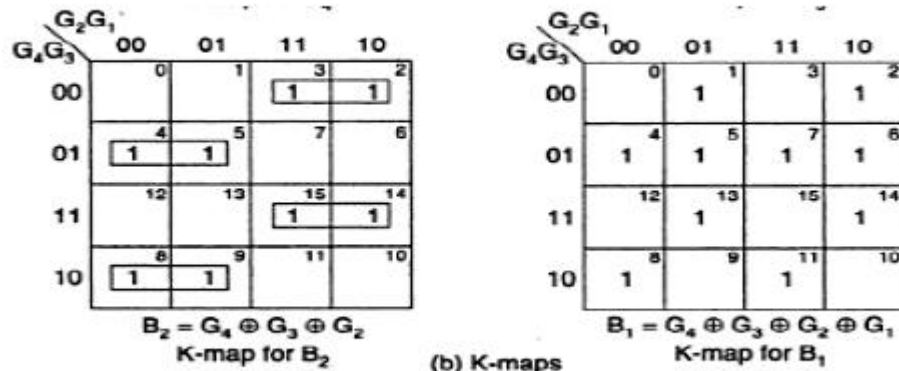
(c) Logic diagram

$G_4 G_3 \backslash G_2 G_1$	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

$B_4 = G_4$
K-map for B_4

$G_4 G_3 \backslash G_2 G_1$	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

$B_3 = G_4 \oplus G_3$
K-map for B_3



4-bit Gray-to-binary code converter.

Design of a 4-bit BCD to XS-3 code converter:

8421 code				XS-3 code			
B_4	B_3	B_2	B_1	X_4	X_3	X_2	X_1
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

(a) Conversion table

$$\begin{aligned}
 X_4 &= \sum m(5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15) \\
 X_3 &= \sum m(1, 2, 3, 4, 9) + d(10, 11, 12, 13, 14, 15) \\
 X_2 &= \sum m(0, 3, 4, 7, 8) + d(10, 11, 12, 13, 14, 15) \\
 X_1 &= \sum m(0, 2, 4, 6, 8) + d(10, 11, 12, 13, 14, 15)
 \end{aligned}$$

The minimal expressions are

$$X_4 = B_4 + B_3B_2 + B_3B_1$$

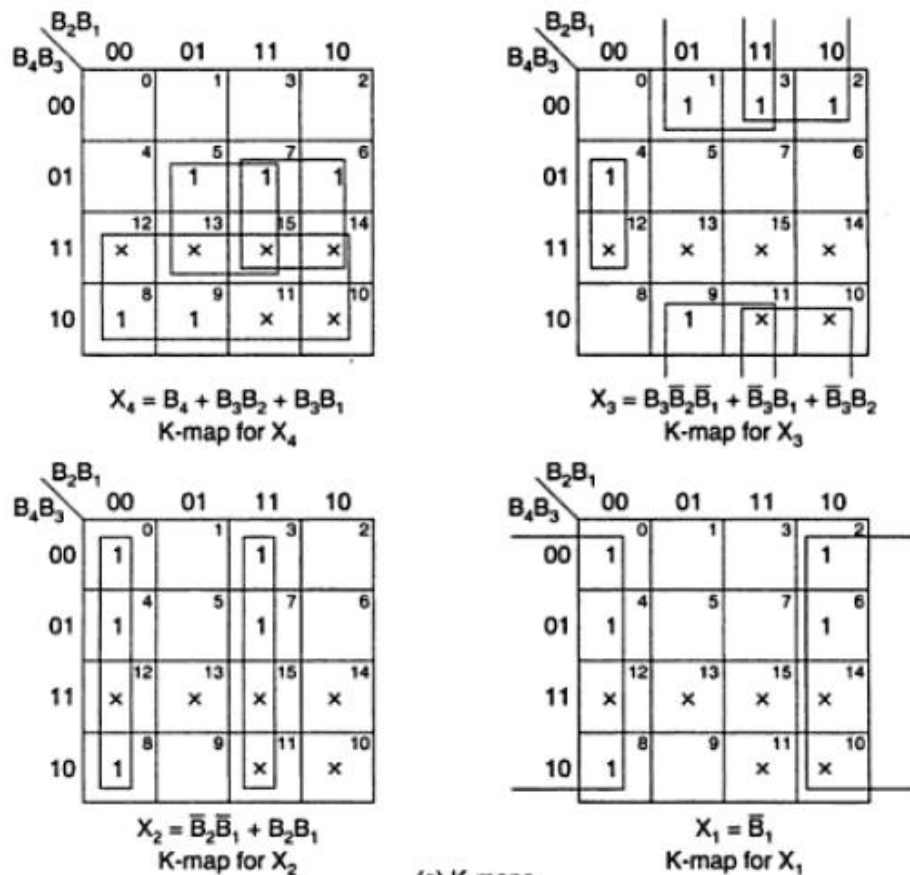
$$X_3 = B_3\bar{B}_2\bar{B}_1 + \bar{B}_3B_1 + \bar{B}_3B_2$$

$$X_2 = \bar{B}_2\bar{B}_1 + B_2B_1$$

$$X_1 = \bar{B}_1$$

(b) Minimal expressions

4-bit BCD-to-XS-3 code converter



Application of Gray Code

The gray code is used in a few specific applications. The main applications include being used in analog to digital converters, as well as being used for error correction in digital communication. Gray code is used to minimize errors in converting analog signals to digital signals.

Advantages of Gray Code

- Better for error minimization in converting analog signals to digital signals
- Reduces the occurrence of “Hamming Walls” (an undesirable state) when used in genetic algorithms
- Can be used to in to minimize a logic circuit
- Useful in clock domain crossing

Disadvantages of Gray Code

- Not suitable for arithmetic operations
- Limited practical use outside of a few specific applications

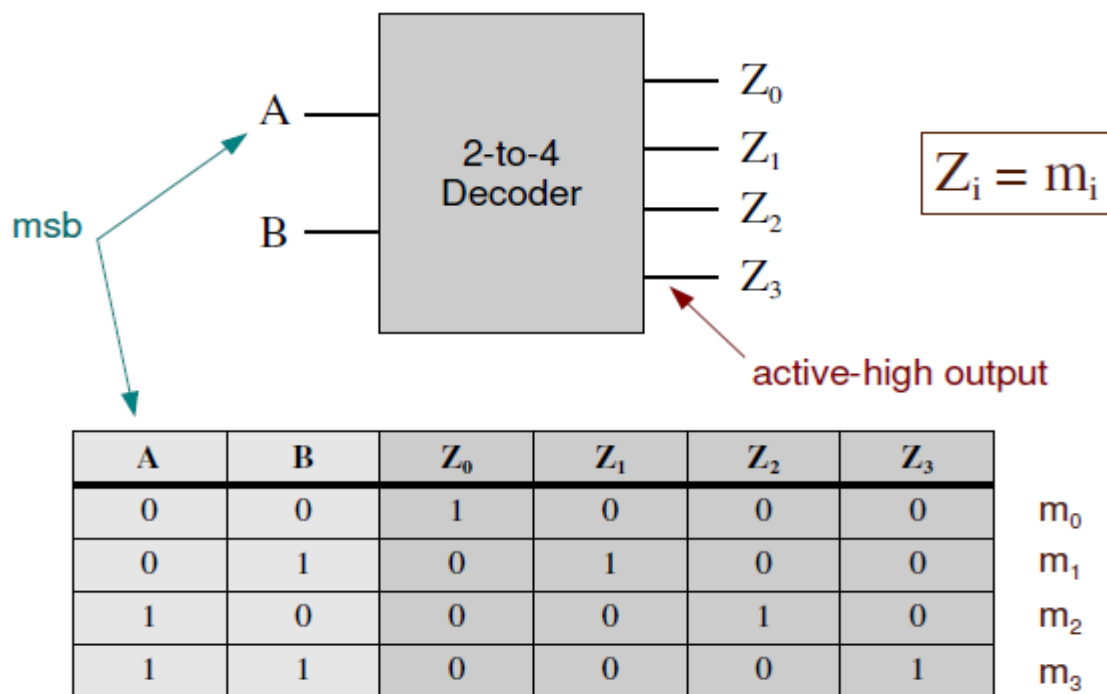
Decoders

- A decoder has – n inputs – 2^n outputs
- A decoder selects one of 2^n outputs by decoding the binary value on the n inputs.
- The decoder generates all of the minterms of the n input variables. – Exactly one output will be active for each combination of the inputs.

Applications:

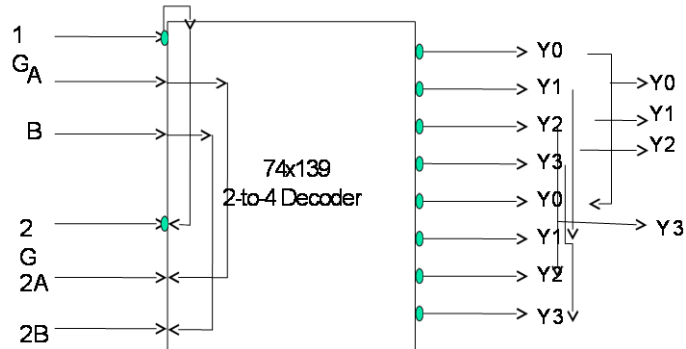
- It is used to implement Combinational circuit.
- It is used to convert BCD to 7-segment code.
- It is used in memories to select particular register.

2*4 DECODER

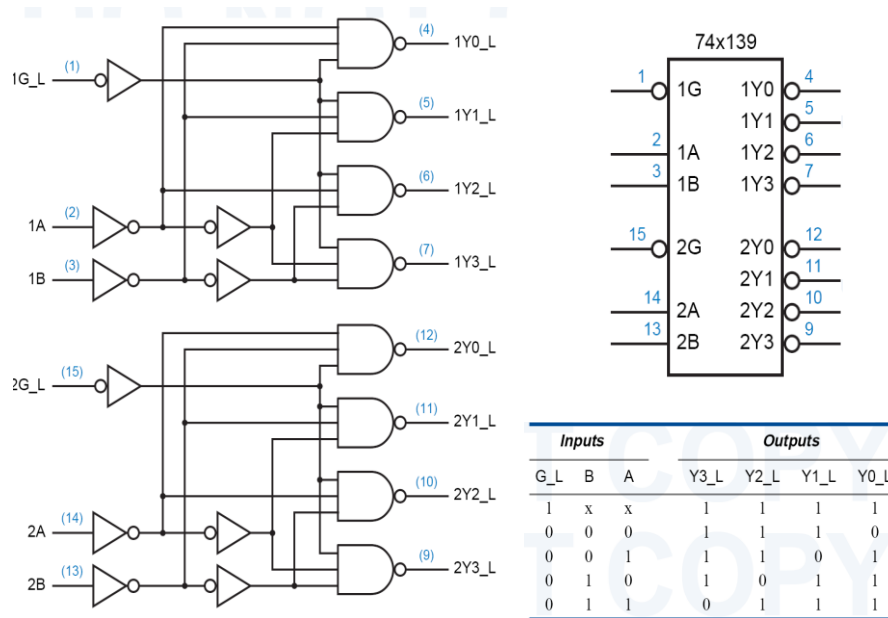




2 to 4 Decoder using IC 74x139



74x139 dual 2-to-4 decoder



3-to-8 line decoder: For each possible input combination, there are seven outputs that are equal to 0 and only one that is equal to 1.

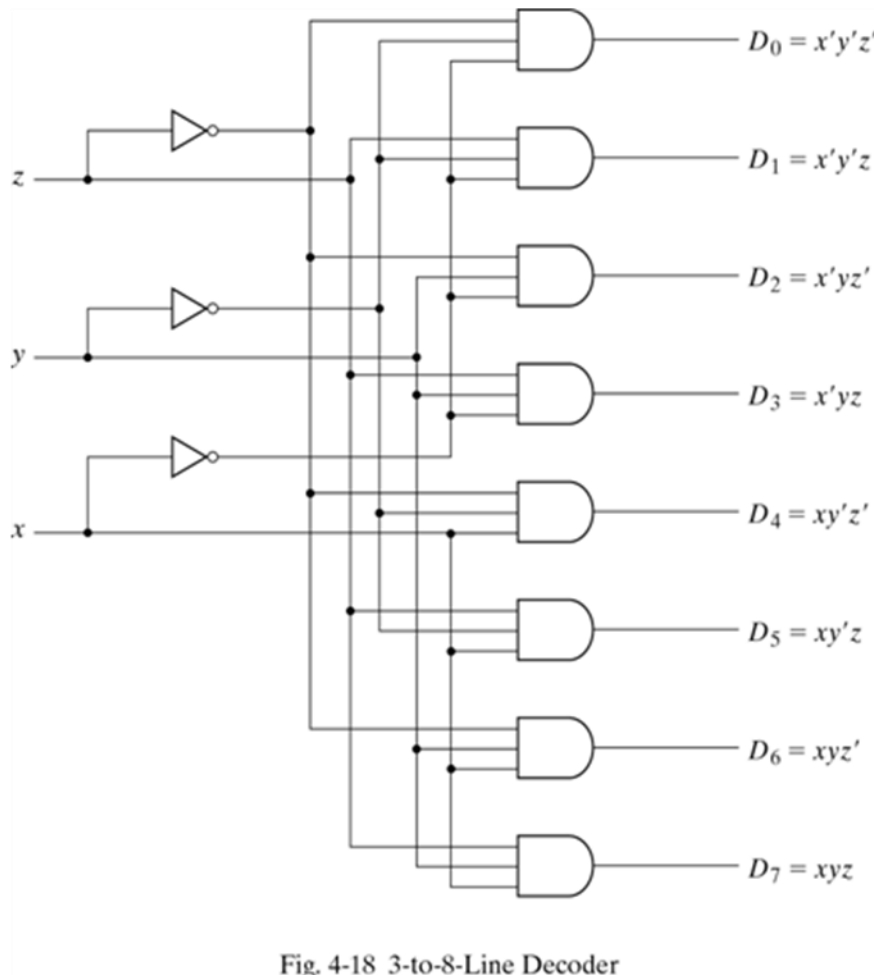
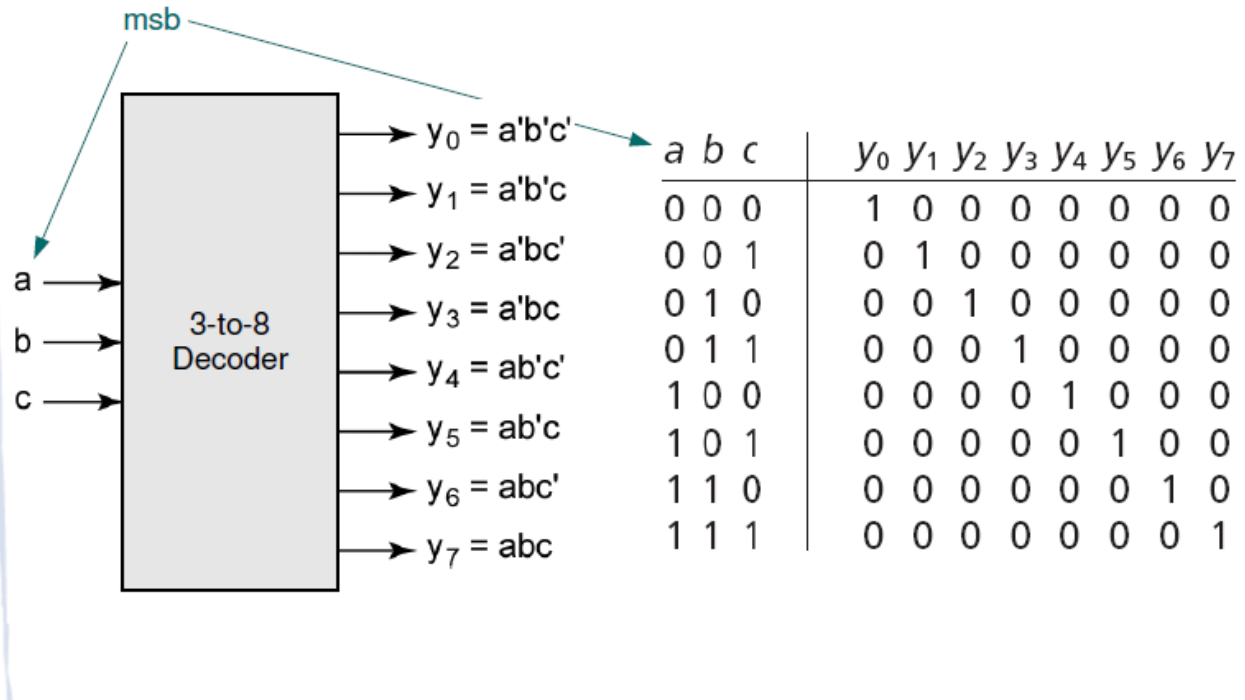
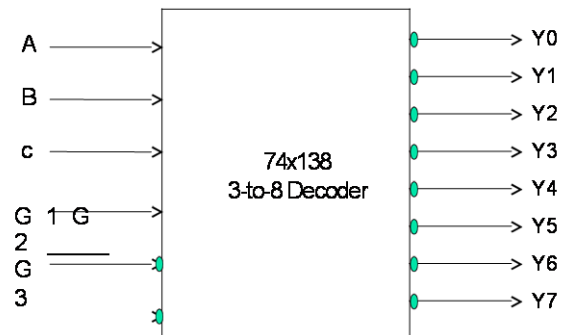


Fig. 4-18 3-to-8-Line Decoder

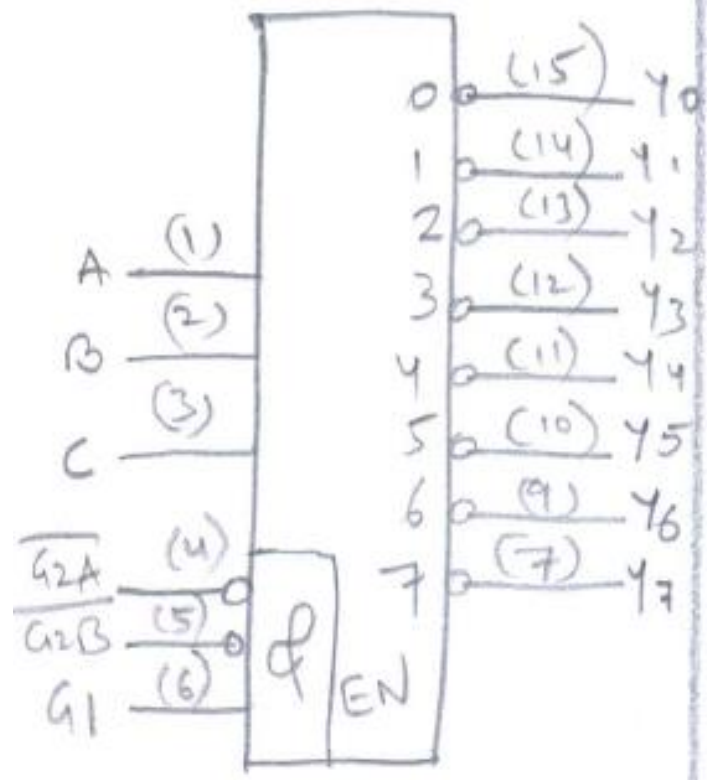
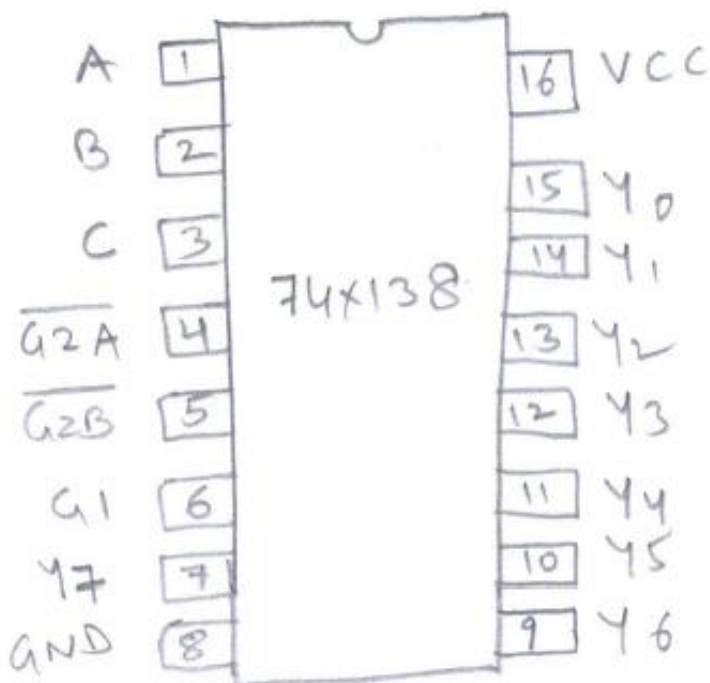


3 to 8 Decoder IC 74x138



38

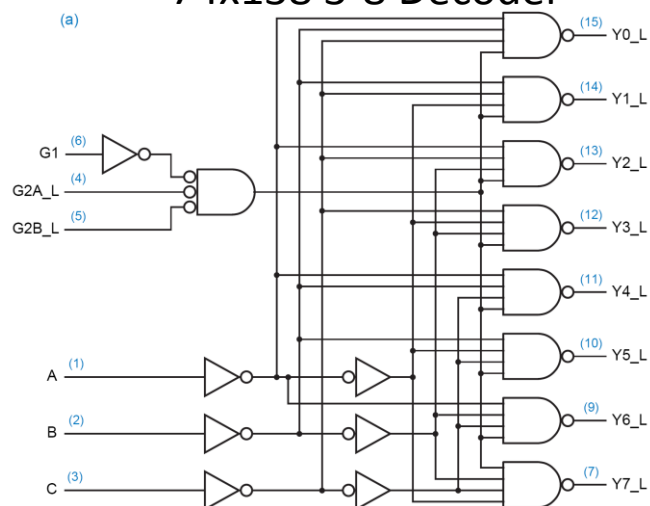
3-line to 8-line decoder(3 X 8)-74HC138



Function Table

Decimal Digit	Inputs			Binary Inputs			Outputs							
	$\overline{G_{2B}}$	$\overline{G_{2A}}$	G_1	C	B	A	$\overline{Y_7}$	$\overline{Y_6}$	$\overline{Y_5}$	$\overline{Y_4}$	$\overline{Y_3}$	$\overline{Y_2}$	$\overline{Y_1}$	$\overline{Y_0}$
X	1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	0	1	0	0	0	1	1	1	1	1	1	1	0
1	0	0	1	0	0	1	1	1	1	1	1	1	0	1
2	0	0	1	0	1	0	1	1	1	1	1	0	1	1
3	0	0	1	0	1	1	1	1	1	1	0	1	1	1
4	0	0	1	1	0	0	0	1	1	0	1	1	1	1
5	0	0	1	1	0	1	1	1	0	1	1	1	1	1
6	0	0	1	1	1	0	1	0	1	1	1	1	1	1
7	0	0	1	1	1	1	0	1	1	1	1	1	1	1

74x138 3-8 Decoder



4*16 Decoder

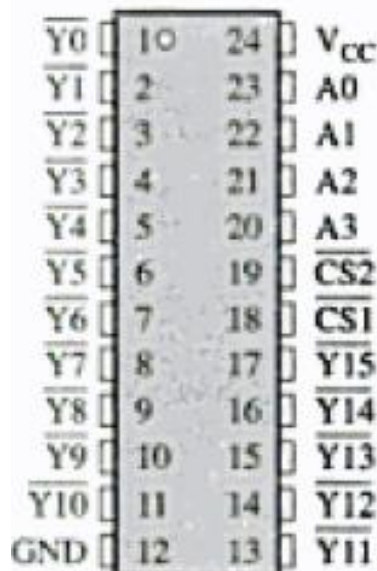
4-line to 16-line decoder(4 X 16)-74HC154

In order to decode all possible combinations of four bits, sixteen decoding gates are required ($2^4 = 16$). This type of decoder is commonly called either a *4-line-to-16-line decoder* because there are four inputs and sixteen outputs or a *1-of-16 decoder* because for any given code on the inputs, one of the sixteen outputs is activated. A list of the sixteen binary codes and their corresponding decoding functions is given in Table 6-4.

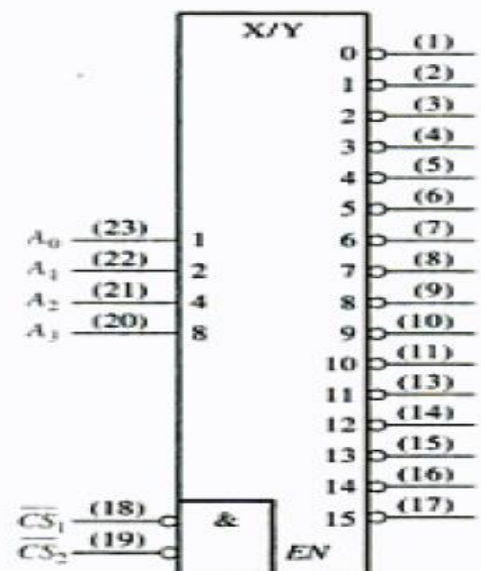
If an active-LOW output is required for each decoded number, the entire decoder can be implemented with NAND gates and inverters. In order to decode each of the sixteen binary codes, sixteen NAND gates are required (AND gates can be used to produce active-HIGH outputs).

The 74HC154 is a good example of an IC decoder. The logic symbol is shown in Figure 6-32. There is an enable function (*EN*) provided on this device, which is implemented with a NOR gate used as a negative-AND. A LOW level on each chip select input, $\overline{CS}_1$ and $\overline{CS}_2$, is required in order to make the enable gate output (*EN*) HIGH. The enable gate output is connected to an input of *each* NAND gate in the decoder, so it must be HIGH for the NAND gates to be enabled. If the enable gate is not activated by a LOW on both inputs, then all sixteen decoder outputs (*Y*) will be HIGH regardless of the states of the four input variables, A_0 , A_1 , A_2 , and A_3 .

Pin Diagram



Logic Diagram



A logic symbol for a 4-line-to-16-line (1-of-16) decoder with active-LOW outputs is shown in Figure 6-31. The BIN/DEC label indicates that a binary input makes the corresponding decimal output active. The input labels 8, 4, 2, and 1 represent the binary weights of the input bits ($2^3 2^2 2^1 2^0$).

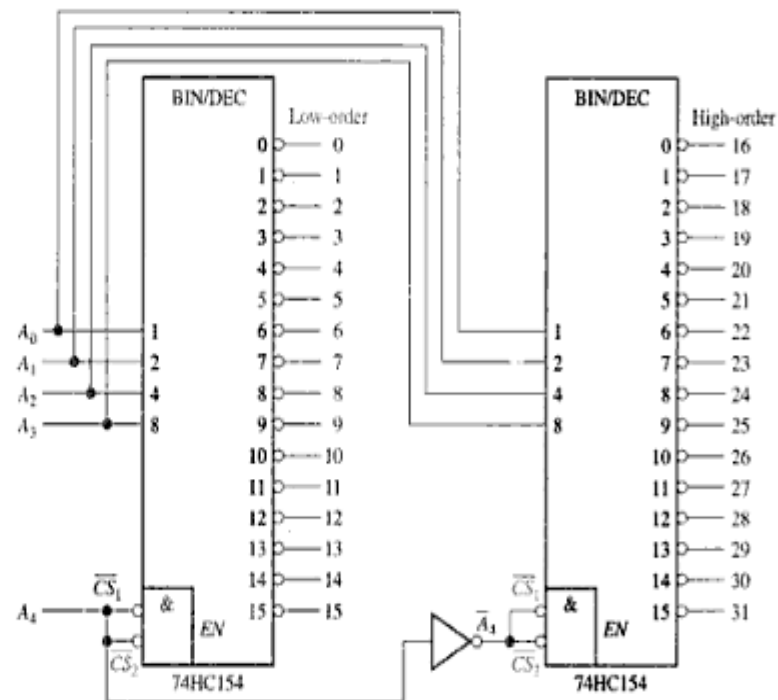
Truth Table:

DECIMAL DIGIT	BINARY INPUTS				DECODING FUNCTION	OUTPUTS															
	A ₃	A ₂	A ₁	A ₀		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	$\overline{A_3}\overline{A_2}\overline{A_1}\overline{A_0}$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	$\overline{A_3}\overline{A_2}\overline{A_1}A_0$	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	0	1	0	$\overline{A_3}\overline{A_2}A_1\overline{A_0}$	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	0	0	1	1	$\overline{A_3}\overline{A_2}A_1A_0$	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4	0	1	0	0	$\overline{A_3}A_2\overline{A_1}\overline{A_0}$	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
5	0	1	0	1	$\overline{A_3}A_2\overline{A_1}A_0$	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
6	0	1	1	0	$\overline{A_3}A_2A_1\overline{A_0}$	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
7	0	1	1	1	$\overline{A_3}A_2A_1A_0$	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1	0	0	0	$A_3\overline{A_2}\overline{A_1}\overline{A_0}$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
9	1	0	0	1	$A_3\overline{A_2}\overline{A_1}A_0$	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
10	1	0	1	0	$A_3\overline{A_2}A_1\overline{A_0}$	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
11	1	0	1	1	$A_3\overline{A_2}A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
12	1	1	0	0	$A_3A_2\overline{A_1}\overline{A_0}$	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
13	1	1	0	1	$A_3A_2\overline{A_1}A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
14	1	1	1	0	$A_3A_2A_1\overline{A_0}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
15	1	1	1	1	$A_3A_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

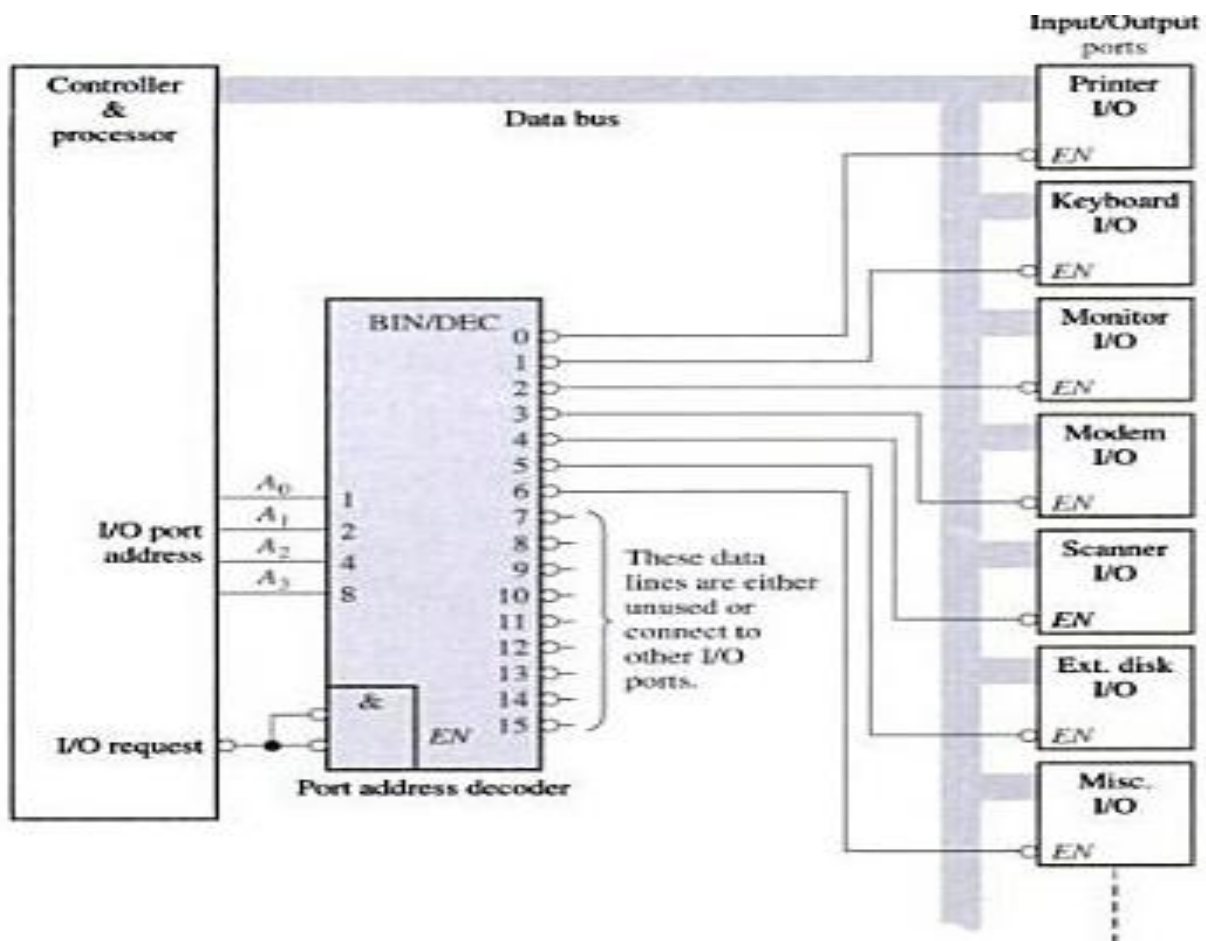
Cascading Decoders-cascading 5-bit number:

Since the 74HC154 can handle only four bits, two decoders must be used to decode five bits. The fifth bit, A_4 , is connected to the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, of one decoder, and $\overline{A}_4$ is connected to the $\overline{CS}_1$ and $\overline{CS}_2$ inputs of the other decoder, as shown in Figure 6-33. When the decimal number is 15 or less, $A_4 = 0$, and the low-order decoder is enabled and the high-order decoder is disabled. When the decimal number is greater than 15, $A_4 = 1$ so $\overline{A}_4 = 0$, and the high-order decoder is enabled and the low-order decoder is disabled.

► FIGURE 6-33



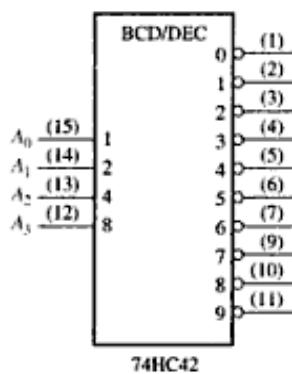
Application-In computers for Input/Output selection:



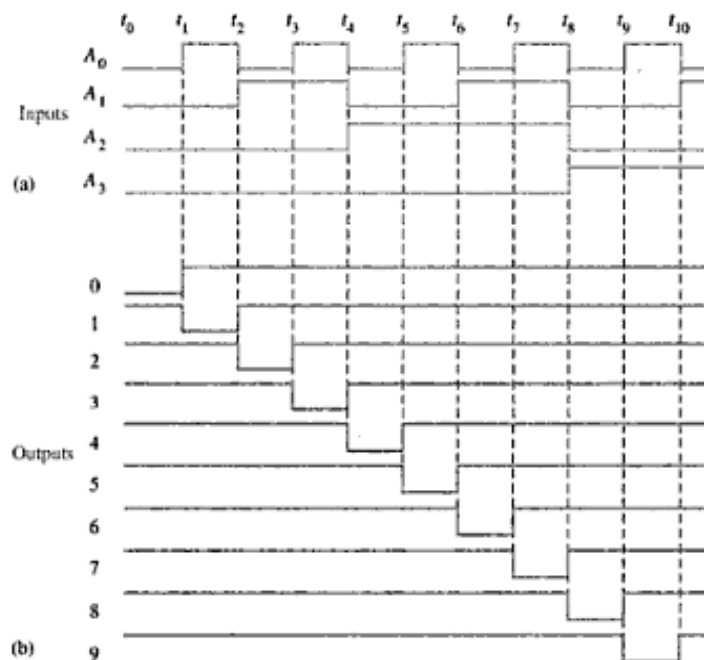
BCD to Decimal Decoder

The BCD-to-decimal decoder converts each BCD code (8421 code) into one of ten possible decimal digit indications. It is frequently referred as a *4-line-to-10-line decoder* or a *1-of-10 decoder*.

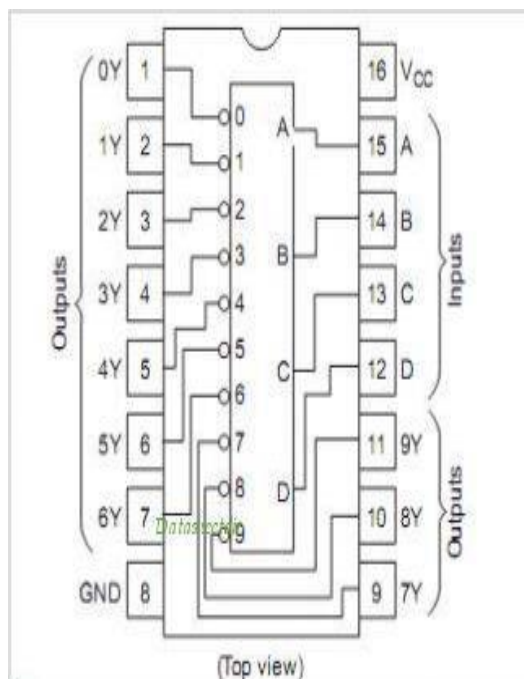
The 74HC42 is an integrated circuit BCD-to-decimal decoder. The logic symbol is shown in Figure 6-35. If the input waveforms in Figure 6-36(a) are applied to the inputs of the 74HC42, show the output waveforms.



▲ FIGURE 6-35



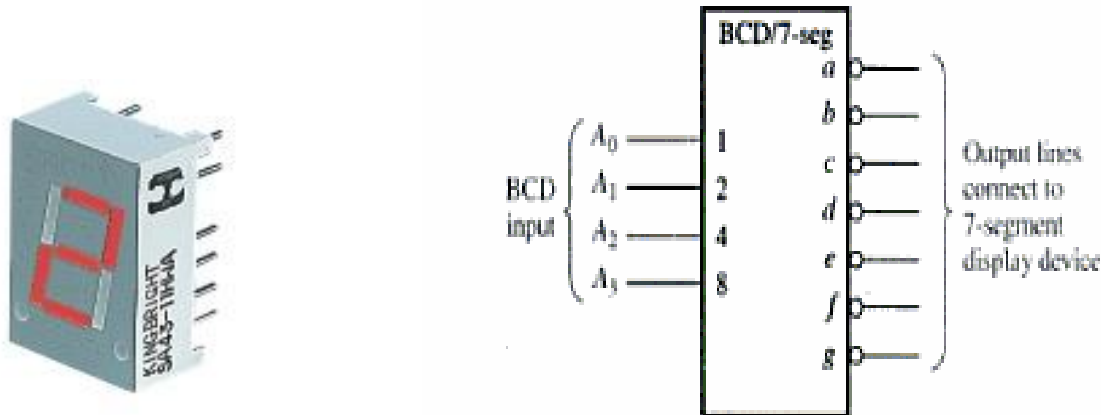
▲ FIGURE 6-36



DECIMAL DIGIT	BCD CODE				DECODING FUNCTION
	A_3	A_2	A_1	A_0	
0	0	0	0	0	$\bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0$
1	0	0	0	1	$\bar{A}_3\bar{A}_2\bar{A}_1A_0$
2	0	0	1	0	$\bar{A}_3\bar{A}_2A_1\bar{A}_0$
3	0	0	1	1	$\bar{A}_3\bar{A}_2A_1A_0$
4	0	1	0	0	$\bar{A}_3A_2\bar{A}_1\bar{A}_0$
5	0	1	0	1	$\bar{A}_3A_2\bar{A}_1A_0$
6	0	1	1	0	$\bar{A}_3A_2A_1\bar{A}_0$
7	0	1	1	1	$\bar{A}_3A_2A_1A_0$
8	1	0	0	0	$A_3\bar{A}_2\bar{A}_1\bar{A}_0$
9	1	0	0	1	$A_3\bar{A}_2\bar{A}_1A_0$

BCD-to-7 segment Decoder (IC 7447)

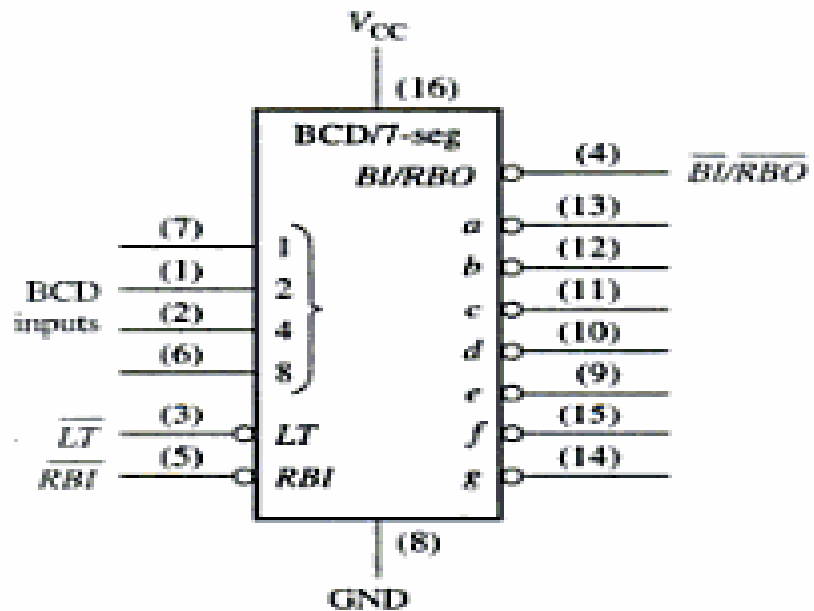
BCD-to-7-segment decoder accepts the BCD code on its inputs and provides outputs to drive 7-segment display devices to produce a decimal readout. The logic diagram for a basic 7-segment decoder is shown in Figure 6-37.



The 74LS47 is an example of an IC device that decodes a BCD input and drives a 7-segment display. In addition to its decoding and segment drive capability, the 74LS47 has several additional features as indicated by the $\overline{LT}$, $\overline{RBI}$, $\overline{BI}/\overline{RBO}$ functions in the logic symbol of Figure 6-38. As indicated by the bubbles on the logic symbol, all of the outputs (a through g) are active-LOW as are the $\overline{LT}$ (lamp test), $\overline{RBI}$ (ripple blanking input), and $\overline{BI}/\overline{RBO}$ (blanking input/ripple blanking output) functions. The outputs can drive a common-anode 7-segment display directly.



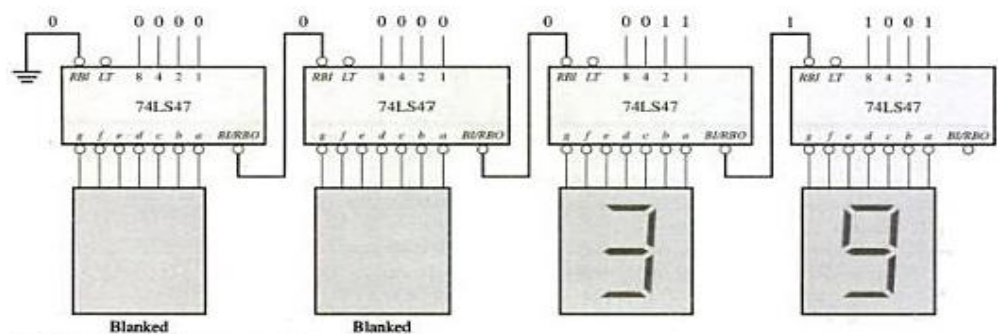
Logic diagram



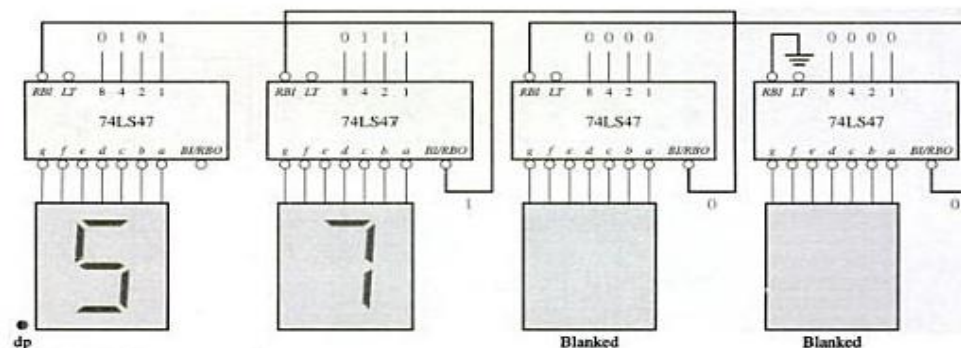
In addition to decoding a BCD input and producing the appropriate 7-segment outputs, the 74LS47 has lamp test and zero suppression capability.

Lamp Test When a LOW is applied to the $\overline{LT}$ input and the $\overline{BI}/\overline{RBO}$ is HIGH, all of the 7 segments in the display are turned on. Lamp test is used to verify that no segments are burned out.

Zero Suppression Zero suppression is a feature used for multidigit displays to blank out unnecessary zeros. For example, in a 6-digit display the number 6.4 may be displayed as 006.400 if the zeros are not blanked out. Blanking the zeros at the front of a number is called *leading zero suppression* and blanking the zeros at the back of the number is called *trailing zero suppression*.



(a) Illustration of leading zero suppression



(b) Illustration of trailing zero suppression

The logic diagram in Figure 6-39(a) illustrates leading zero suppression for a whole number. The highest-order digit position (left-most) is always blanked if a zero code is on its BCD inputs because the $\overline{RBI}$ of the most-significant decoder is made LOW by connecting it to ground. The $\overline{RBO}$ of each decoder is connected to the $\overline{RBI}$ of the next lowest-order decoder so that all zeros to the left of the first nonzero digit are blanked. For example, in part (a) of the figure the two highest-order digits are zeros and therefore are blanked. The remaining two digits, 3 and 9 are displayed.

The logic diagram in Figure 6-39(b) illustrates trailing zero suppression for a fractional number. The lowest-order digit (right-most) is always blanked if a zero code is on its BCD inputs because the $\overline{RBI}$ is connected to ground. The $\overline{RBO}$ of each decoder is connected to the $\overline{RBI}$ of the next highest-order decoder so that all zeros to the right of the first nonzero digit are blanked. In part (b) of the figure, the two lowest-order digits are zeros and therefore are blanked. The remaining two digits, 5 and 7 are displayed. To combine both leading and trailing zero suppression in one display and to have decimal point capability, additional logic is required.

Implement the 4-to-16 decoder using two 3*8 Decoder

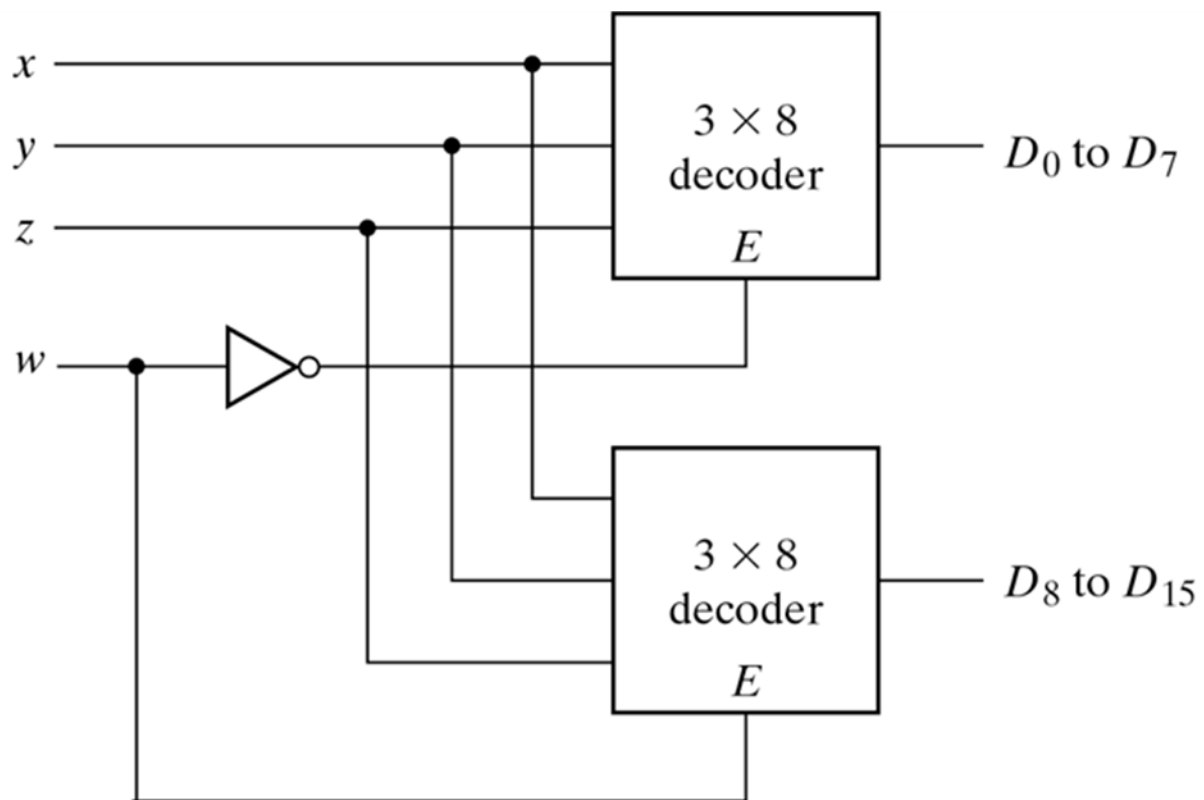
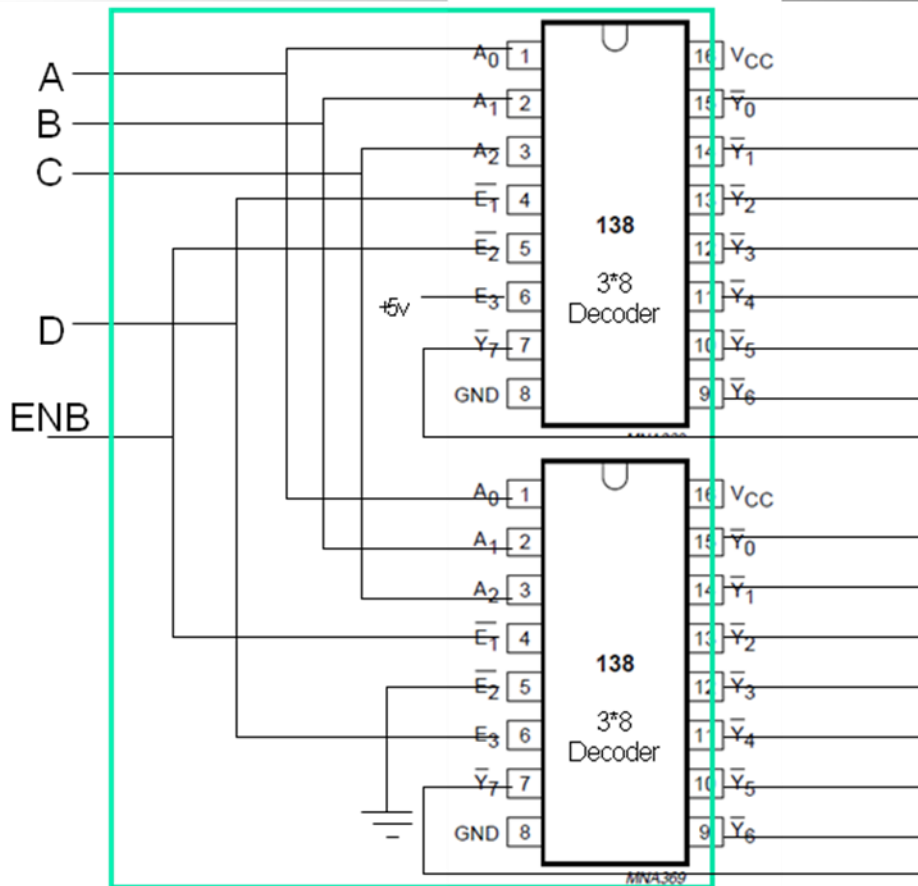
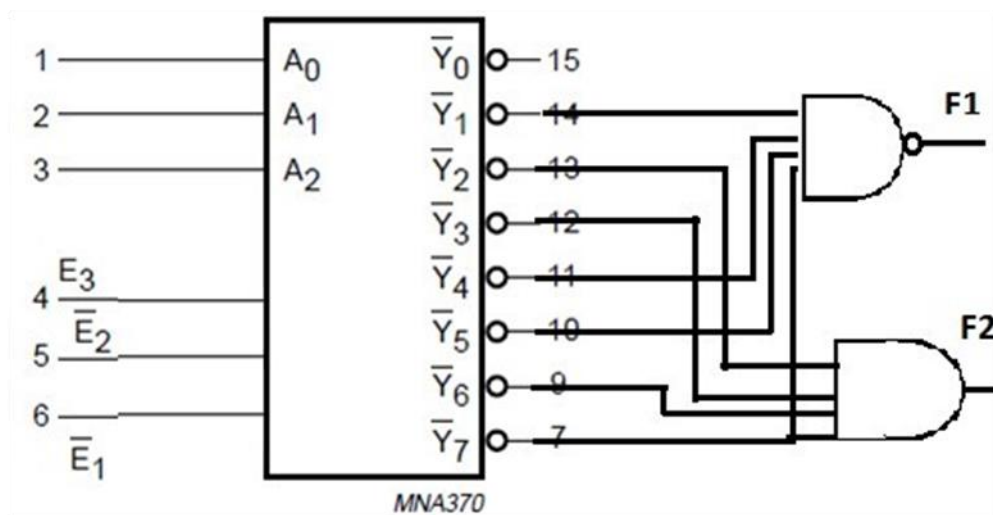


Fig. 4-20 4×16 Decoder Constructed with Two 3×8 Decoders



Implement the following multiple output function using 74LS138 and external gates. $F_1(A,B,C) = \sum m(1,4,5,7)$ & $F_2(A,B,C) = \prod m(2,3,6,7)$ 74LS138 is a 3*8 decoder. The outputs of this ic have active Low. i.e in SOP form for F_1 using NAND gate and POS function for F_2 using AND gate.



Implementation of a Full Adder with a Decoder

From table 4-4, we obtain the functions for the combinational circuit in sum of minterms:

$$S(x, y, z) = \sum(1, 2, 4, 7)$$

$$C(x, y, z) = \sum(3, 5, 6, 7)$$

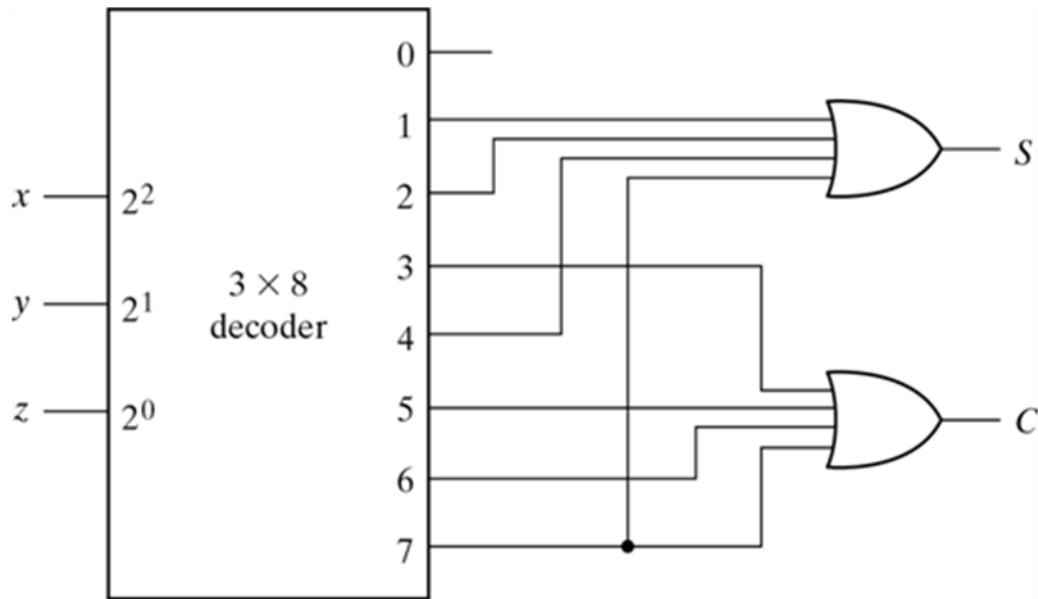


Fig. 4-21 Implementation of a Full Adder with a Decoder

Design 5*32 decoder using one 2*4 Decoder and four 3*8 Decoder

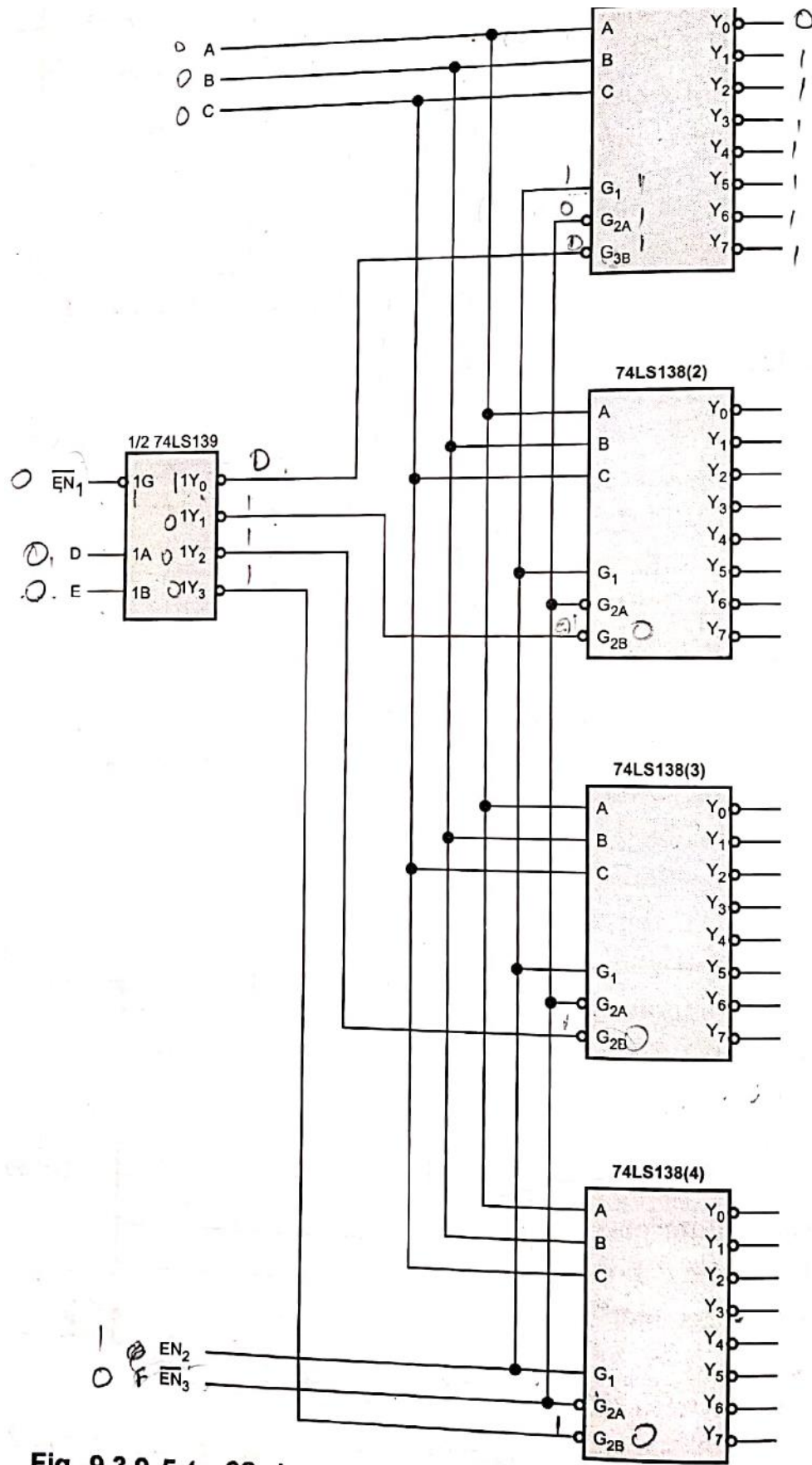
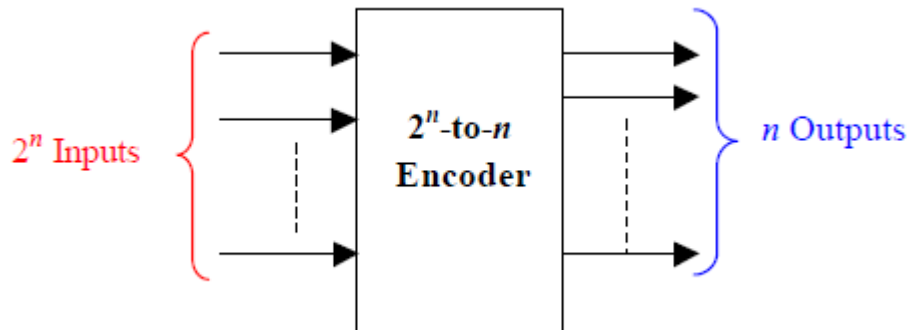


Fig. 9.3.9 5 to 32 decoder using 74LS138 and 74LS139

ENCODER

An encoder has – 2^n inputs – n outputs

- ✓ Outputs the binary value of the selected (or active) input.
- ✓ Performs the inverse operation of a decoder.
- ✓ Issues – What if more than one input is active? – What if no inputs are active?

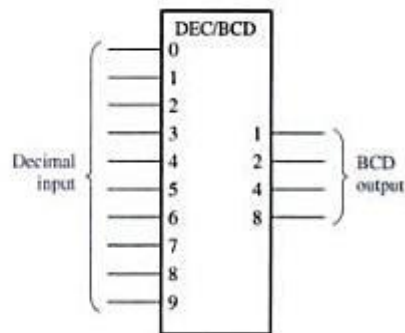


The Decimal-to-BCD Encoder

This type of encoder has ten inputs—one for each decimal digit—and four outputs corresponding to the BCD code, as shown in Figure 6–40. This is a basic 10-line-to-4-line encoder.

► **FIGURE 6–40**

Logic symbol for a decimal-to-BCD encoder.



Truth table for Decimal to BCD encoder:

DECIMAL DIGIT	BCD CODE			
	A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

$$A_3 = 8 + 9$$

Bit A_2 is always a 1 for decimal digit 4, 5, 6 or 7 can be expressed as an OR function as follows:

$$A_2 = 4 + 5 + 6 + 7$$

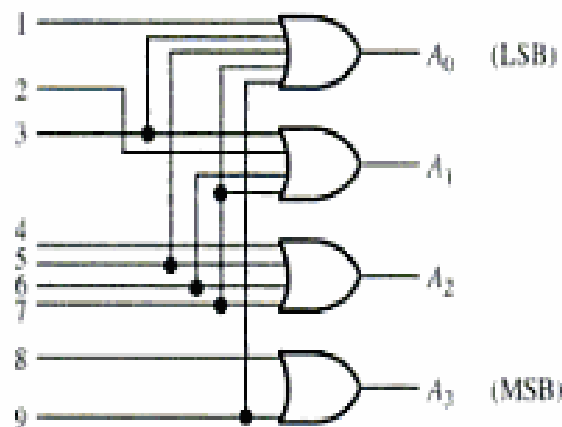
Bit A_1 is always a 1 for decimal digit 2, 3, 6, or 7 and can be expressed as

$$A_1 = 2 + 3 + 6 + 7$$

Finally, A_0 is always a 1 for decimal digit 1, 3, 5, 7, or 9. The expression for A_0 is

$$A_0 = 1 + 3 + 5 + 7 + 9$$

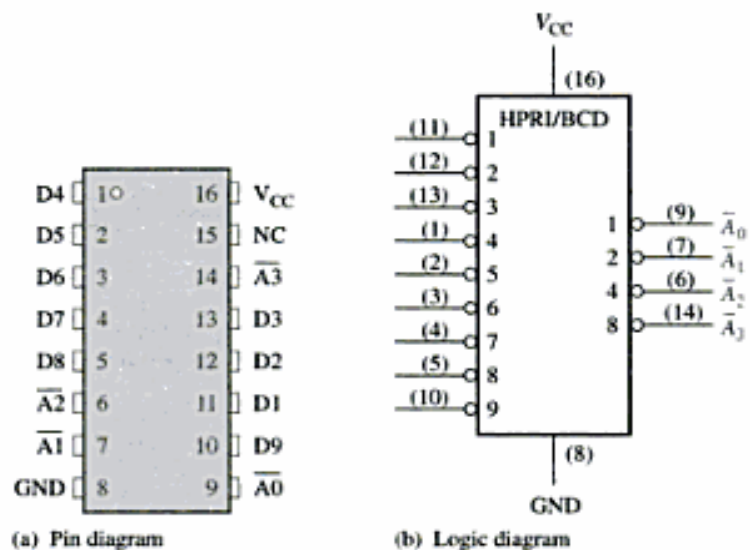
Gate level diagram of Decimal to BCD encoder:



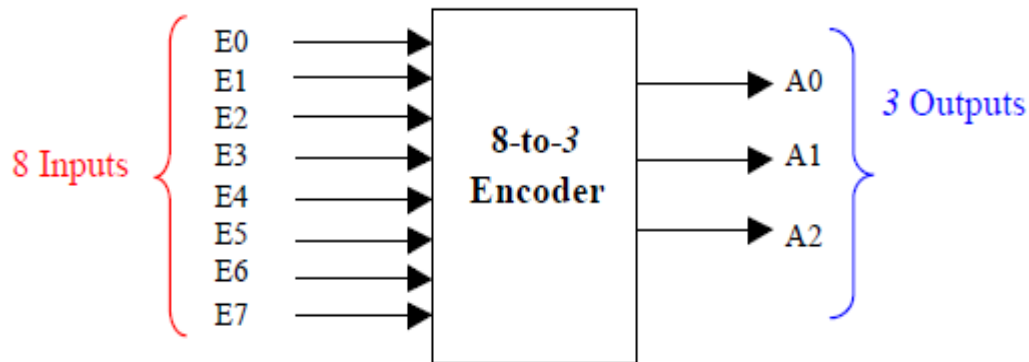
A Decimal-to-BCD Encoder

The 74HC147 is a **priority encoder** with active-LOW inputs (0) for decimal digits 1 through 9 and active-LOW BCD outputs as indicated in the logic symbol in Figure 6-42. A BCD zero output is represented when none of the inputs is active. The device pin numbers are in parentheses.

► **FIGURE 6-42**



Octal-to-binary encoder



We will use 8-to-3 encoder (Figure 11) for this problem, since we have eight inputs, one for each of the octal digits, and three outputs that generate the corresponding binary number. Thus, in the truth table, we see eight input variables on the left side of the vertical lines, and three variables on the right side of the vertical line (table 7).

Inputs								Outputs			Decimal Code
E7	E6	E5	E4	E3	E2	E1	E0	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0	0	
0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	1	0	0	0	1	1
0	0	0	0	0	1	0	0	0	1	0	2
0	0	0	0	1	0	0	0	0	1	1	3
0	0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	0	0	0	0	1	0	1	5
0	1	0	0	0	0	0	0	1	1	0	6
1	0	0	0	0	0	0	0	1	1	1	7

Table 7: Truth table of Octal-to-binary encoder

Note that not all input combinations are valid.

Valid combinations are those which have exactly one input equal to logic 1 while all other inputs are logic 0's.

Since, the number of inputs = 8, K-maps cannot be used to derive the output Boolean expressions.

The encoder implementation, however, can be directly derived from the truth table

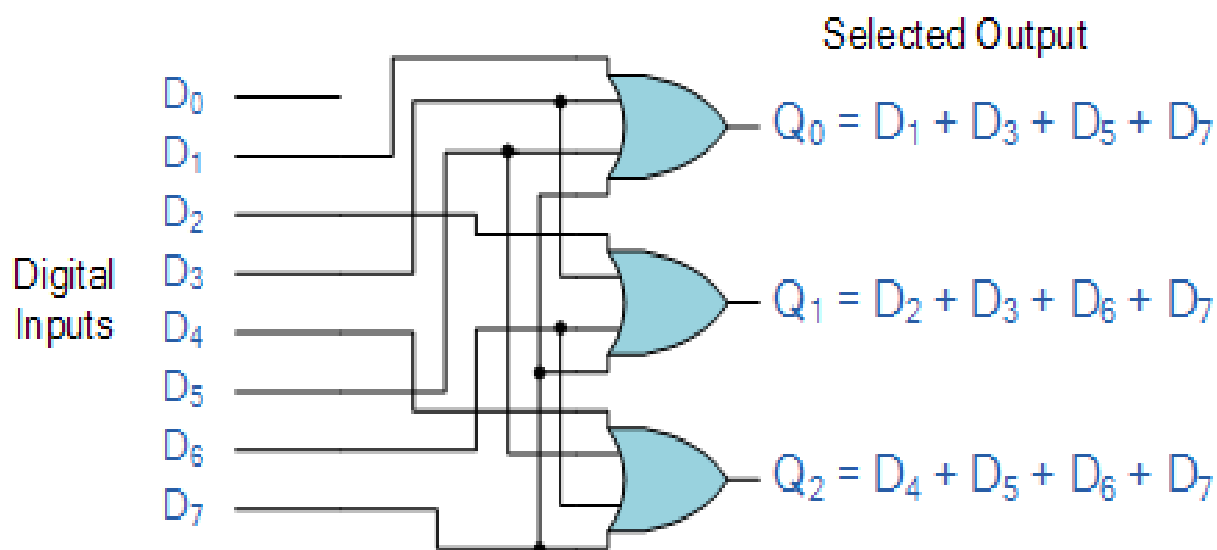
- Since $A_0 = 1$ if the input octal digit is 1 or 3 or 5 or 7, then we can write:

$$A_0 = E_1 + E_3 + E_5 + E_7$$

- Likewise, $A_1 = E_2 + E_3 + E_6 + E_7$, and similarly

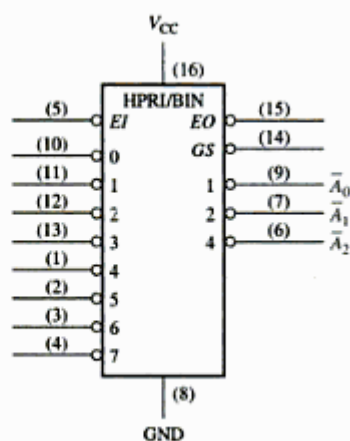
- $A_2 = E_4 + E_5 + E_6 + E_7$

Thus, the encoder can be implemented using three 4-input OR gates.



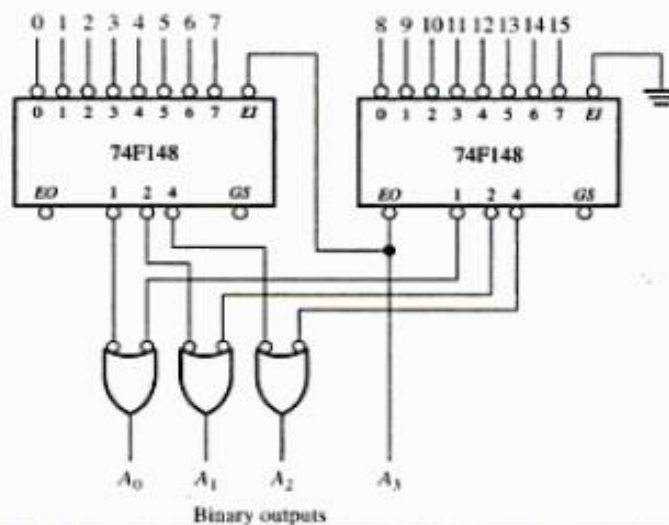
IC74F48-OCTAL TO BINARY ENCODER:

► FIGURE 6-43



The 74F148 can be expanded to a 16-line-to-4-line encoder by connecting the *EO* of the higher-order encoder to the *EI* of the lower-order encoder and negative-ORing the corresponding binary outputs as shown in Figure 6-44. The *EO* is used as the fourth and most-significant bit. This particular configuration produces active-HIGH outputs for the 4-bit binary number.

► FIGURE 6-44



Major Limitation of Encoders

- Exactly one input must be active at any given time.
- If the number of active inputs is less than one or more than one, the output will be incorrect.
- For example, if $E_3 = E_6 = 1$, the output of the encoder $A_2A_1A_0 = 111$, which implies incorrect output.

Two Problems to Resolve.

1. If two or more inputs are active at the same time, *what should the output be?*
2. An output of all 0's is generated in 2 cases:
 - when all inputs are 0
 - when E_0 is equal to 1.

How can this ambiguity be resolved?

Solution To Problem 1:

- Use a *Priority Encoder* which produces the output corresponding to the input with higher priority.
- Inputs are assigned priorities according to their subscript value; e.g. higher subscript inputs are assigned higher priority.
- In the previous example, if $E_3 = E_6 = 1$, the output corresponding to E_6 will be produced ($A_2A_1A_0 = 110$) since E_6 has higher priority than E_3 .

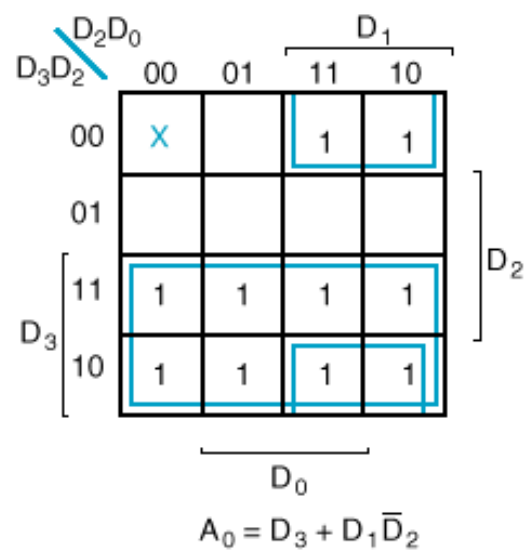
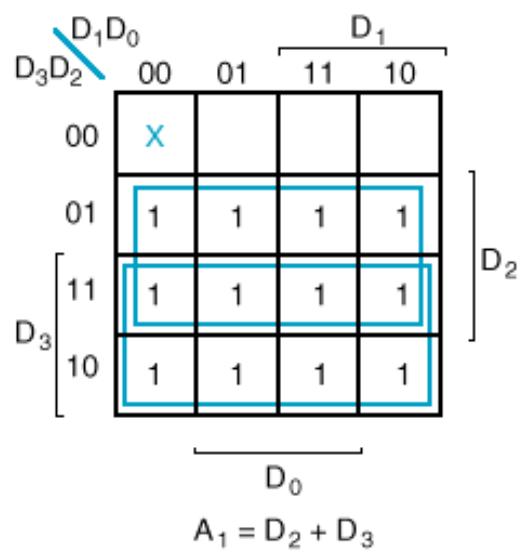
Solution To Problem 2:

- Provide one more output signal V to indicate *validity* of input data.
- $V = 0$ if none of the inputs equals 1, otherwise it is 1

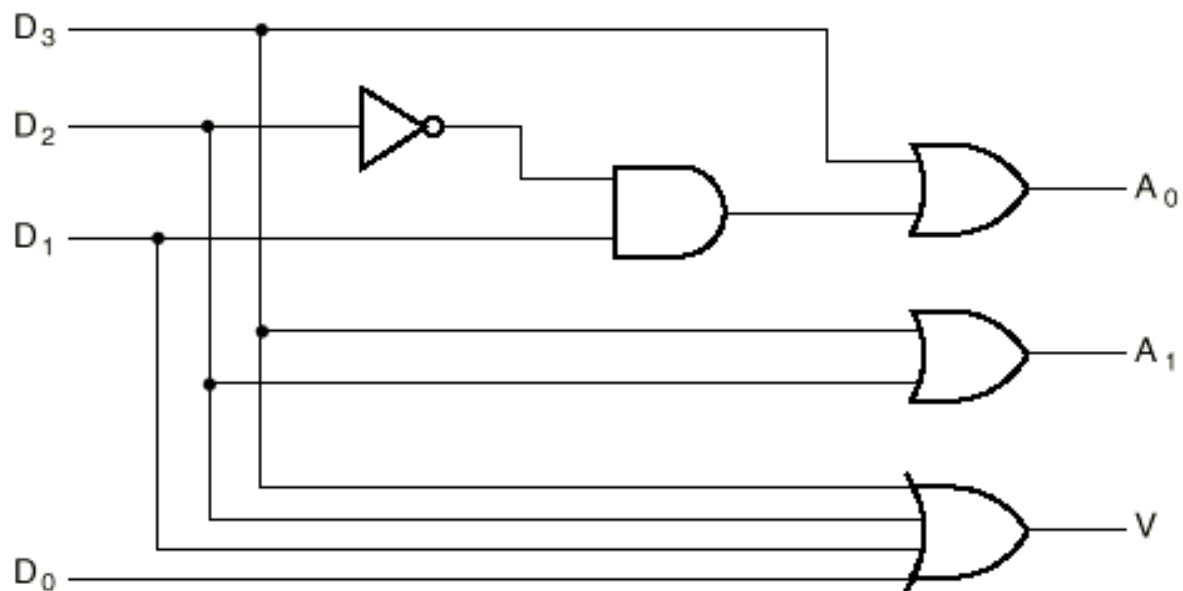
Priority Encoder:

- Solves the ambiguities mentioned above.
- Multiple asserted inputs are allowed; one has priority over all others.
- Separate indication of no asserted inputs.
- The operation of the priority encoder is such that:
- If two or more inputs are equal to 1 at the same time, the input in the highest-numbered position will take precedence.
- A **valid output indicator**, designated by V , is set to 1 only when one or more inputs are equal to 1. $V = D_3 + D_2 + D_1 + D_0$ by inspection.

Inputs				Outputs		
D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1



Logic Diagram:



Multiplexer

Multiplexer means many into one. A multiplexer is a circuit used to select and route any one of the several input signals to a signal output. An simple example of an non electronic circuit of a multiplexer is a single pole multiposition switch.

Multiposition switches are widely used in many electronics circuits. However circuits that operate at high speed require the multiplexer to be automatically selected. A mechanical switch cannot perform this task satisfactorily. Therefore, multiplexer used to perform high speed switching are constructed of electronic components.

Multiplexer handle two type of data that is analog and digital. For analog application, multiplexer are built of relays and transistor switches. For digital application, they are built from standard logic gates.

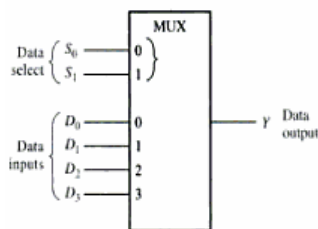
The multiplexer used for digital applications, also called digital multiplexer, is a circuit with many input but only one output. By applying control signals, we can steer any input to the output. Few types of multiplexer are 2-to-1, 4-to-1, 8-to-1, 16-to-1 multiplexer.

4-to-1 Multiplexer:

Multiplexer(IC 74151)

- “It is a device that allows digital information from several sources to one line”.

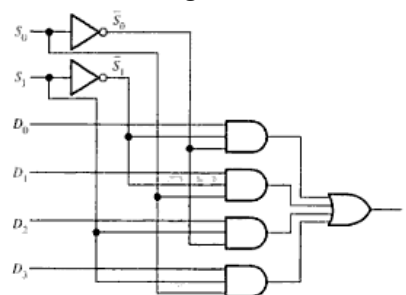
Logic Diagram



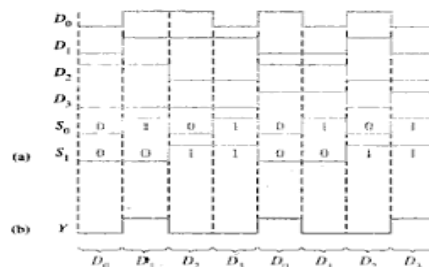
Truth table

DATA-SELECT INPUTS		INPUT SELECTED
S_1	S_0	
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Gate level Diagram



Waveforms



The data output is equal to D_0 only if $S_1 = 0$ and $S_0 = 0$: $Y = D_0 \bar{S}_1 \bar{S}_0$.

The data output is equal to D_1 only if $S_1 = 0$ and $S_0 = 1$: $Y = D_1 \bar{S}_1 S_0$.

The data output is equal to D_2 only if $S_1 = 1$ and $S_0 = 0$: $Y = D_2 S_1 \bar{S}_0$.

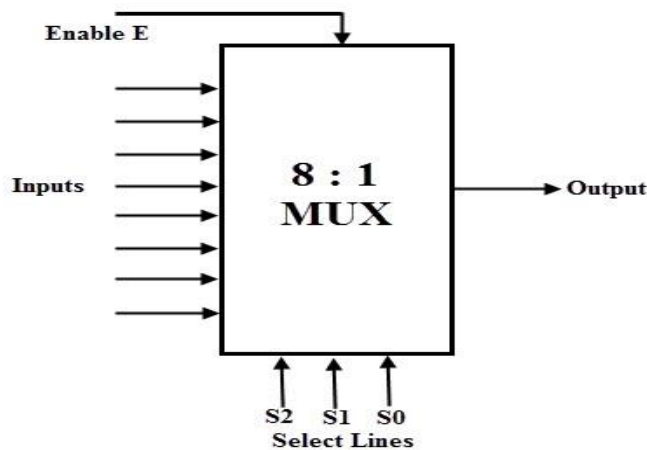
The data output is equal to D_3 only if $S_1 = 1$ and $S_0 = 1$: $Y = D_3 S_1 S_0$.

When these terms are ORed, the total expression for the data output is

$$Y = D_0 \bar{S}_1 \bar{S}_0 + D_1 \bar{S}_1 S_0 + D_2 S_1 \bar{S}_0 + D_3 S_1 S_0$$

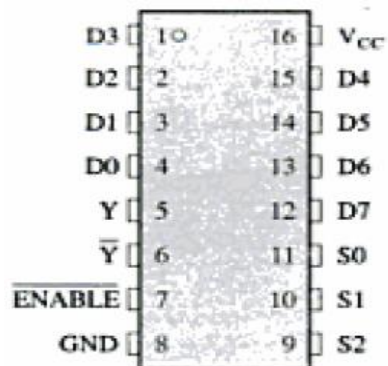
8 to 1 MUX-74LS151:

An **8-to-1 multiplexer** consists of **eight** data inputs D_0 through D_7 , three input select lines S_2 through S_0 and a single output line Y . Depending on the select lines combinations, **multiplexer** decodes the inputs.

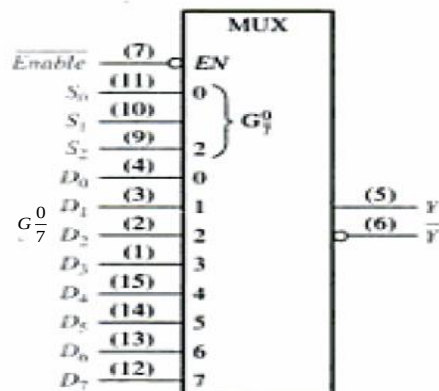


8 to 1 MUX-74LS151

Pin Diagram-74LS151



Logic Diagram

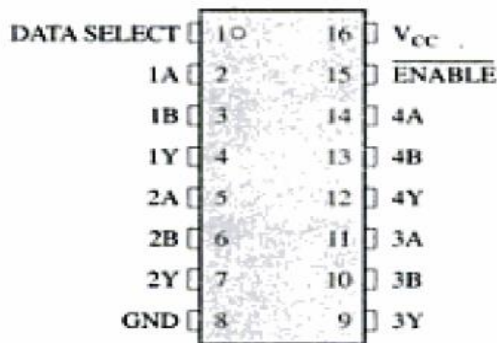


- $\overline{Enable}$ = LOW, allows the selected input data to pass through to the output.
- G_7^0 indicates AND relationship between data select inputs and each of the data inputs 0 through 7.

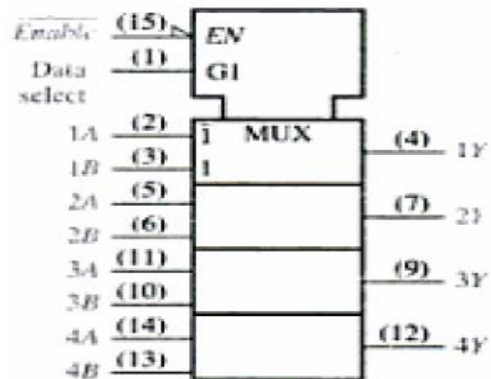
Quad 2-input Multiplexer-IC 74HC157

- It contains 4-separate 2-input multiplexers.
- All the multiplexers share common data select line and a common Enable.
- $\overline{Enable}$ =LOW, allows selected input data to pass through to the output.
- $\overline{Enable}$ =HIGH, prevents data from going through to the output (disables the multiplexer).

Pin Diagram



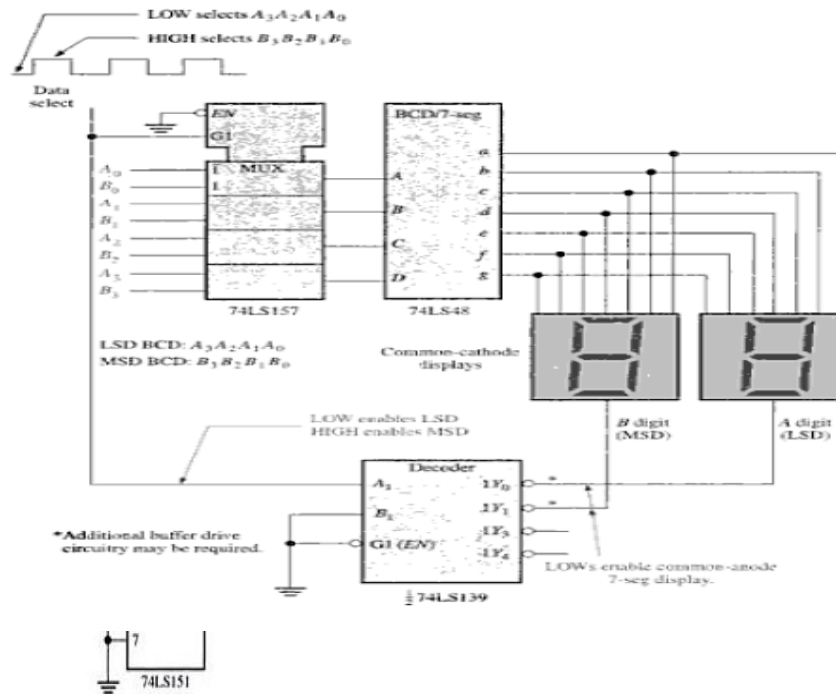
Logic Diagram



- G1=indicates AND relationship between data select input and data inputs.
- When data select=HIGH, B inputs of the multiplexer are selected.
- When data select=LOW, A inputs of the multiplexer are selected

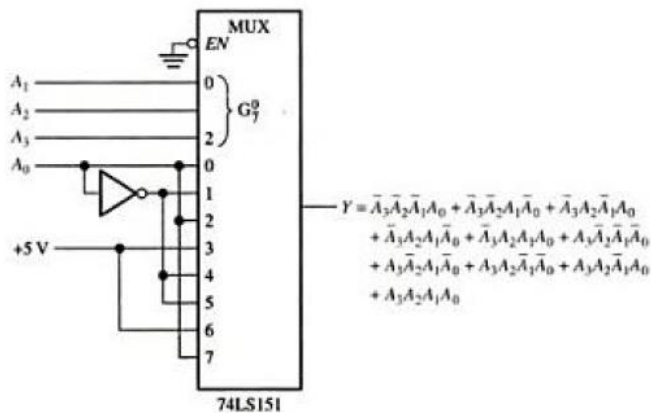
Applications

- 1) 7-segment display multiplexer



- b) Implement the logic function specified in truth table by using 74LS151 8-input data selector. Compare this method with a discrete logic gate implementation

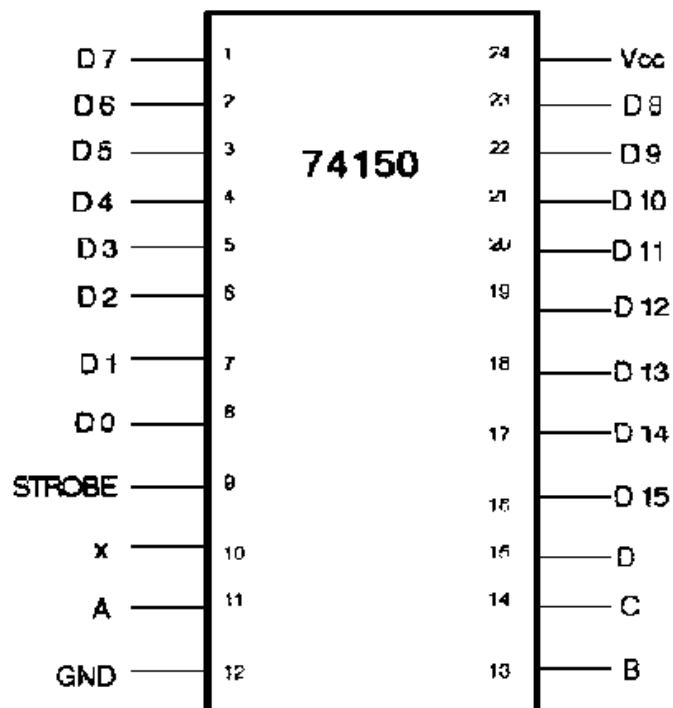
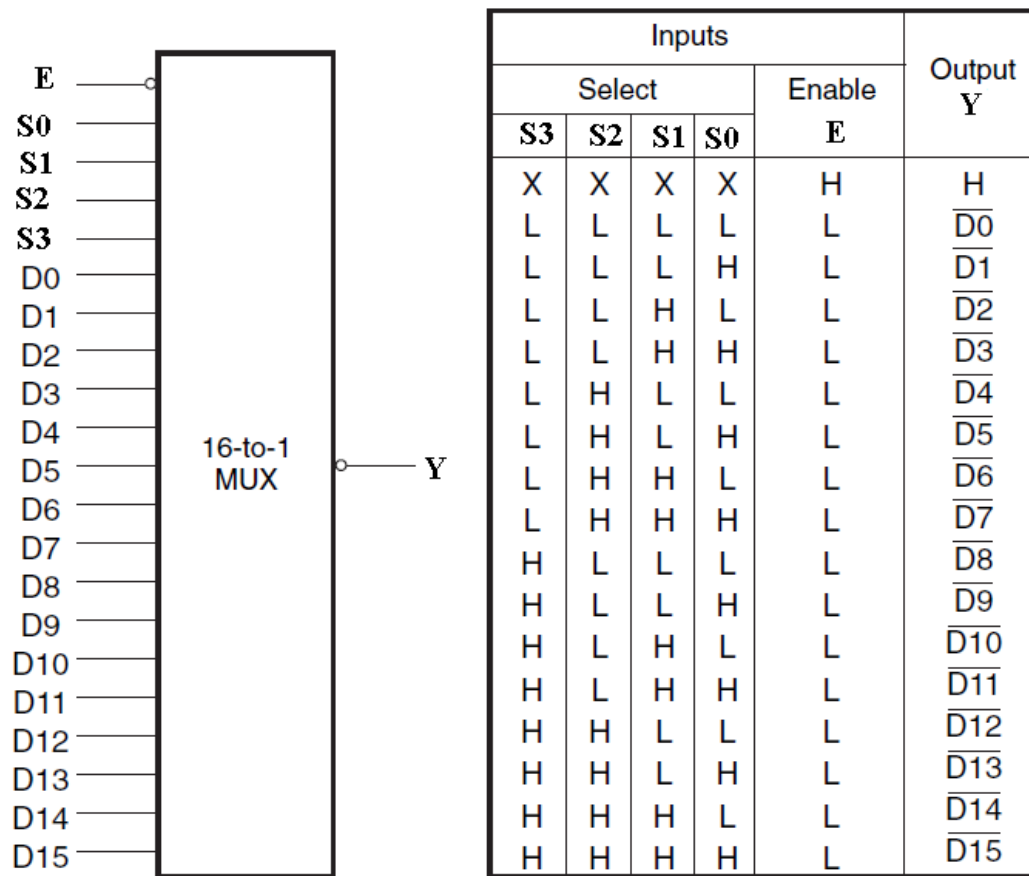
Sol:



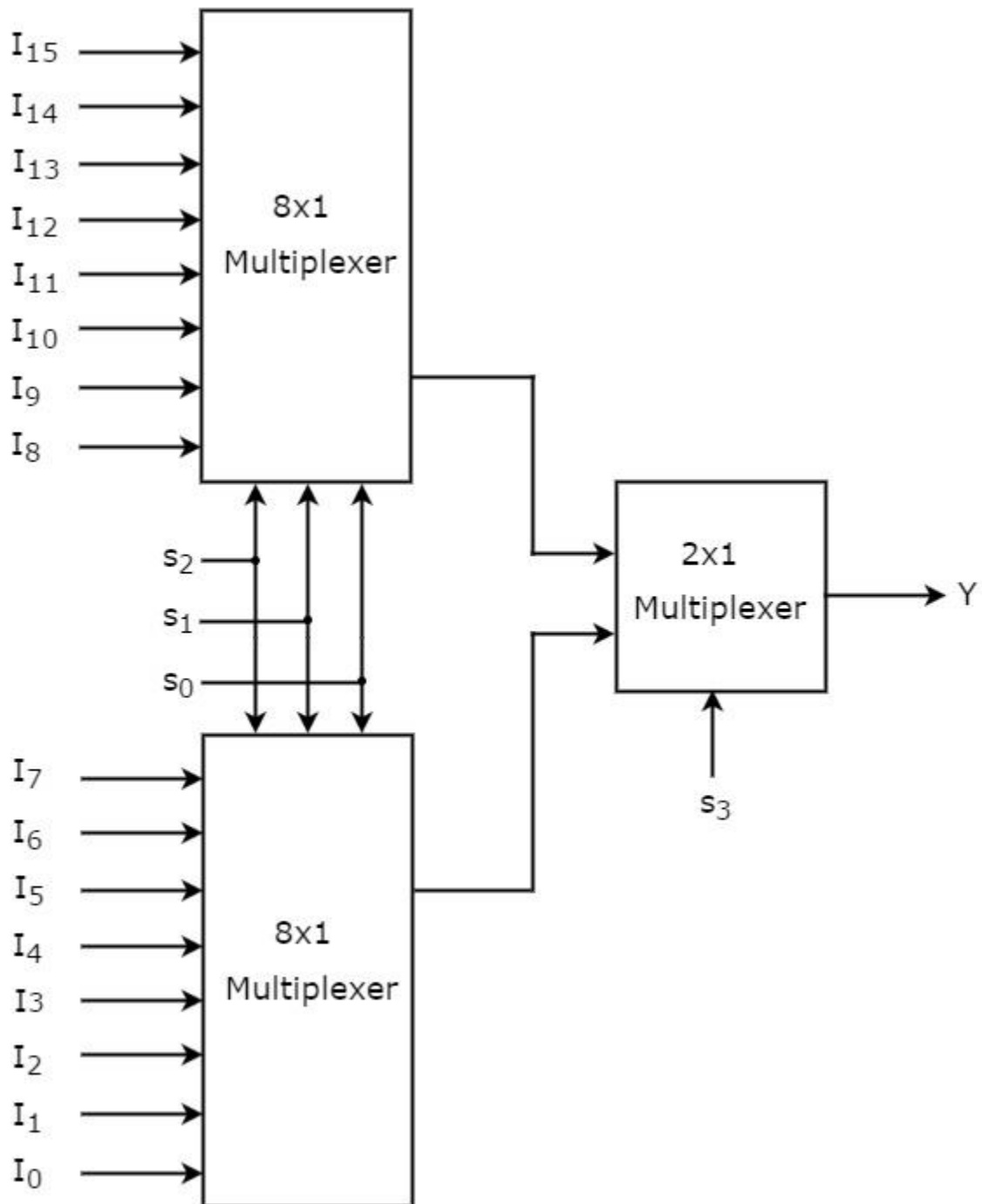
DECIMAL DIGIT	A ₂	A ₁	A ₀	OUTPUT Y
0	0	0	0	0
1	0	0	1	1
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1
8	1	0	0	1
9	1	0	1	0
10	1	1	0	1
11	1	1	1	0
12	1	1	0	1
13	1	1	1	1
14	1	1	1	0
15	1	1	1	1

16*1 MUX:

Figure below shows the 16-to-1 multiplexer Integrated circuit of TTL family 74150. This multiplexer has active LOW ENABLE input and active LOW output.



16*1 mux USING 8*1 mux



32-to-1 multiplexer using two 74xx150 ICs

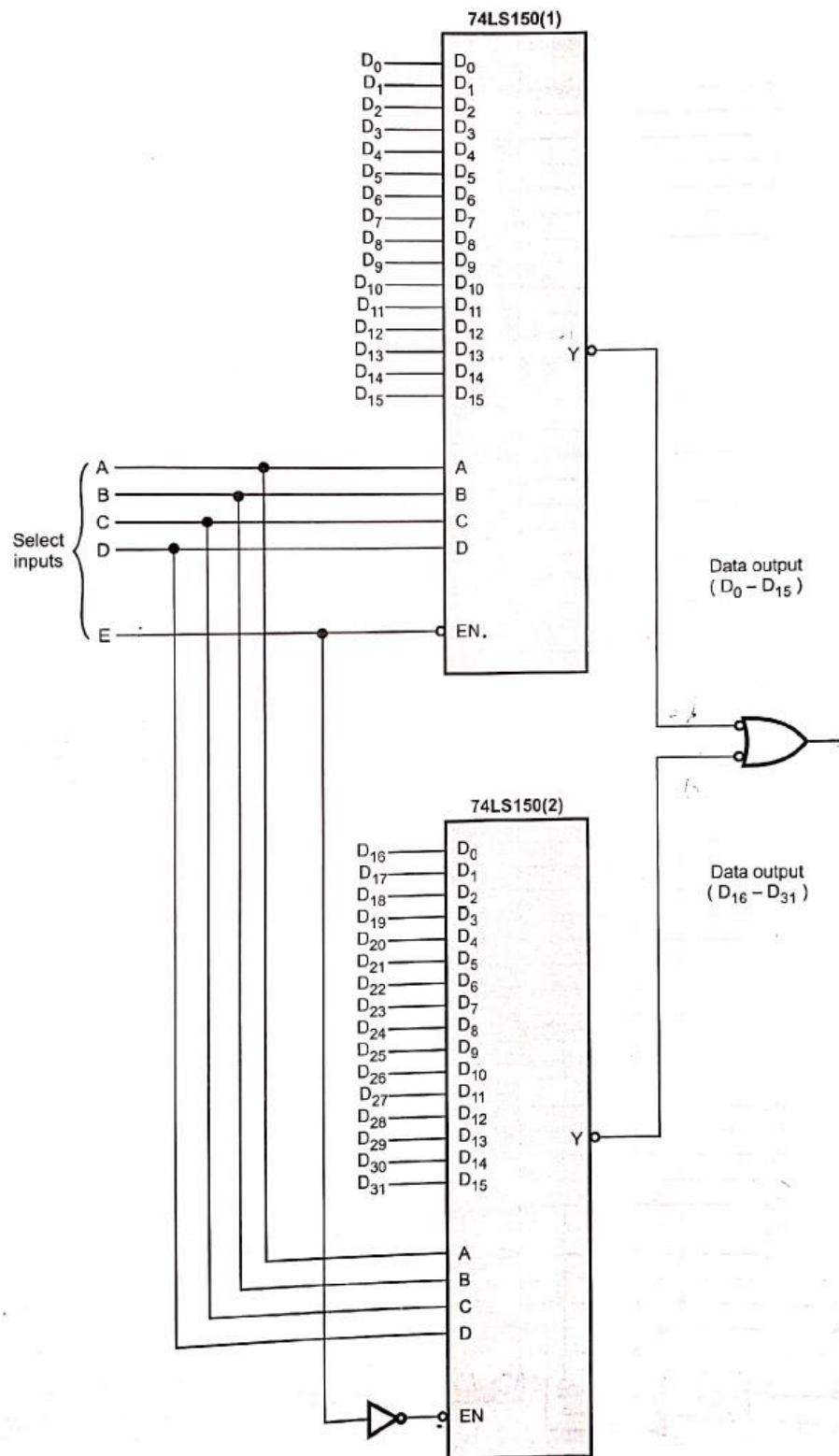
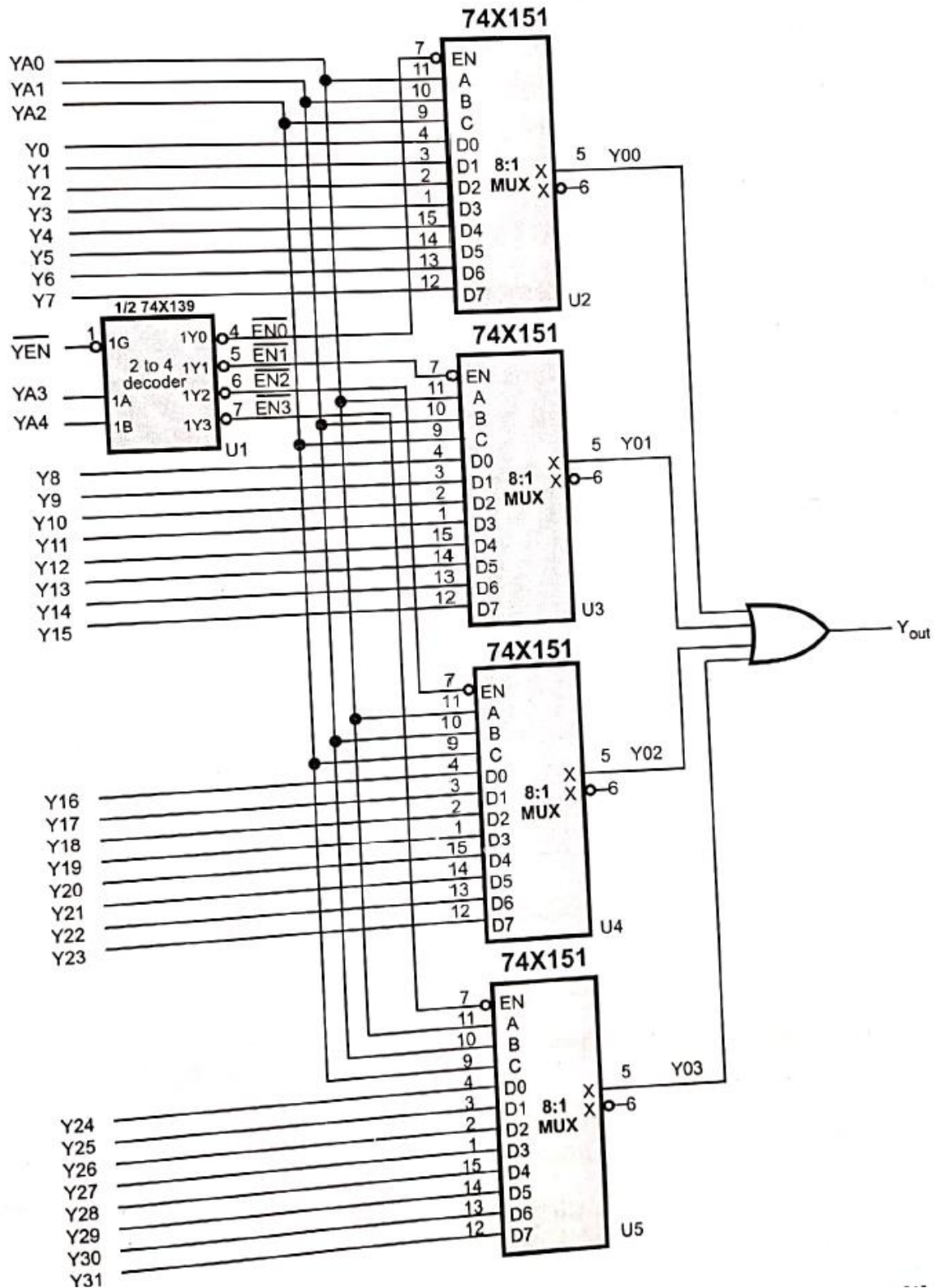
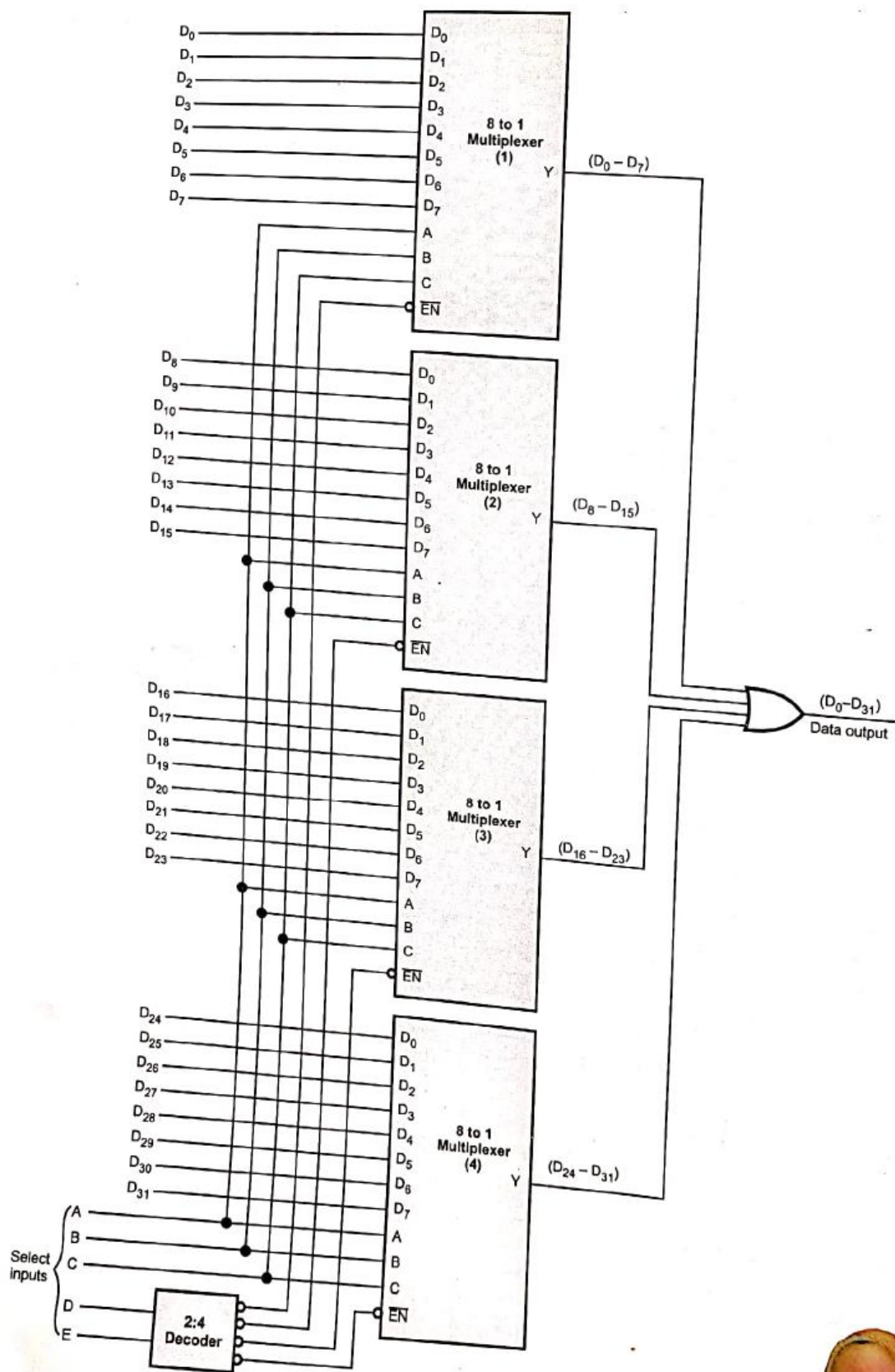


FIG. 5.7 32-to-1 multiplexer using two 74LS150 ICs

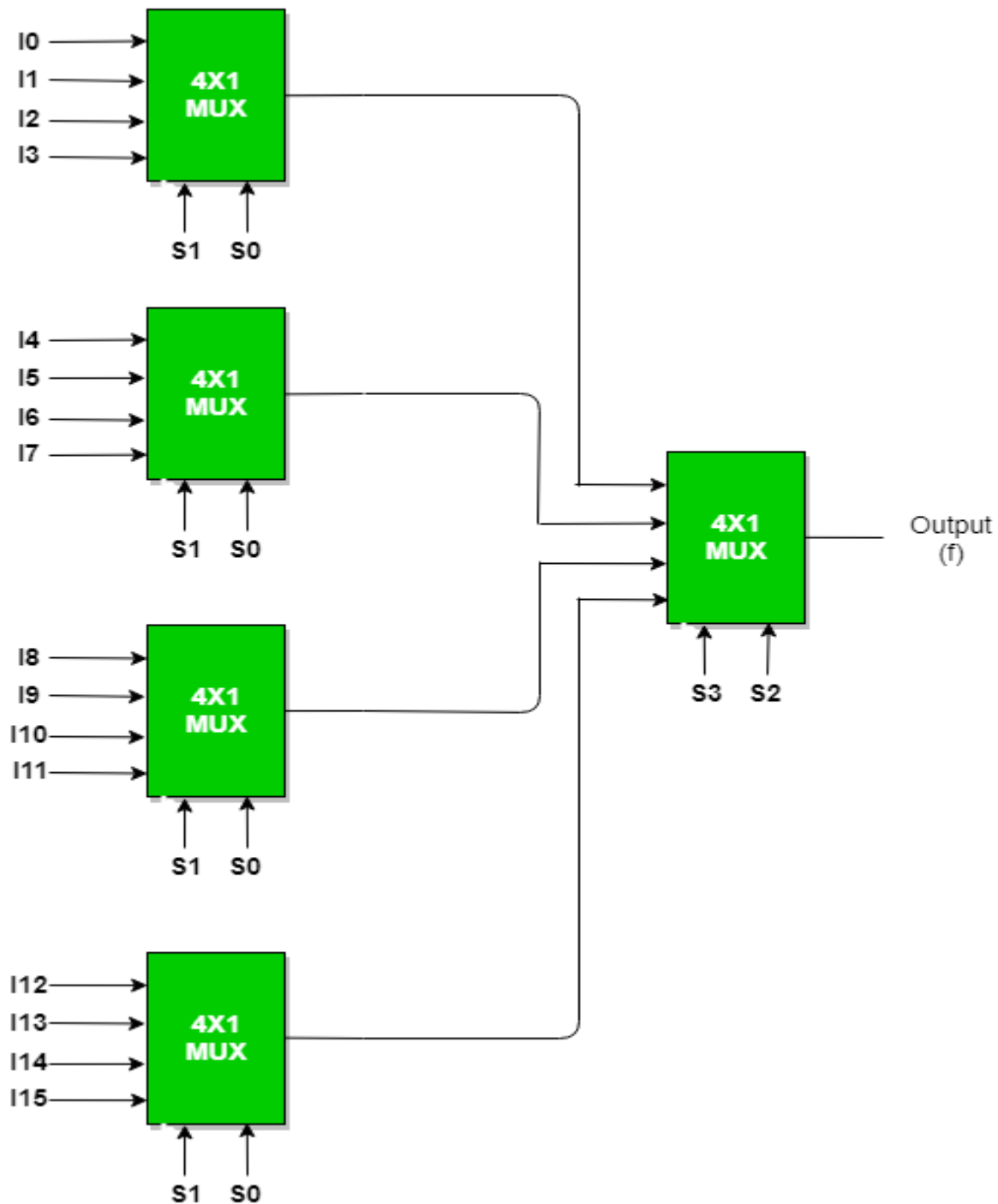
32-to-1 multiplexer using four 8-to-1 multiplexers(74X151) and a 2-to-4 decoder(74x139)





16 : 1 MUX using 4 : 1 MUX:

Inputs



Applications:

Multiplexer are used in various fields where multiple data need to be transmitted using a single line.

Following are some of the applications of multiplexers

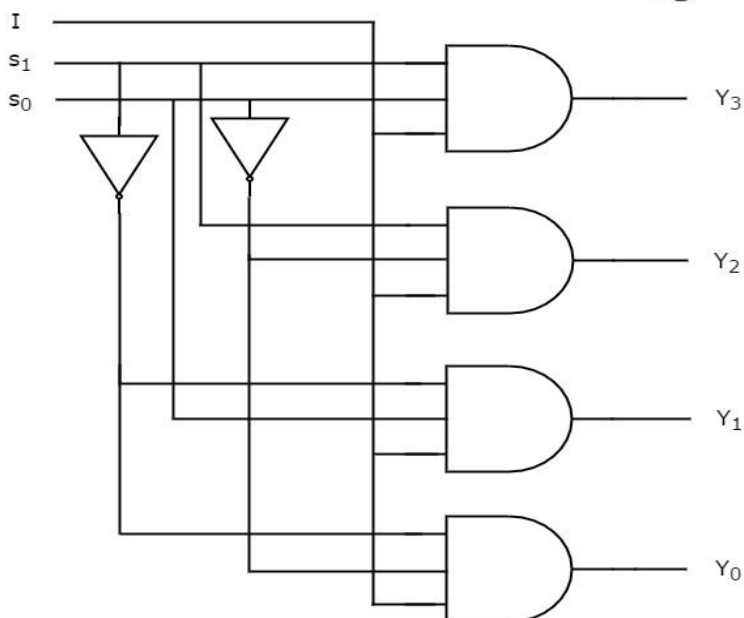
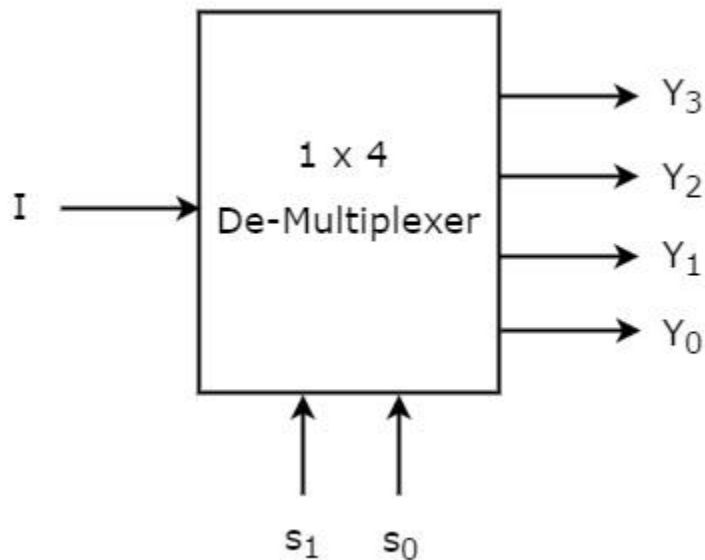
- Communication system,
- Telephone network,
- Computer memory ,
- Transmission from the computer system of a satellite

DEMULTIPLEXER

Demultiplexer means one to many. A demultiplexer is a circuit with one input and many output. By applying control signal, we can steer any input to the output. Few types of demultiplexer are 1-to-2, 1-to-4, 1-to-8 and 1-to-16 demultiplexer.

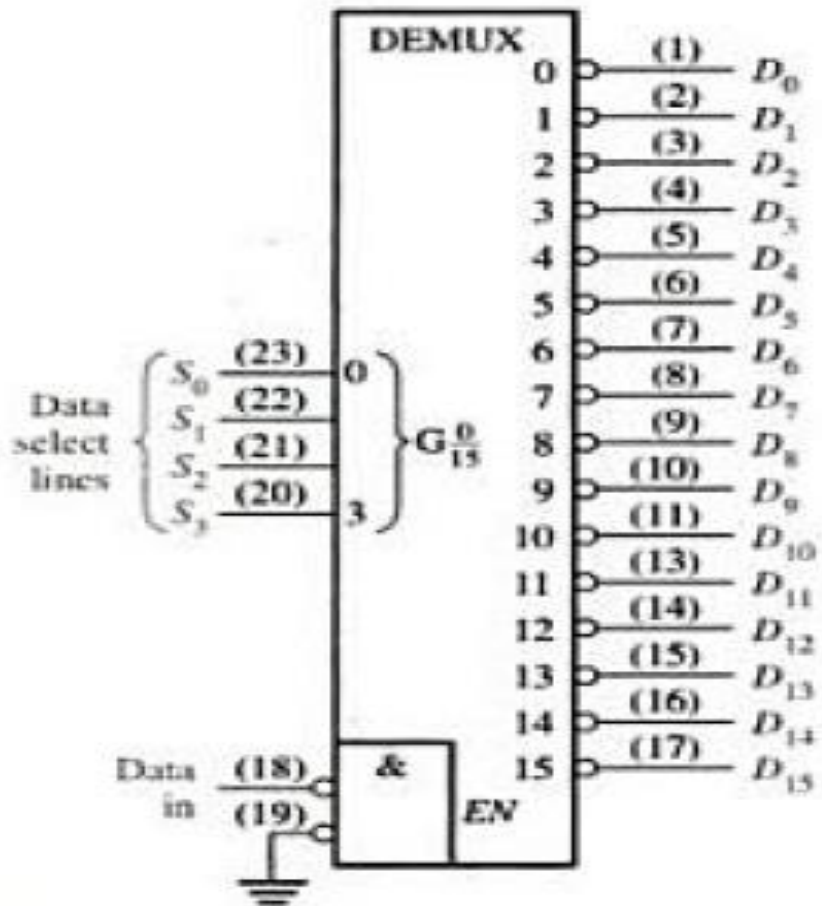
1- to-4 Demultiplexer:

1x4 De-Multiplexer has one input I , two selection lines, s_1 & s_0 and four outputs Y_3 , Y_2 , Y_1 & Y_0 . The **block diagram** of 1x4 De-Multiplexer is shown in the following figure.

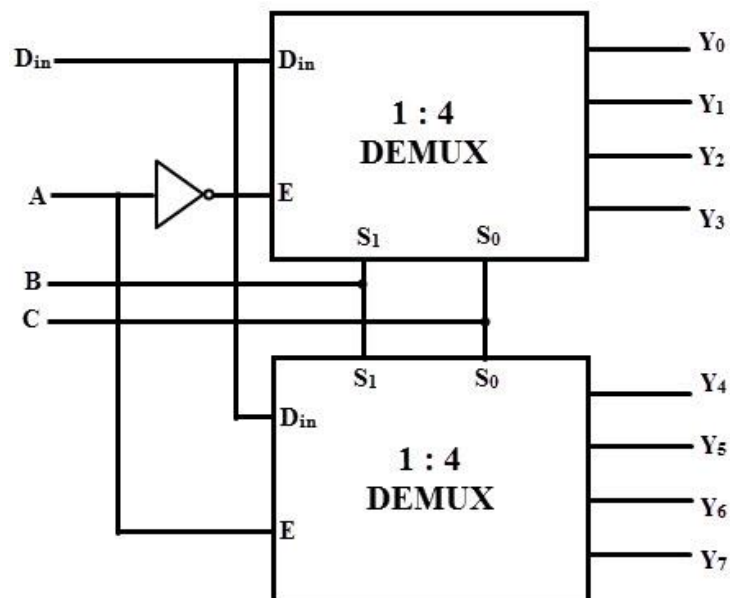


Data Input	Select Inputs		Outputs			
	s_1	s_0	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

1 to 16 line demultiplexer-74154:

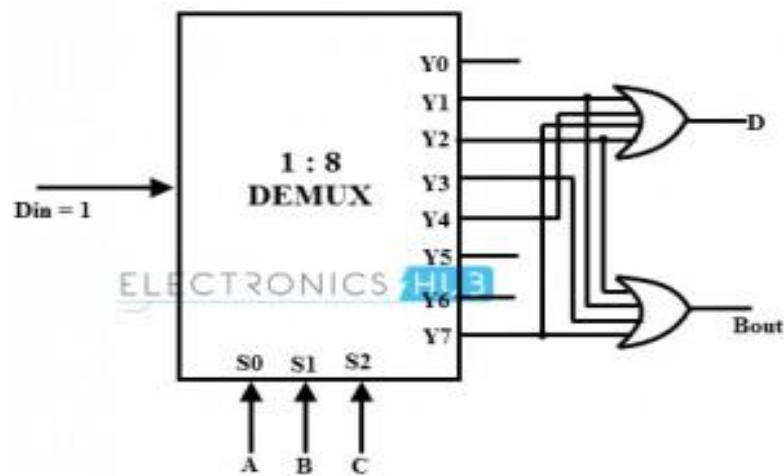


1-to-8 DEMUX using Two 1-to-4 Demultiplexers:



Implementation of Full Subtractor Using 1-to-8 DEMUX

A	B	B _{in}	D	B _{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Applications of DeMux:

De-multiplexer is used to connect a single source to multiple destinations. The main application area of de-multiplexer is communication system where multiplexer are used.

- Communication System
- ALU (Arithmetic Logic Unit)
- Serial to parallel converter

Parity Generator and Checker

A parity generator is a combinational logic circuit that generates the parity bit in the transmitter. On the other hand, a circuit that checks the parity in the receiver is called parity checker. A combined circuit or devices of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data word.

The sum of the data bits and parity bits can be even or odd. In even parity, the added parity bit will make the total number of 1s an even amount whereas in odd parity the added parity bit will make the total number of 1s odd amount.

Such error detecting and correction can be implemented by using Ex-OR gates (since Ex-OR gate produce zero output when there are even number of inputs).

Parity Generator:

It is combinational circuit that accepts an n-1 bit stream data and generates the additional bit that is to be transmitted with the bit stream. This additional or extra bit is termed as a parity bit.

Types: 1) Even Parity 2) Odd Parity

In even parity bit scheme, the parity bit is '0' if there are even number of 1s in the data stream and the parity bit is '1' if there are odd number of 1s in the data stream.

In odd parity bit scheme, the parity bit is '1' if there are even number of 1s in the data stream and the parity bit is '0' if there are odd number of 1s in the data stream.

Even Parity Generator

- a 3-bit message is to be transmitted with an even parity bit. Let the three inputs A, B and C are applied to the circuits and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P.

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

A \ BC	BC			
	00	01	11	10
00	0	1	0	1
01	1	0	1	0

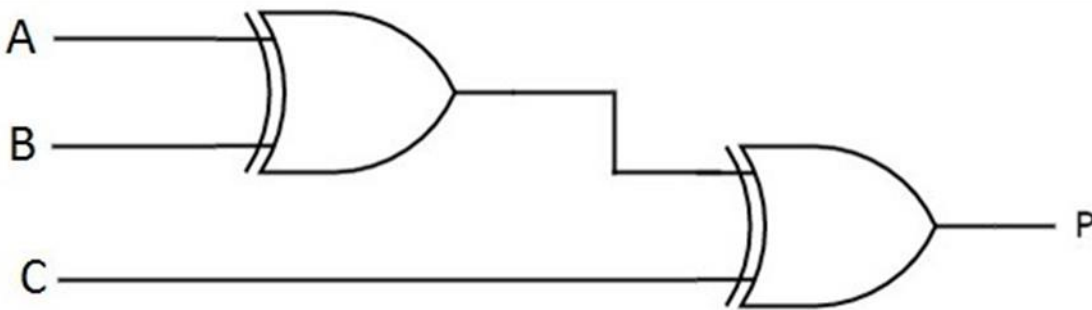
$$P = \bar{A} \bar{B} C + \bar{A} B \bar{C} + A \bar{B} \bar{C} + A B C$$

$$= \bar{A} (\bar{B} C + B \bar{C}) + A (\bar{B} \bar{C} + B C)$$

$$= \bar{A} (B \oplus C) + A (\overline{B \oplus C})$$

$$P = A \oplus B \oplus C$$

$$P = A \oplus B \oplus C$$



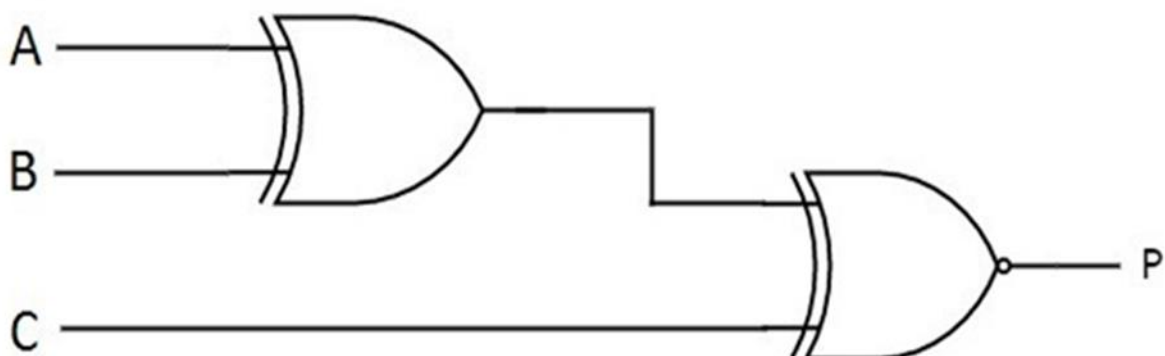
Odd Parity Generator

- the 3-bit data is to be transmitted with an odd parity bit. The three inputs are A, B and C and P is the output parity bit. The total number of bits must be odd in order to generate the odd parity bit.

3-bit message			Odd parity bit generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

BC				
	00	01	11	10
A	0	1	3	2
	00	0	1	0
01	4	5	7	6
	0	1	0	1

$$P = A \oplus B \text{ Ex-NOR } C$$



Parity Checker:

It is a logic circuit that checks for possible errors in the transmission. This circuit can be an even parity checker or odd parity checker depending on the type of parity generated at the transmission end. When this circuit is used as even parity checker, the number of input bits must always be even.

Consider that three input message along with even parity bit is generated at the transmitting end. These 4 bits are applied as input to the parity checker circuit which checks the possibility of error on the data. Since the data is transmitted with even parity, four bits received at circuit must have an even number of 1s.

If any error occurs, the received message consists of odd number of 1s. The output of the parity checker is denoted by PEC (parity error check).

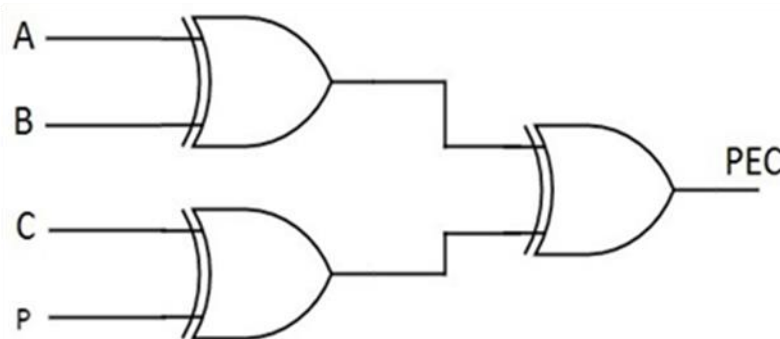
Even Parity Checker:

The below table shows the truth table for the even parity checker in which $PEC = 1$ if the error occurs, i.e., the four bits received have odd number of 1s and $PEC = 0$ if no error occurs, i.e., if the 4-bit message has even number of 1s.

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

CP \ AB	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

$$\begin{aligned}
 PEC &= \bar{A} \bar{B} (\bar{C} D + \underline{C} \bar{D}) + \bar{A} B (\bar{C} \bar{D} + C D) + A B (\bar{C} D + C \bar{D}) + A \bar{B} (\bar{C} \bar{D} + C D) \\
 &= \bar{A} \bar{B} (C \oplus D) + \bar{A} B (\overline{C \oplus D}) + A B (C \oplus D) + A \bar{B} (\overline{C \oplus D}) \\
 &= (\bar{A} \bar{B} + A B) (C \oplus D) + (\bar{A} B + \underline{A} \bar{B}) (\overline{C \oplus D}) \\
 &= (A \oplus B) \oplus (C \oplus D)
 \end{aligned}$$

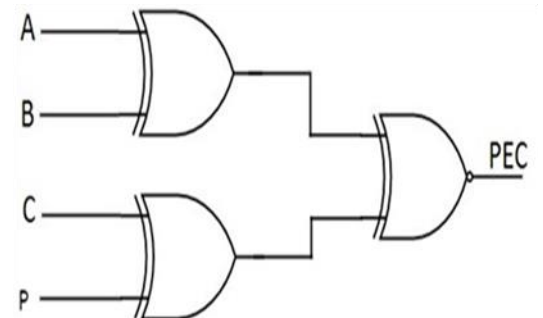


Odd Parity Checker:

The below figure shows the truth table for odd parity generator where **PEC = 1** if the 4-bit message received consists of **even number of 1s** (hence the error occurred) and **PEC= 0** if the message contains **odd number of 1s** (that means no error).

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

AB	CP			
	00	01	11	10
00	1 ⁰	0 ¹	1 ³	0 ²
01	0 ⁴	1 ⁵	0 ⁷	1 ⁶
11	1 ¹²	0 ¹³	1 ¹⁵	0 ¹⁴
10	0 ⁸	1 ⁹	0 ¹¹	1 ¹⁰

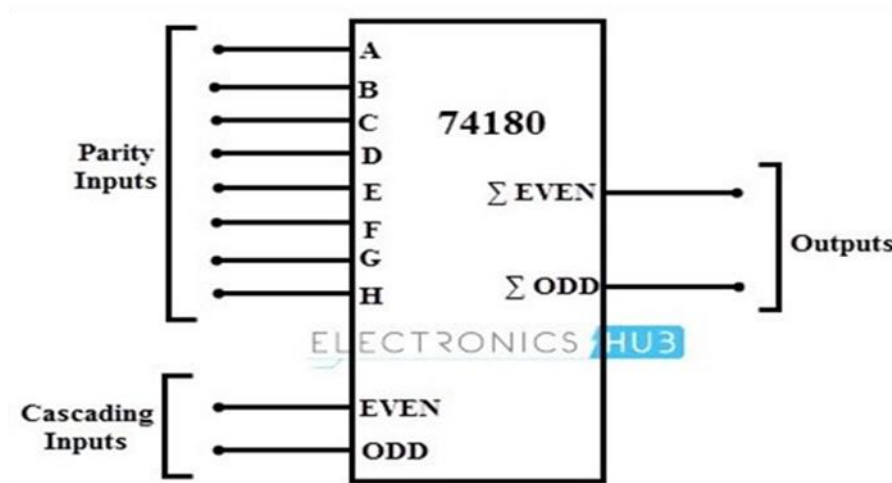


$$PEC = (A \text{ Ex-NOR } B) \text{ Ex-NOR } (C \text{ Ex-NOR } D)$$

Parity Generator/Checker IC 74180

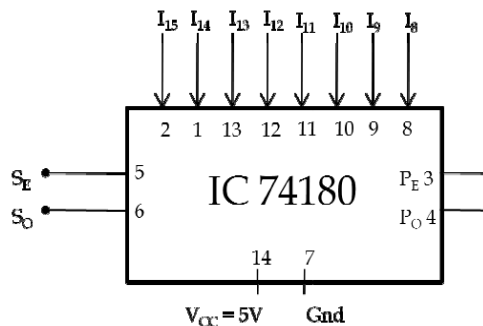
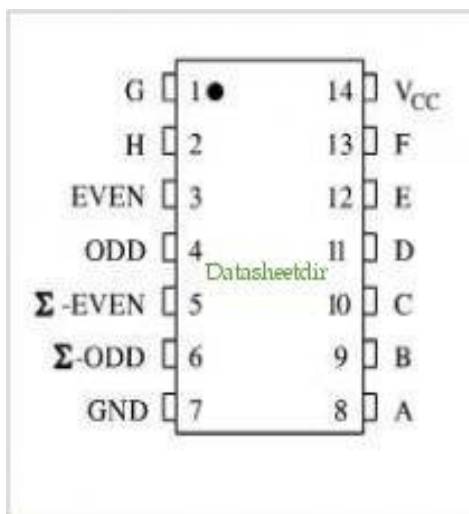
It is a 9-bit parity generator or checker used to detect errors in high speed data transmission or data retrieval systems. The figure below shows the pin diagram of **74180 IC**

This IC can be used to generate a 9-bit odd or even parity code or it can be used to check for odd or even parity in a 9-bit code (8 data bits and one parity bit).



74180 – TTL parity generator-checker:

The 74180 – TTL parity generator-checker



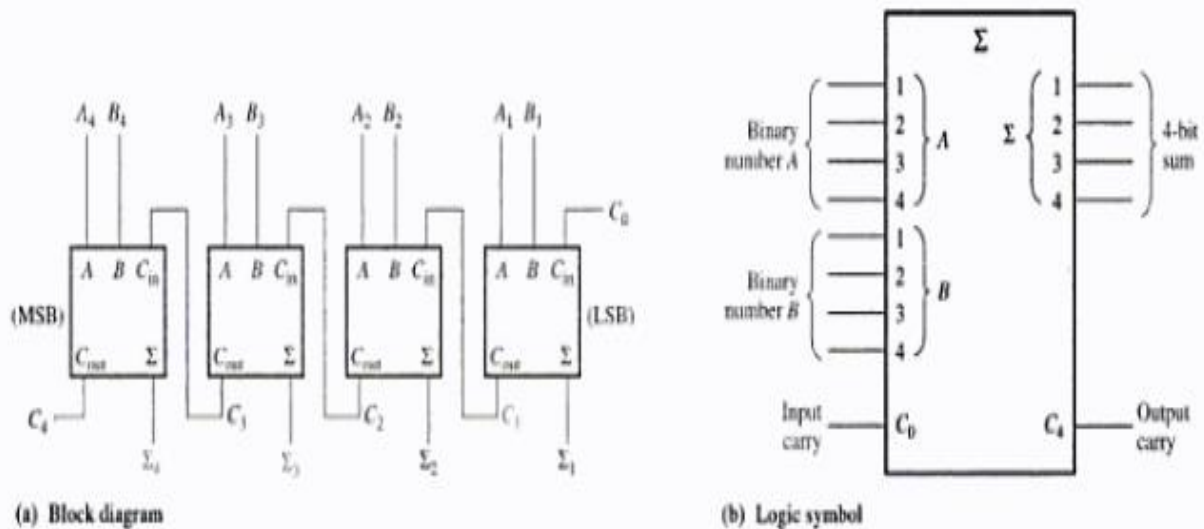
Inputs			Outputs	
Σ of H's at A thru H	Even	Odd	Σ Even	Σ Odd
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = High Level, L = Low Level, X = Don't Care

Four-bit Parallel Adder/Subtractor:(IC7483)

Four bit parallel adder:

A group of four bits is called a **nibble**. A basic 4-bit parallel adder is implemented with four full-adder stages as shown in Figure 6-17. Again, the LSBs (A_1 and B_1) in each number being added go into the right-most full-adder; the higher-order bits are applied as shown to the successively higher-order adders, with the MSBs (A_4 and B_4) in each number being applied to the left-most full-adder. The carry output of each adder is connected to the carry input of the next higher-order adder as indicated. These are called *internal carries*.



▲ FIGURE 6-17

A 4-bit parallel adder

In terms of the method used to handle carries in a parallel adder, there are two types: the *ripple carry* adder and the *carry look-ahead* adder. A **ripple carry** adder is one in which the carry output of each full-adder is connected to the carry input of the next higher-order stage (a stage is one full-adder). The sum and the output carry of any stage cannot be produced until the input carry occurs; this causes a time delay in the addition process. The carry propagation delay for each full-adder is the time from the application of the input carry until the output carry occurs, assuming that the A and B inputs are already present.

A method of speeding up the addition process by eliminating this ripple carry delay is called **look-ahead carry** addition. The look-ahead carry adder anticipates the output carry of each stage, and based on the input bits of each stage, produces the output carry by either *carry generation* or *carry propagation*.

Carry generation occurs when an output carry is produced (generated) internally by the full-adder. A carry is generated only when both input bits are 1s. The generated carry, C_g , is expressed as the AND function of the two input bits, A and B .

$$C_g = AB$$

Carry propagation occurs when the input carry is rippled to become the output carry. An input carry may be propagated by the full-adder when either or both of the input bits are 1s. The propagated carry, C_p , is expressed as the OR function of the input bits.

$$C_p = A + B$$

Truth Table for a 4-Bit Parallel Adder

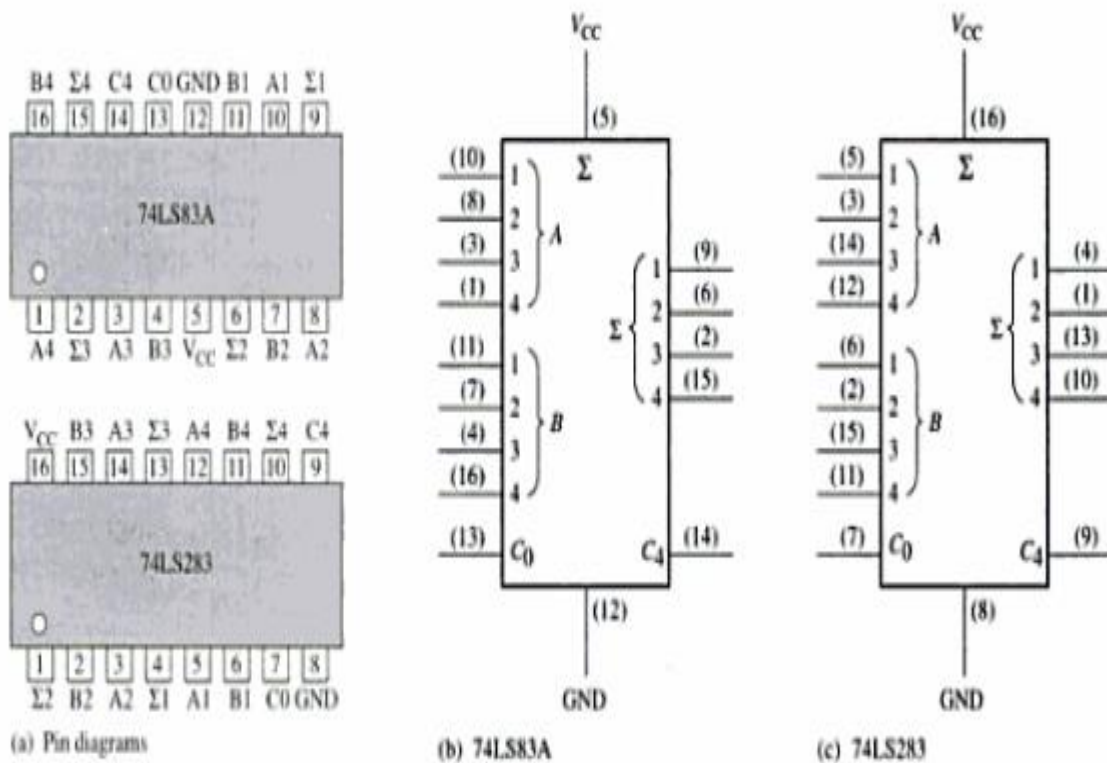
Table 6-3 is the truth table for a 4-bit adder. On some data sheets, truth tables may be called *function tables* or *functional truth tables*. The subscript n represents the adder bits and can be 1, 2, 3, or 4 for the 4-bit adder. C_{n-1} is the carry from the previous adder. Carries C_1 , C_2 , and C_3 are generated internally. C_0 is an external carry input and C_4 is an output. Example 6-3 illustrates how to use Table 6-3.

► **TABLE 6-3**

C_{n-1}	A_n	B_n	Σ_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Examples of 4 bit parallel adder ICs:

Examples of 4-bit parallel adders that are available in IC form are the 74LS83A and the 74LS283 low-power Schottky TTL devices. The 74LS83A and the 74LS283 are functionally identical to each other but not pin compatible; that is, the pin numbers for the inputs and outputs are different due to different power and ground pin connections. For the 74LS83A, V_{CC} is pin 5 and ground is pin 12 on the 16-pin package. For the 74LS283, V_{CC} is pin 16 and ground is pin 8, which is a more standard configuration. Pin diagrams and logic symbols for both of these devices are shown, with pin numbers in parentheses on the logic symbols, in Figure 6-18.

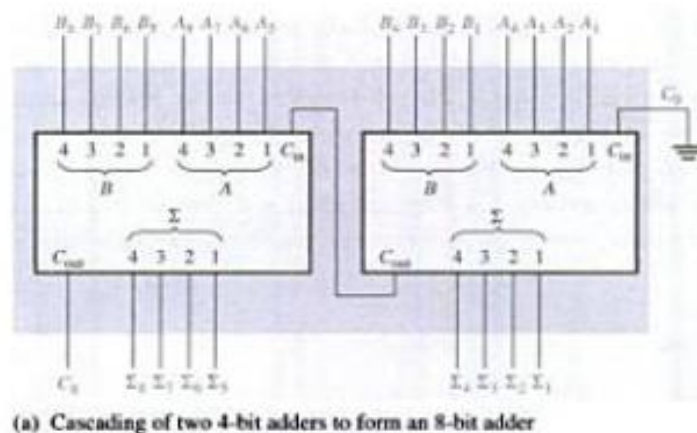


▲ FIGURE 6-18

4-bit Parallel adder can be expanded to handle the addition of two 8-bit numbers by using two 4-bit adders.

Carry input of Low-order adder(C_0) is connected to ground because there is no carry into least significant bit position.

Carry output of Low-order adder is connected to carry input of high-order adder.

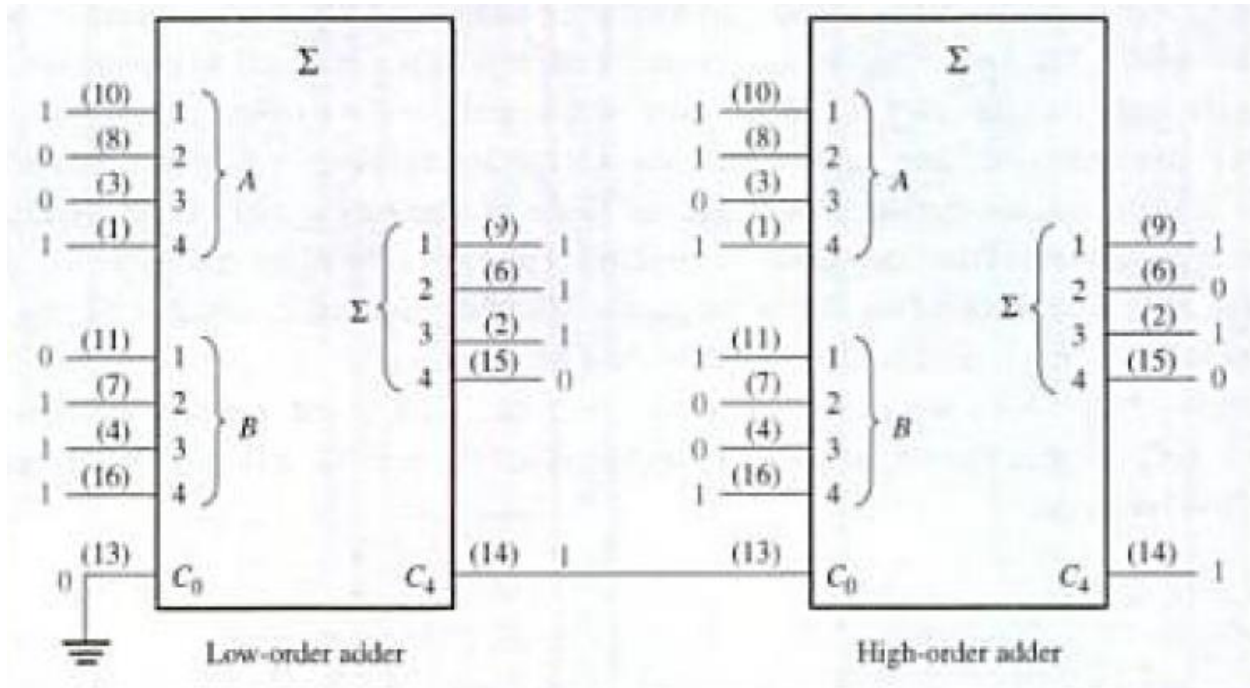


Example:

Show how two 74LS83A adders can be connected to form an 8-bit parallel adder.

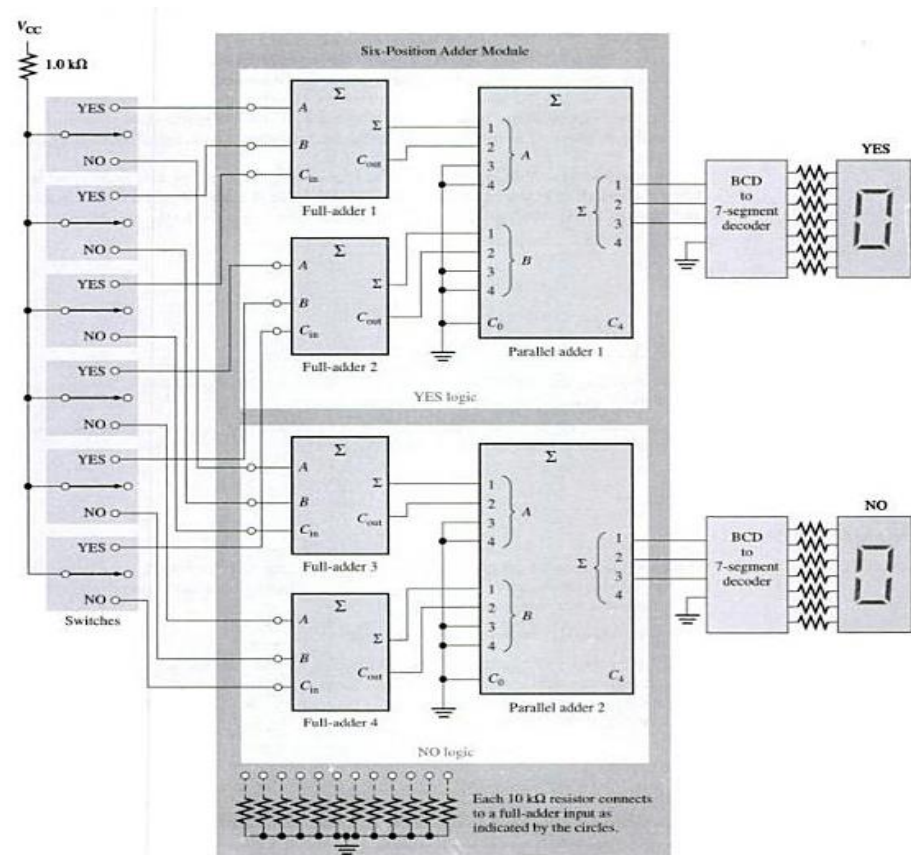
Show output bits for the following 8-bit input numbers:

$A_8A_7A_6A_5A_4A_3A_2A_1=10111001$, $B_8B_7B_6B_5B_4B_3B_2B_1=10011110$



Application:

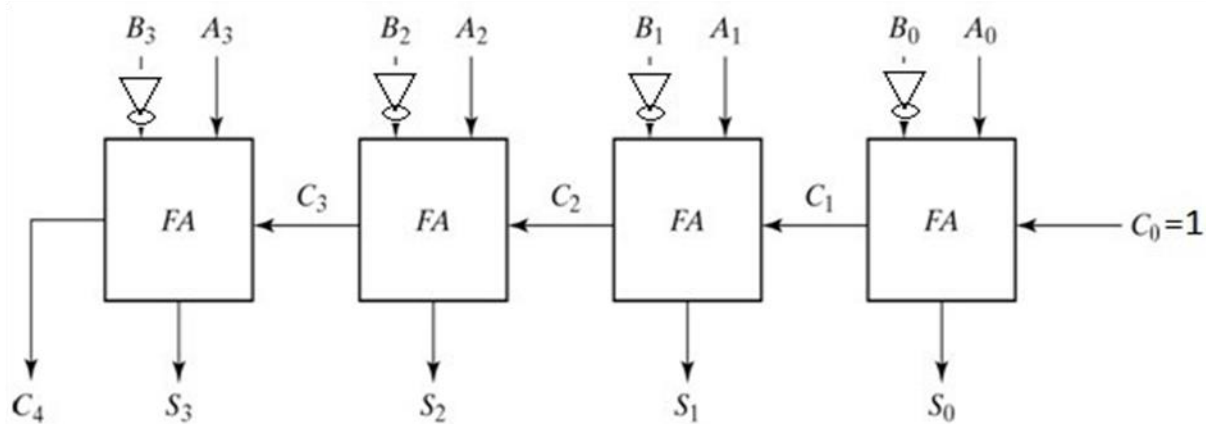
Simple voting System



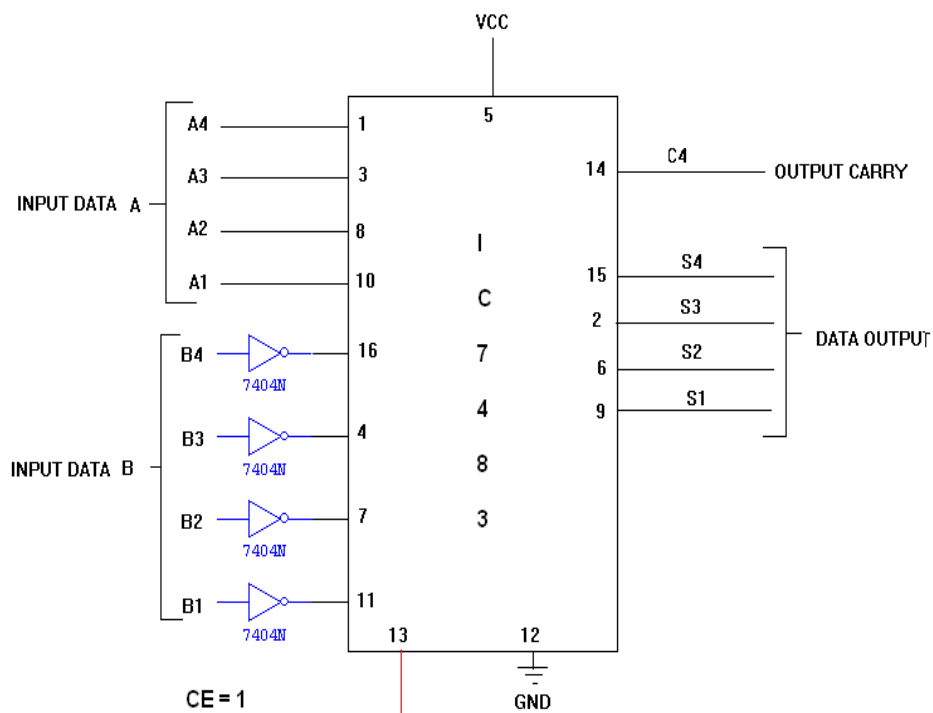
4-bit parallel subtractor:

The circuit for subtracting $A-B$ consists of an adder with inverters, placed between each data input 'B' and the corresponding input of full adder. The input carry C_0 must be equal to 1 when performing subtraction.

- ✓ In general subtraction, we made as $A-B$. Means $A+(-B)$. We can write it as 2's Complement of B is added to the A.
- ✓ 2's complement means 1's complement + 1. We make add inverter across B and take as carry 1. then it will also acts as 2's complement of B.
- ✓ Then we make add that to A, by using adder circuit.

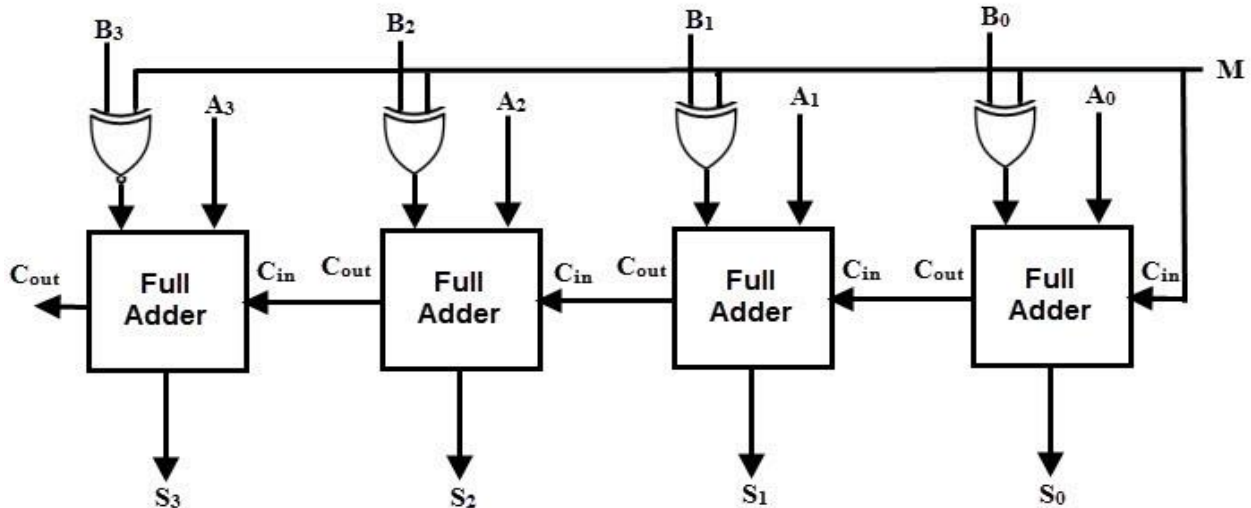


4-bit parallel subtractor



4-BIT

- When $M = 1$, the circuit is a subtractor and when $M = 0$, the circuit becomes adder. The Ex-OR gate consists of two inputs to which one is connected to the B and other to input M. When $M = 0$, B Ex-OR of 0 produce B. Then full adders add the B with A with carry input zero and hence an addition operation is performed.
- When $M = 1$, B Ex-OR of 0 produce B complement and also carry input is 1. Hence the complemented B inputs are added to A and 1 is added through the input carry, nothing but a 2's complement operation. Therefore, the subtraction operation is performed.



Pin diagram

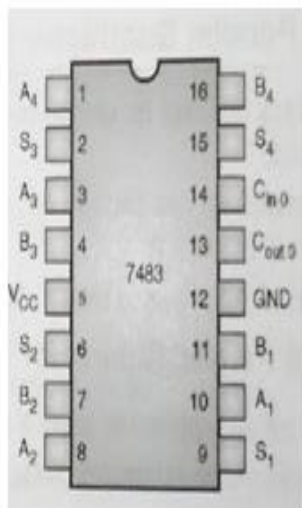
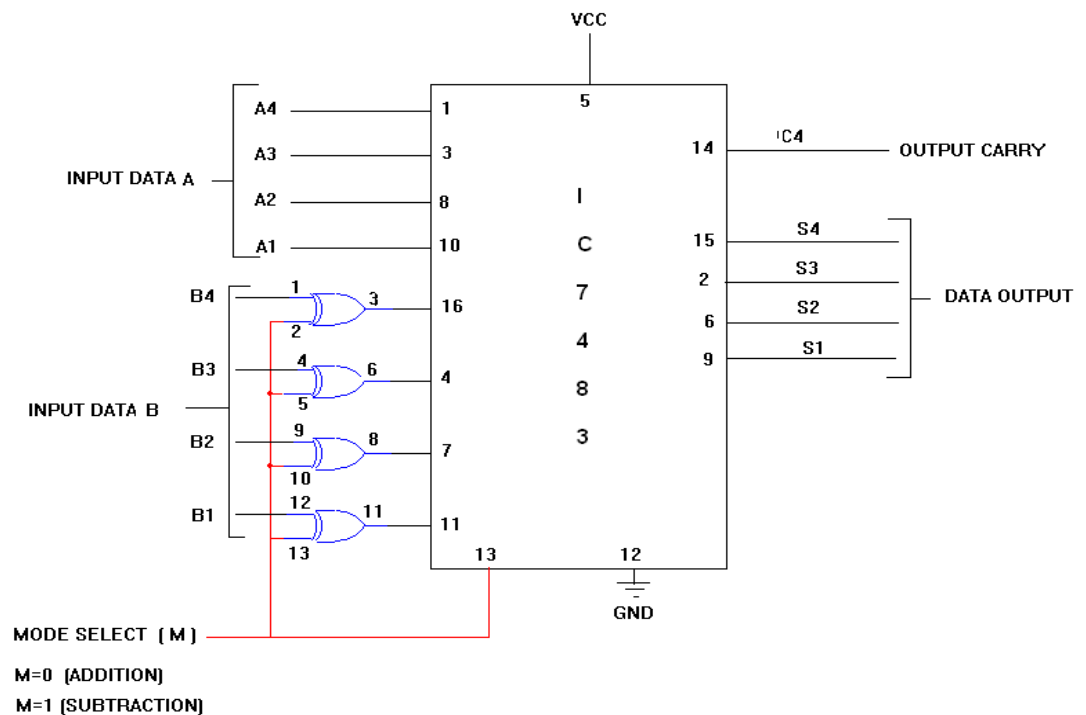


Fig1. Pin diagram of IC 7483

Logic diagram



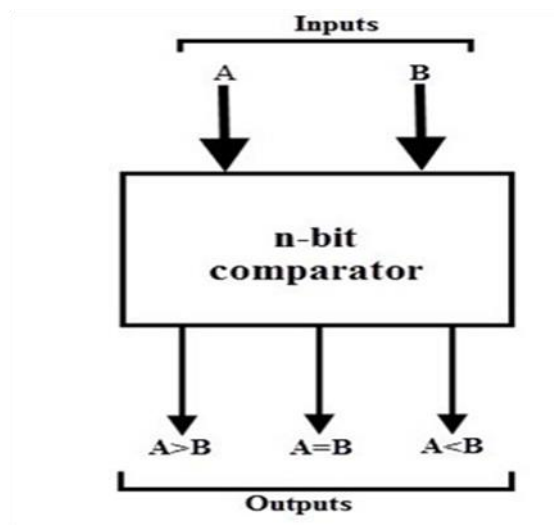
Magnitude Comparator (IC 7485)

Data comparison is needed in digital systems while performing arithmetic or logical operations. This comparison determines whether one number is greater than, equal, or less than the other number.

A digital comparator is widely used in combinational system and is specially designed to compare the relative magnitudes of binary numbers. These are also available in IC form with different bit comparing configurations such as 4-bit, 8-bit, etc. Whenever we want to compare the two binary numbers, first we have to compare the most significant bits (MSB).

If these MSBs are equal, then only we need to compare the next significant bits. But if the MSBs are not equal, then it would be clear that either A is greater than or less than B and the process of comparison ceases.

Magnitude Comparators: Comparators with three output terminals and checks for three conditions i.e. greater than or less than or equal to is magnitude comparator.



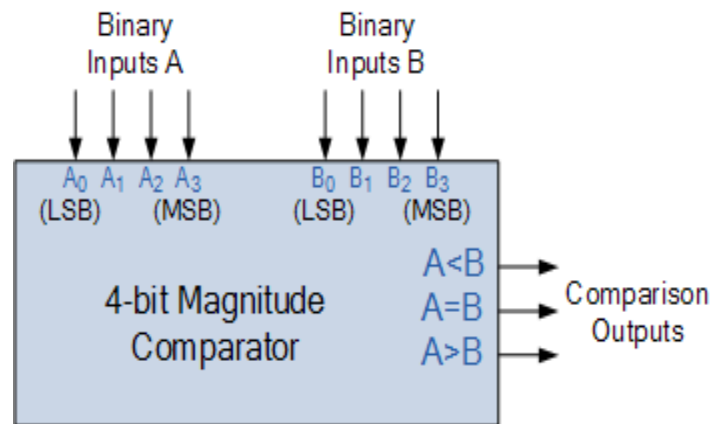
Comparators can compare 4-bit numbers depending on the application requirement. These are available in TTL as well as CMOS logic family ICs and some of these ICs include IC 7485 (4-bit comparator), IC 4585 (4-bit comparator in CMOS family) and IC 74AS885 (8-bit comparator).

4-bit Magnitude Comparator(IC 7485):

Basic function:

Compare the magnitudes of two binary numbers to determine relationship of those quantities.

74HC85 is a 4-bit comparator



It can be used to compare two four-bit words. The two 4-bit numbers are $A = A_3 A_2 A_1 A_0$ and $B = B_3 B_2 B_1 B_0$ where A_3 and B_3 are the most significant bits.

It compares each of these bits in one number with bits in that of other number and produces one of the following outputs as $A = B$, $A < B$ and $A > B$.

The output logic statements of this converter are

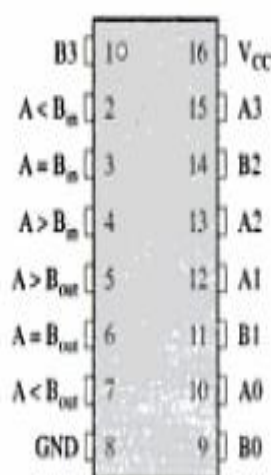
If $A_3 = 1$ and $B_3 = 0$, then A is greater than B ($A > B$). Or If $A_3 = B_3$, and if $A_2 = 1$ and $B_2 = 0$, then $A > B$. Or

If $A_3 = B_3$, & $A_2 = B_2$, and if $A_1 = 1$, and $B_1 = 0$, then $A > B$. Or

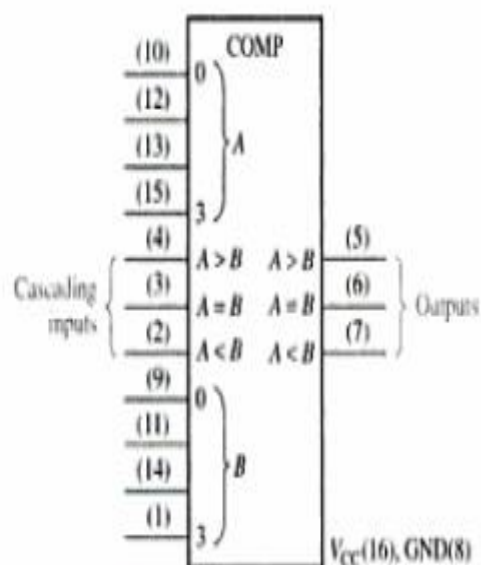
If $A_3 = B_3$, $A_2 = B_2$, and $A_1 = B_1$, and if $A_0 = 1$ and $B_0 = 0$, then $A > B$.

The 74HC85 is a comparator that is also available in other IC families. The pin diagram and logic symbol are shown in Figure 6-27. Notice that this device has all the inputs and outputs of the generalized comparator previously discussed and, in addition, has three cascading inputs: $A < B$, $A = B$, $A > B$. These inputs allow several comparators to be cascaded for comparison of any number of bits greater than four. To expand the comparator, the $A < B$, $A = B$, and $A > B$ outputs of the lower-order comparator are connected to the corresponding cascading inputs of the next higher-order comparator. The lowest-order comparator must have a HIGH on the $A = B$ input and LOWs on the $A < B$ and $A > B$ inputs.

► FIGURE 6-27



(a) Pin diagram



(b) Logic symbol

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

Functional table for 74LS85:

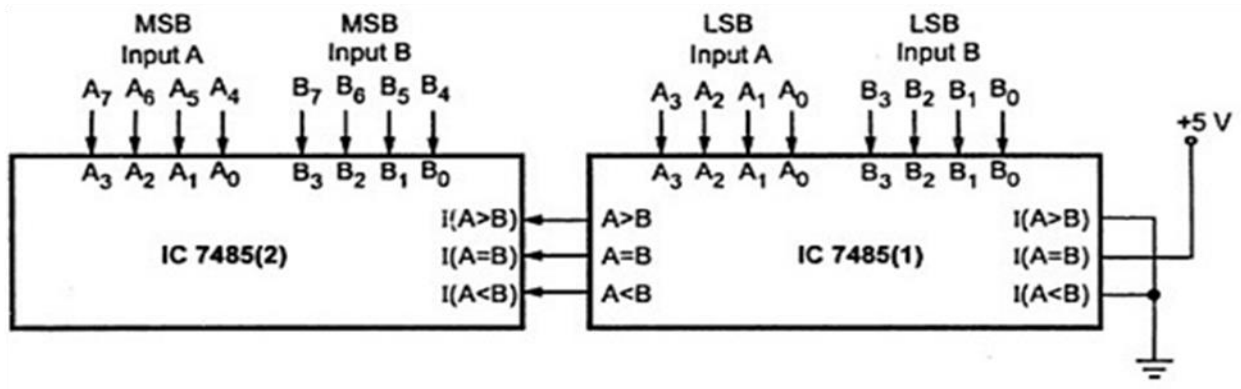
Comparing inputs A B	cascading inputs			output		
	$\Sigma(A > B)$	$\Sigma(A = B)$	$\Sigma(A < B)$	A > B	A = B	A < B
A > B	X	X	X	1	0	0
A = B	1	0	0	1	0	0
	X	1	X	0	1	0
	0	0	1	0	0	1
	0	0	0	1	0	1
	1	0	1	0	0	0
A < B	X	X	X	0	0	1

Applications of Comparators:

- These are used in the address decoding circuitry in computers and microprocessor based devices to select a specific input/output device for the storage of data.
- These are used in control applications in which the binary numbers representing physical variables such as temperature, position, etc. are compared with a reference value. Then the outputs from the comparator are used to drive the actuators so as to make the physical variables closest to the set or reference value.
- Process controllers ,servo-motor control

8 Bit Comparators using IC7485:

An 8-bit comparator compares the two 8-bit numbers by cascading of two 4-bit comparators. The circuit connection of this comparator is shown below in which the lower order comparator A<B, A=B and A>B outputs are connected to the respective cascade inputs of the higher order comparator



ALL IC NOs

Binary parallel Adder: IC74LS83/IC74LS283

Decoder: 3 to 8 => IC74x138

2 to 4 => IC74x139

7 segment Display => IC7447

Encoder 8 to 3 Priority : IC74LS348/148

Qud 2 input Mux: IC74x157

Dual 1 to 4 Demux : IC74x154

PARITY Generator/Checker : IC74180/280 Comparators: 4 bit => IC7485

8 bit => IC74x682

Multiplexer : 4x1 => IC74LS153

8x1 => IC74LS151

16x1 => IC74LS150

UNIT-V SEQUENTIAL LOGIC IC'S AND MEMORIES

Familiarity with commonly available 74XX & CMOS 40XX series ICs-All Types of Flip-flops, Conversion of Flip flops, Synchronous Counters , Decade Counters ,Shift Registers ,

MEMORIES - ROM Architecture, Types of ROMS & Applications RAM Architecture, Static & Dynamic RAMs.

Flip Flops

Latches:

The latch is a type of temporary storage device that has two stable states (bistable) and is normally placed in a category separate from that of flip-flops. Latches are basically similar to flip-flops because they are bistable devices that can reside in either of two states using a feedback arrangement, in which the outputs are connected back to the opposite inputs. The main difference between latches and flip-flops is in the method used for changing their state.

Flip Flop:

A circuit that changes from 1 to 0 or from 0 to 1 when current is applied. It is one bit storage location.

Flip flops are actually an application of logic gates. When a certain input value is given to them, they will be remembered and executed, if the logic gates are designed correctly. A higher application of flip flops is helpful in designing better electronic circuits.

The most commonly used application of flip flops is in the implementation of a feedback circuit. As a memory relies on the feedback concept, flip flops can be used to design it.

Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes.

There are basically four main types of latches and flip-flops: SR, D, JK, and T. The major differences in these flip-flop types are the number of inputs they have and how they change state. For each type, there are also different variations that enhance their operations. In this chapter, we will look at the operations of the various latches and flip-flops.

There are mainly four types of flip flops that are used in electronic circuits.

1. **The basic Flip Flop or S-R Flip Flop**
2. **Delay Flip Flop [D Flip Flop]**
3. **J-K Flip Flop**
4. **T Flip Flop**

S-R Flip Flop:

The SET-RESET flip flop is not designed with the help of two NOR gates and also two NAND gates. These flip flops are also called S-R Latch.

S-R Flip Flop using NOR Gate

The design of such a flip flop includes two inputs, called the SET [S] and RESET [R]. There are also two outputs, Q and Q'. The diagram and truth table is shown below.

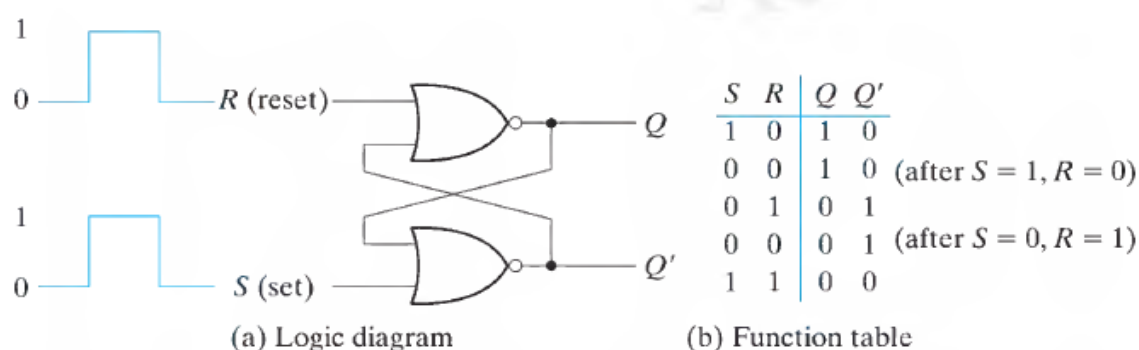


Fig. 5-3 SR Latch with NOR Gates

The operation has to be analyzed with the 4 inputs combinations together with the 2 possible previous states.

From the diagram it is evident that the flip flop has mainly four states. They are

1. When $S=1, R=0$ the output becomes $Q=1, Q'=0$

This SR flip flop function table is constructed based on the XOR gate. In XOR gate if any of the input is 1 the output becomes 1.

In this state when $S=1$ and $R=0$ the output Q becomes set (1). So this state is also called the SET state.

2. When $S=0, R=1$, the output becomes $Q=0, Q'=1$

In this state When $R=1$ it resets the output. So this state is known as the RESET state. In both the states you can see that the outputs are just compliments of each other and that the value of Q follows the value of S .

3. When $S=0, R=0$ the output is $Q \& Q' = \text{Remember (memory)}$

If both the values of S and R are switched to 0, then the circuit remembers the value of S and R in their previous state.

4. When $S=1, R=1$ the output $Q=0, Q'=0$ [Invalid]

This is an invalid state because the values of both Q and Q' are 0. They are supposed to be compliments of each other. Normally, this state must be avoided.

S-R Flip Flop using NAND Gate

The above SR flip flop can be constructed using NAND gate.

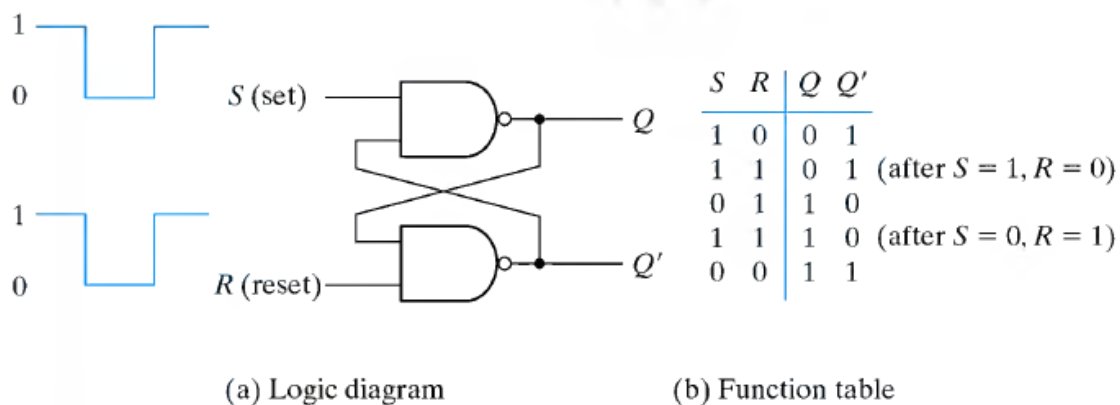


Fig. 5-4 SR Latch with NAND Gates

Like the NOR Gate S-R flip flop, this one also has four states. They are

1. $S=1, R=0, Q=0, Q'=1$

This state is also called the SET state.

2. $S=0, R=1, Q=1, Q'=0$

This state is known as the RESET state.

In both the states you can see that the outputs are just compliments of each other and that the value of Q follows the compliment value of S .

3. $S=0, R=0, Q=1, \& Q'=1$ [Invalid]

If both the values of S and R are switched to 0 it is an invalid state because the values of both Q and Q' are 1. They are supposed to be compliments of each other. Normally, this state must be avoided.

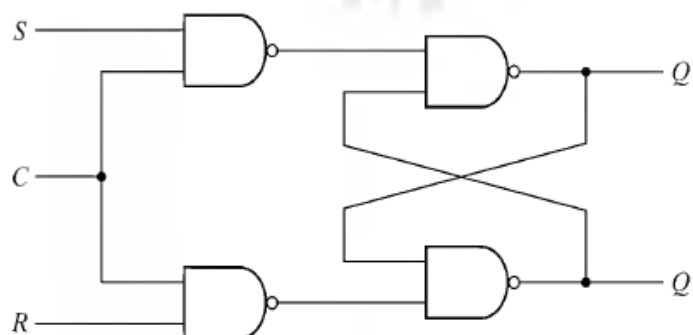
4. $S=1, R=1, Q \& Q' = \text{Remember}$

If both the values of S and R are switched to 1, then the circuit remembers the value of S and R in their previous state.

Clocked S-R Flip Flop

- ❖ It is also called a Gated S-R flip flop.
- ❖ The problems with S-R flip flops using NOR and NAND gate is the invalid state.
- ❖ This problem can be overcome by using a bistable SR flip-flop that can change outputs when certain invalid states are met, regardless of the condition of either the Set or the Reset inputs.
- ❖ For this, a clocked S-R flip flop is designed by adding two AND neither gates to a basic NOR Gate flip flop.
- ❖ The circuit diagram and truth table is shown below.

The circuit of the S-R flip flop using NAND Gate and its truth table is shown below.



(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

Fig. 5-5 SR Latch with Control Input

- A clock pulse [CP] is given to the inputs of the AND Gate.
- When the value of the clock pulse is '0', the outputs of both the AND Gates remain '0'.

- As soon as a pulse is given the value of CP turns '1'.
- This makes the values at S and R to pass through the NOR Gate flip flop. But when the values of both S and R values turn '1', the HIGH value of CP causes both of them to turn to '0' for a short moment.
- As soon as the pulse is removed, the flip flop state becomes intermediate.
- Thus either of the two states may be caused, and it depends on whether the set or reset input of the flip-flop remains a '1' longer than the transition to '0' at the end of the pulse. Thus the invalid states can be eliminated.

Excitation Table of the SR Latch

- During the design process we usually know the transition from present state to next state and wish to find the latch input conditions that will cause the required transition.
- For this reason, we need a table that lists the required inputs for a given change of state. Such a table is called an excitation table, and it specifies the excitation behavior of the sequential circuits. These are used in the synthesis (design) of sequential circuits, which we shall see later.
- The excitation of the SR latch is as follows:

Excitation Table:

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeter
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeter

Note: Indeter = not used

K Map for Q_{n+1} :

SR Q_n					
		00	01	11	10
0				X	1
1	1			X	1

$$Q_{n+1} = S + \bar{R} \cdot Q_n$$

D-Flip Flop:

- D flip flop is actually a slight modification of the above explained clocked SR flip-flop. From the figure you can see that the D input is connected to the S input and the complement of the D input is connected to the R input.
- The D input is passed on to the flip flop when the value of CP is '1'.
- When CP is HIGH, the flip flop moves to the SET state. If it is '0', the flip flop switches to the CLEAR state.
- As long as the clock input $C = 0$, the SR latch has both inputs equal to 0 and it can't change its state regardless of the value of D
- When C is 1, the latch is placed in the set or reset state based on the value of D.
 - If $D = 1$, the Q output goes to 1.
 - If $D = 0$, the Q output goes to 0.

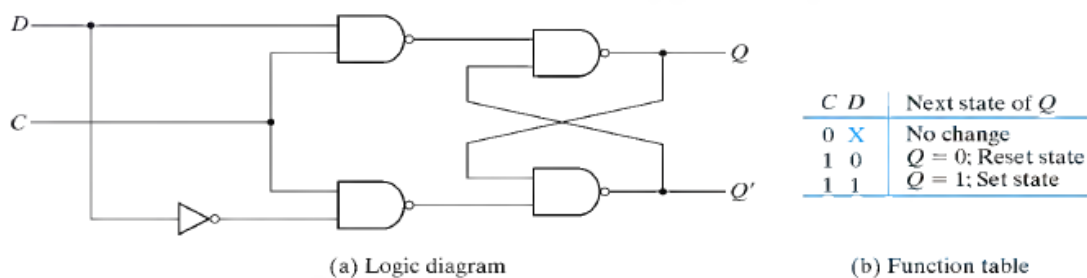
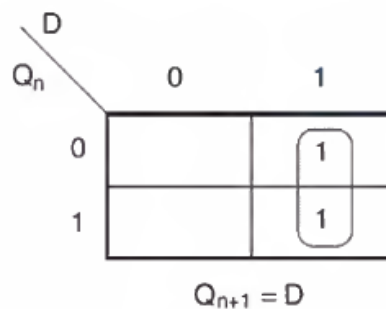


Fig. 5-6 D Latch

Excitation Table:

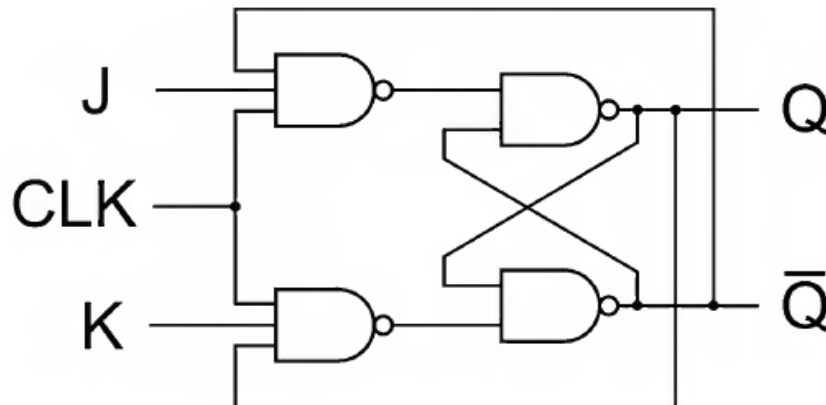
Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

K- Map for Q_{n+1} :



3. J-K Flip Flop

- ❖ A J-K flip flop can also be defined as a modification of the S-R flip flop. The only difference is that the intermediate state is more refined and precise than that of a S-R flip flop.



- ❖ The behavior of inputs J and K is same as the S and R inputs of the S-R flip flop. The letter J stands for SET and the letter K stands for CLEAR.
- ❖ When both the inputs J and K have a HIGH state, the flip-flop switches to the complement state. So, for a value of $Q = 1$, it switches to $Q=0$ and for a value of $Q = 0$, it switches to $Q=1$.
- ❖ The circuit includes two 3-input AND gates. The output Q of the flip flop is returned back as a feedback to the input of the AND along with other inputs like K and clock pulse [CP].
- ❖ So, if the value of CP is '1', the flip flop gets a CLEAR signal and with the condition that the value of Q was earlier 1.
- ❖ Similarly output Q' of the flip flop is given as a feedback to the input of the AND along with other inputs like J and clock pulse [CP].
- ❖ So the output becomes SET when the value of CP is 1 only if the value of Q' was earlier 1.
- ❖ The output may be repeated in transitions once they have been complimented for $J=K=1$ because of the feedback connection in the JK flip-flop.
- ❖ This can be avoided by setting a time duration lesser than the propagation delay through the flip-flop.
- ❖ The restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction.

Characteristic table:

Clk	J	K	Q _{n+1}
0	X	X	Memory
1	0	0	Memory
1	0	1	0
1	1	0	1 (Set)
1	1	1	Toggle

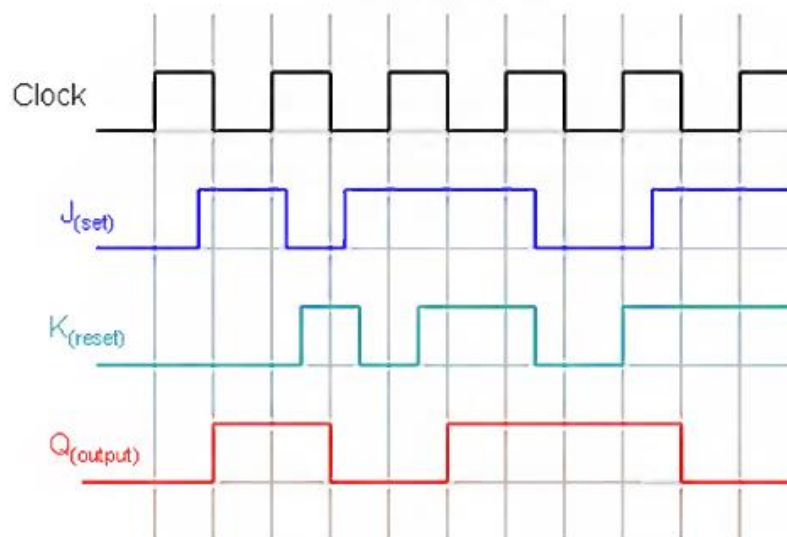
Excitation table for JK Flipflop K map for Q_{n+1}:

Q _n	J	K	Q _{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Q _n \	00	01	11	10
0			1	1
1	1			1

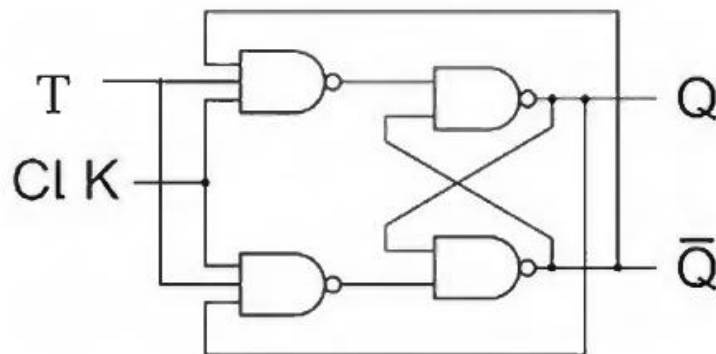
$$Q_{n+1} = J \cdot \overline{Q_n} + \overline{K} \cdot Q_n$$

Timing Diagram:



4. T Flip Flop

- ❖ This is a much simpler version of the J-K flip flop.
- ❖ Both the J and K inputs are connected together and thus are also called a single input J-K flip flop.
- ❖ When clock pulse is given to the flip flop, the output begins to toggle.
- ❖ Here also the restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction. Take a look at the circuit and truth table below.



Excitation Table for T Flip Flop:

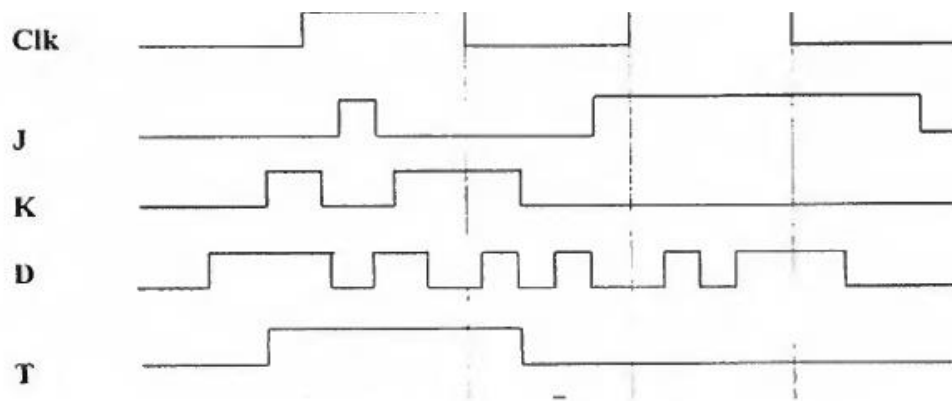
Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

K map for T Flip Flop:

		T	
		0	1
Q_n	0		1
	1	1	

Characteristic Equation:

$$Q_{n+1} = T \cdot \overline{Q_n} + \overline{T} \cdot Q_n$$

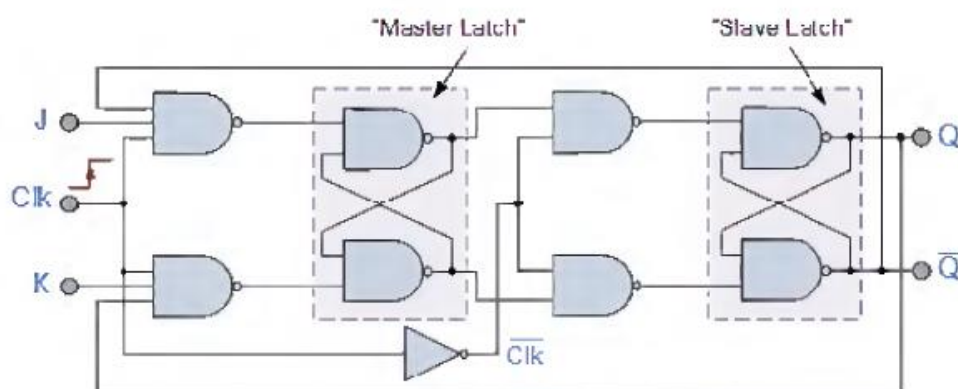


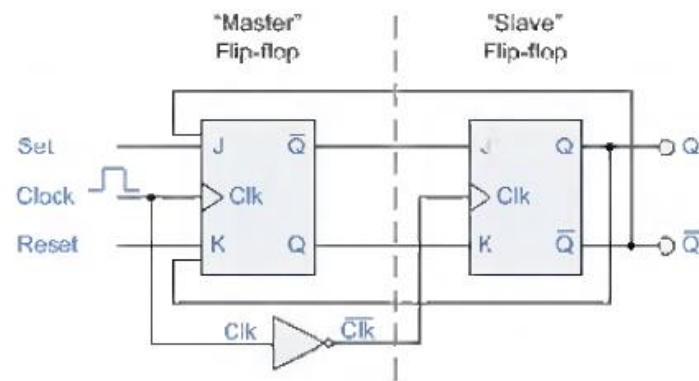
Master-Slave Flip Flop Circuit

Before knowing more about the master-slave flip flop you have to know more on the basics of a J-K flip flop and S-R flip flop. To know more about the flip flops, click on the link below.

Master-slave flip flop is designed using two separate flip flops. Out of these, one acts as the master and the other as a slave. The figure of a master-slave J-K flip flop is shown below.

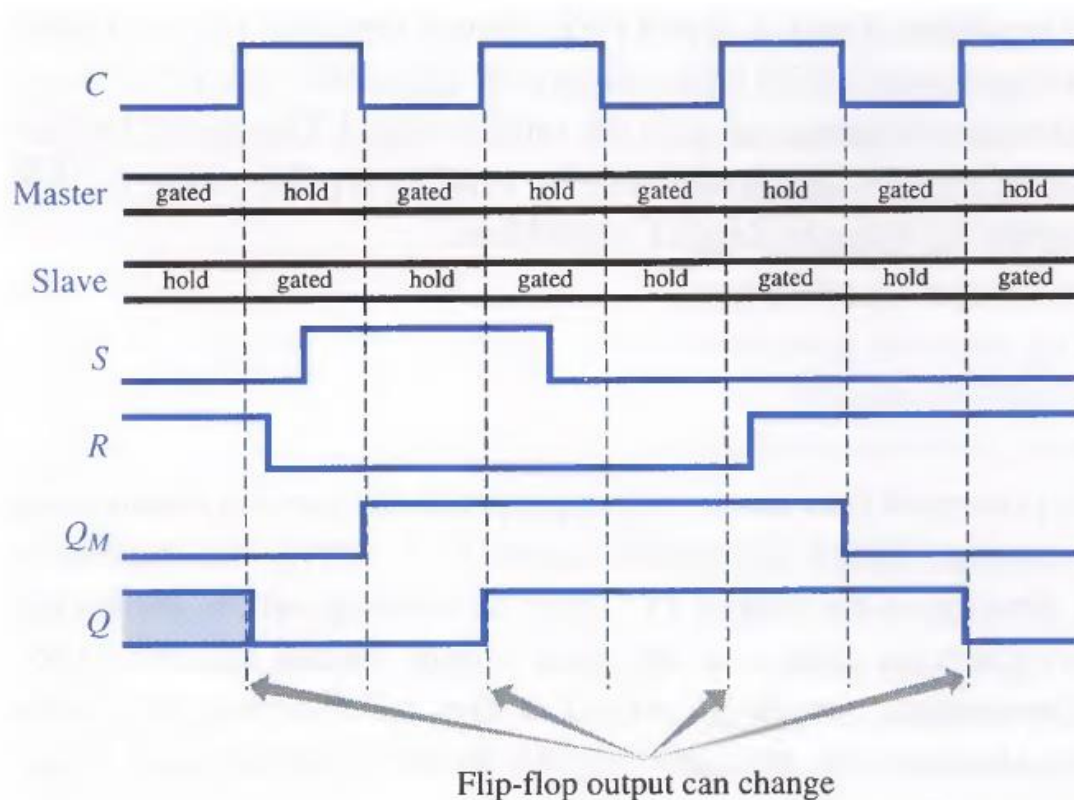
From the below figure you can see that both the J-K flip flops are presented in a series connection. The output of the master J-K flip flop is fed to the input of the slave J-K flip flop. The output of the slave J-K flip flop is given as a feedback to the input of the master J-K flip flop. The clock pulse [Clk] is given to the master J-K flip flop and it is sent through a NOT Gate and thus inverted before passing it to the slave J-K flip flop.





Working

When Clock=1, the master J-K flip flop gets disabled. The Clock input of the master input will be the opposite of the slave input. So the master flip flop output will be recognized by the slave flip flop only when the Clock value becomes 0. Thus, when the clock pulse makes a transition from 1 to 0, the locked outputs of the master flip flop are fed through to the inputs of the slave flip-flop making this flip flop edge or pulse-triggered. To understand better take a look at the timing diagram illustrated below.



Flip Flop Conversion

For the conversion of one flip flop to another, a combinational circuit has to be designed first. If a JK Flip Flop is required, the inputs are given to the combinational circuit and the output of the combinational circuit is connected to the inputs of the actual flip flop. Thus, the output of the actual flip flop is the output of the required flip flop. The following flip flop conversions will be explained.

- **SR Flip Flop to JK Flip Flop**
- **JK Flip Flop to SR Flip Flop**
- **SR Flip Flop to D Flip Flop**
- **D Flip Flop to SR Flip Flop**
- **JK Flip Flop to T Flip Flop**
- **JK Flip Flop to D Flip Flop**
- **D Flip Flop to JK Flip Flop**

SR Flip Flop to JK Flip Flop

As told earlier, J and K will be given as external inputs to S and R. As shown in the logic diagram below, S and R will be the outputs of the combinational circuit.

The truth tables for the flip flop conversion are given below. The present state is represented by Q_p and Q_{p+1} is the next state to be obtained when the J and K inputs are applied.

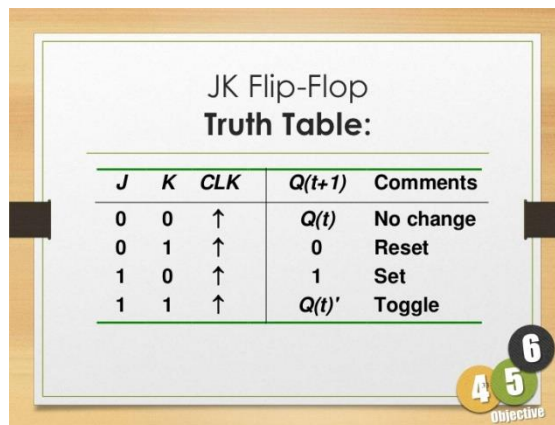
For two inputs J and K, there will be eight possible combinations. For each combination of J, K and Q_p , the corresponding Q_{p+1} states are found. Q_{p+1} simply suggests the future values to be obtained by the JK flip flop after the value of Q_p . The table is then completed by writing the values of S and R required getting each Q_{p+1} from the corresponding Q_p . That is, the values of S and R that are required to change the state of the flip flop from Q_p to Q_{p+1} are written.

PROCEDURE FOR CONVERSION

1. Draw the block diagram of the destination flip flop from the given problem.
2. Write truth table for the destination flip-flop.
3. Write excitation table for the source flip- flop.
4. Draw k-map for destination flip-flop.
5. Draw the block diagram.

SR to JK FF:

Truth Table/Characteristic table:



JK Flip-Flop
Truth Table:

J	K	CLK	$Q(t+1)$	Comments
0	0	↑	$Q(t)$	No change
0	1	↑	0	Reset
1	0	↑	1	Set
1	1	↑	$Q(t)'$	Toggle

Objective 4 5 6

Excitation table:-

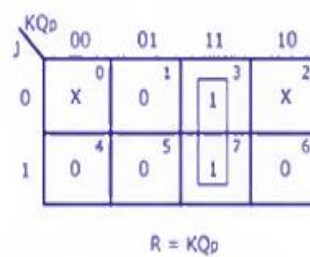
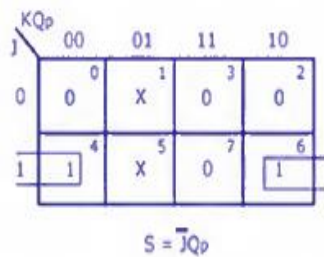
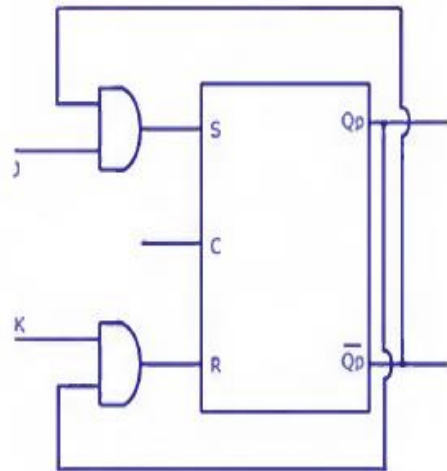
Q_p	Q_{p+1}	S Input	R input
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

S-R Flip Flop to J-K Flip Flop

Conversion Table

J-K Inputs		Outputs		S-R Inputs	
J	K	Q_p	Q_{p+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Logic Diagram



K-Map

JK Flip Flop to SR Flip Flop

This will be the reverse process of the above explained conversion. S and R will be the external inputs to J and K. As shown in the logic diagram below, J and K will be the outputs of the combinational circuit. Thus, the values of J and K have to be obtained in terms of S, R and Q_p . The logic diagram is shown below.

A conversion table is to be written using S, R, Q_p , Q_{p+1} , J and K. For two inputs, S and R, eight combinations are made. For each combination, the corresponding Q_{p+1} outputs are found out. The outputs for the combinations of $S=1$ and $R=1$ are not permitted for an SR flip flop. Thus the outputs are considered invalid and the J and K values are taken as “don’t cares”.

TT:

clock	S	R	Q	$\bar{Q}$	STATUS
↑	0	0	Q	$\bar{Q}$	HOLD (NoChange)
↑	0	1	0	1	RESET
↑	1	0	1	0	SET
↑	1	1	0	0	INVALID

Excitation table:

Present state of Q o/p	Next state of Q o/p	S _n Input	R _n input
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

J-K Flip Flop to S-R Flip Flop

Conversion Table

S-R Inputs		Outputs		J-K Inputs	
S	R	Q _p	Q _{p+1}	J	K
0	0	0	0	0	x
0	0	1	1	x	0
0	1	0	0	0	x
0	1	1	0	x	1
1	0	0	1	1	x
1	0	1	1	x	0
1	1	Invalid		Dont care	
1	1	Invalid		Dont care	

Logic Diagram

K-maps

J=S

S \ RQp	00	01	11	10
0	0 ⁰	x ¹	x ³	0 ²
1	1 ⁴	x ⁵	x ⁷	x ⁶

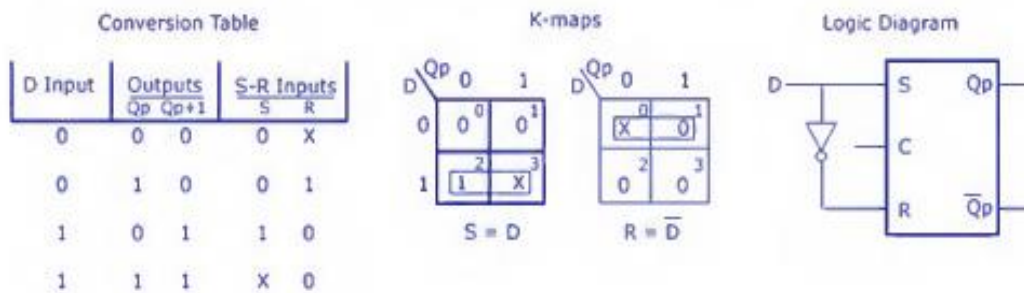
K=R

S \ RQp	00	01	11	10
0	x ⁰	0 ¹	1 ³	x ²
1	x ⁴	0 ⁵	x ⁷	x ⁶

SR Flip Flop to D Flip Flop

As shown in the figure, S and R are the actual inputs of the flip flop and D is the external input of the flip flop. The four combinations, the logic diagram, conversion table, and the K-map for S and R in terms of D and Qp are shown below.

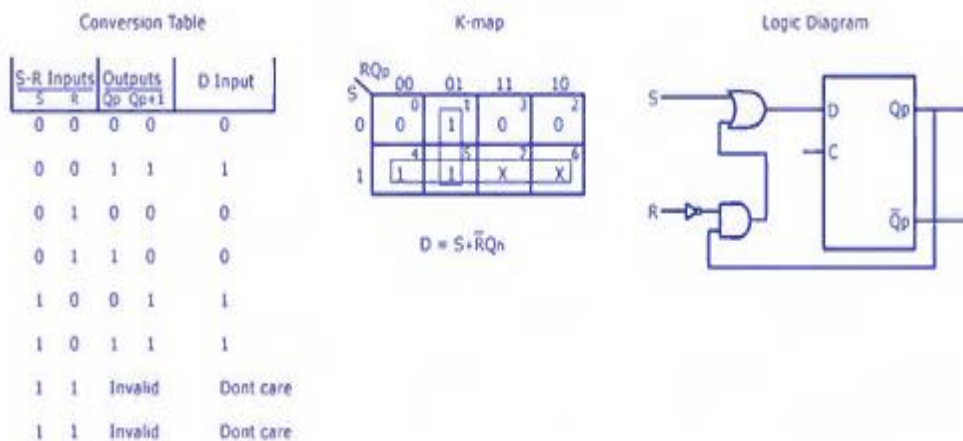
S-R Flip Flop to D Flip Flop



D Flip Flop to SR Flip Flop

D is the actual input of the flip flop and S and R are the external inputs. Eight possible combinations are achieved from the external inputs S, R and Qp. But, since the combination of S=1 and R=1 are invalid, the values of Qp+1 and D are considered as “don’t cares”. The logic diagram showing the conversion from D to SR, and the K-map for D in terms of S, R and Qp are shown below.

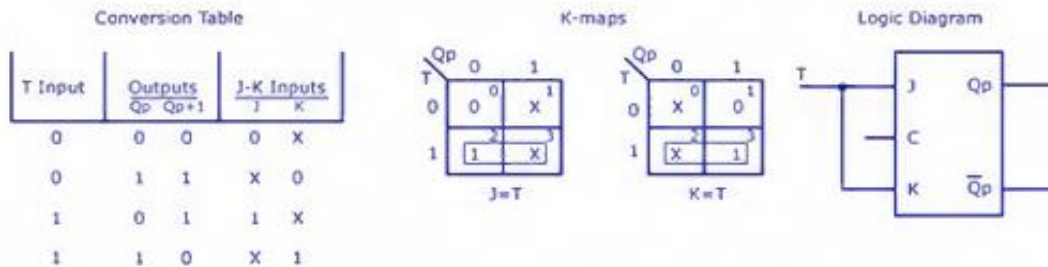
D Flip Flop to S-R Flip Flop



JK Flip Flop to T Flip Flop

J and K are the actual inputs of the flip flop and T is taken as the external input for conversion. Four combinations are produced with T and Q_p . J and K are expressed in terms of T and Q_p . The conversion table, K-maps, and the logic diagram are given below.

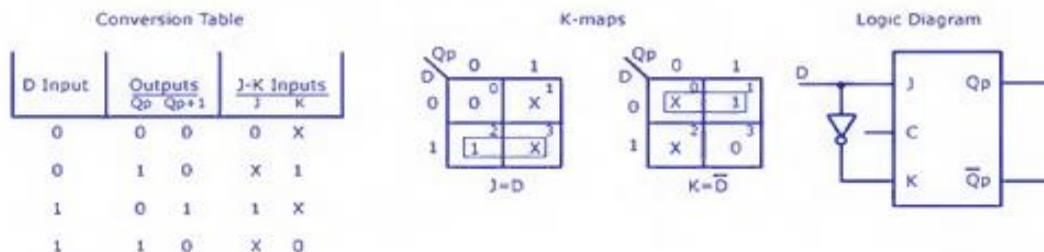
J-K Flip Flop to T Flip Flop



JK Flip Flop to D Flip Flop

D is the external input and J and K are the actual inputs of the flip flop. D and Q_p make four combinations. J and K are expressed in terms of D and Q_p . The four combination conversion table, the K-maps for J and K in terms of D and Q_p , and the logic diagram showing the conversion from JK to D are given below.

J-K Flip Flop to D Flip Flop

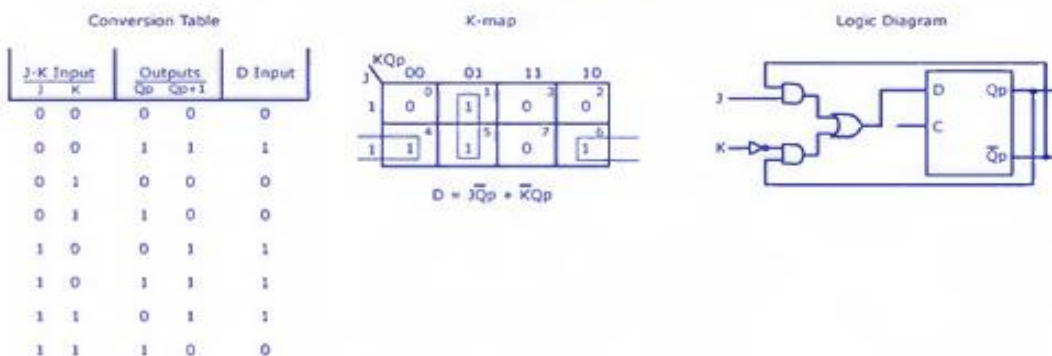


D Flip Flop to JK Flip Flop

In this conversion, D is the actual input to the flip flop and J and K are the external inputs. J, K and Q_p make eight possible combinations, as shown in the conversion table below. D is expressed in terms of J, K and Q_p .

The conversion table, the K-map for D in terms of J, K and Q_p and the logic diagram showing the conversion from D to JK are given in the figure below.

D Flip Flop to J-K Flip Flop



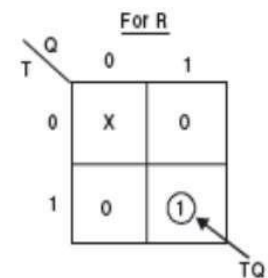
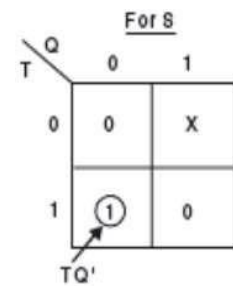
SR(Source) to T(Destination)FF:

SR(Source) to T(Destination)

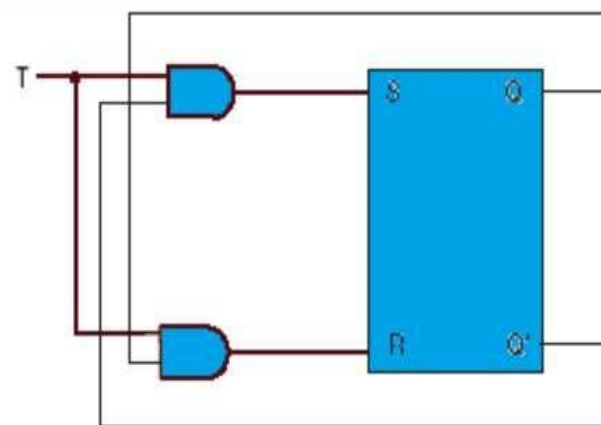
Conversion Table

Input	Present state	Next state	Flip flop Inputs	
T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

K- MAP
SIMPLIFICATION



Logic Diagram (SR to T)



A T flip-flop using S-R flip-flop.

D(Source) to T(Destination) Flip-Flop Conversion Table

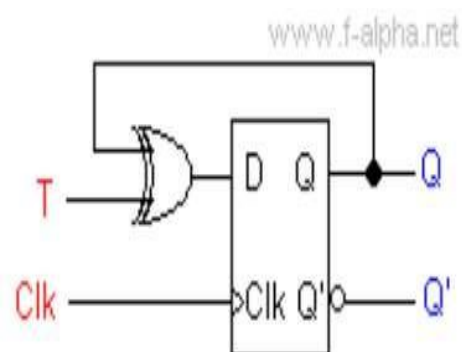
Input	Present state	Next state	Flipflop Inputs
T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

K-MAP SIMPLIFICATION

	Q_n	
	0	1
T		
0	0	1
1	1	0

$D = T'Q_n + TQ_n'$

Logic Diagram(D to T)



T (Source) to D(Destination) Flip-flop Conversion Table

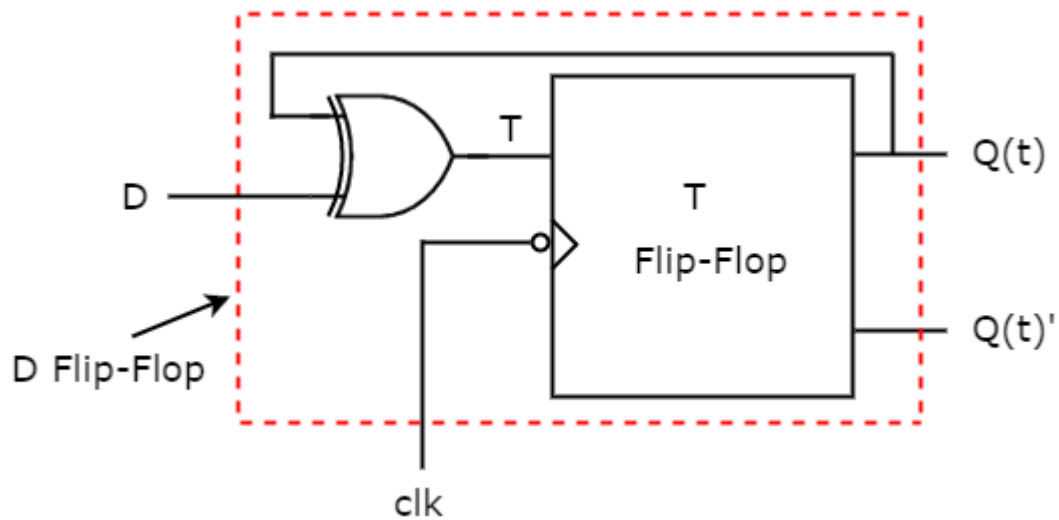
Input	Present state	Next state	Flip flop Inputs
D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

K- MAP SIMPLIFICATION

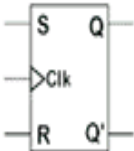
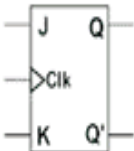
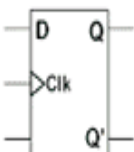
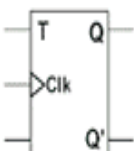
	Q_n	0	1
D	0	0	1
1	1	1	0

$$T = DQ_n' + D'Q_n$$

Logic Diagram:



Characteristic table and excitation table of FFs:

FLIP-FLOP NAME	FLIP-FLOP SYMBOL	CHARACTERISTIC TABLE	CHARACTERISTIC EQUATION	EXCITATION TABLE																																			
SR		<table><tr><th>S</th><th>R</th><th>$Q_{(next)}$</th></tr><tr><td>0</td><td>0</td><td>Q</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>?</td></tr></table>	S	R	$Q_{(next)}$	0	0	Q	0	1	0	1	0	1	1	1	?	$Q_{(next)} = S + R'Q$ $SR = 0$	<table><tr><th>Q</th><th>$Q_{(next)}$</th><th>S</th><th>R</th></tr><tr><td>0</td><td>0</td><td>0</td><td>X</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>X</td><td>0</td></tr></table>	Q	$Q_{(next)}$	S	R	0	0	0	X	0	1	1	0	1	0	0	1	1	1	X	0
S	R	$Q_{(next)}$																																					
0	0	Q																																					
0	1	0																																					
1	0	1																																					
1	1	?																																					
Q	$Q_{(next)}$	S	R																																				
0	0	0	X																																				
0	1	1	0																																				
1	0	0	1																																				
1	1	X	0																																				
JK		<table><tr><th>J</th><th>K</th><th>$Q_{(next)}$</th></tr><tr><td>0</td><td>0</td><td>Q</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>Q'</td></tr></table>	J	K	$Q_{(next)}$	0	0	Q	0	1	0	1	0	1	1	1	Q'	$Q_{(next)} = JQ' + K'Q$	<table><tr><th>Q</th><th>$Q_{(next)}$</th><th>J</th><th>K</th></tr><tr><td>0</td><td>0</td><td>0</td><td>X</td></tr><tr><td>0</td><td>1</td><td>1</td><td>X</td></tr><tr><td>1</td><td>0</td><td>X</td><td>1</td></tr><tr><td>1</td><td>1</td><td>X</td><td>0</td></tr></table>	Q	$Q_{(next)}$	J	K	0	0	0	X	0	1	1	X	1	0	X	1	1	1	X	0
J	K	$Q_{(next)}$																																					
0	0	Q																																					
0	1	0																																					
1	0	1																																					
1	1	Q'																																					
Q	$Q_{(next)}$	J	K																																				
0	0	0	X																																				
0	1	1	X																																				
1	0	X	1																																				
1	1	X	0																																				
D		<table><tr><th>D</th><th>$Q_{(next)}$</th></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table>	D	$Q_{(next)}$	0	0	1	1	$Q_{(next)} = D$	<table><tr><th>Q</th><th>$Q_{(next)}$</th><th>D</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	Q	$Q_{(next)}$	D	0	0	0	0	1	1	1	0	0	1	1	1														
D	$Q_{(next)}$																																						
0	0																																						
1	1																																						
Q	$Q_{(next)}$	D																																					
0	0	0																																					
0	1	1																																					
1	0	0																																					
1	1	1																																					
T		<table><tr><th>T</th><th>$Q_{(next)}$</th></tr><tr><td>0</td><td>Q</td></tr><tr><td>1</td><td>Q'</td></tr></table>	T	$Q_{(next)}$	0	Q	1	Q'	$Q_{(next)} = TQ' + T'Q$	<table><tr><th>Q</th><th>$Q_{(next)}$</th><th>T</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	Q	$Q_{(next)}$	T	0	0	0	0	1	1	1	0	1	1	1	0														
T	$Q_{(next)}$																																						
0	Q																																						
1	Q'																																						
Q	$Q_{(next)}$	T																																					
0	0	0																																					
0	1	1																																					
1	0	1																																					
1	1	0																																					

Synchronous Counters:

- **Synchronous Counters** can be made from Toggle or D-type flip-flops.
- Synchronous counters are easier to design than asynchronous counters.
- They are called synchronous counters because the clock input of the flip-flops are all clocked together at the same time with the same clock signal.
- Due to this common clock pulse all output states switch or change simultaneously. With all clock inputs wired together there is no inherent propagation delay.
- Synchronous counters are sometimes called parallel counters as the clock is fed in parallel to all flip-flops.
- The inherent memory circuit keeps track of the counters present state.
- The count sequence is controlled using logic gates.
- Overall faster operation may be achieved compared to Asynchronous counters.

2 bit synchronous counter:

Synchronous Counter Operation

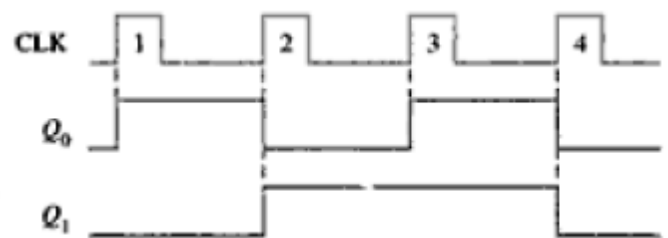
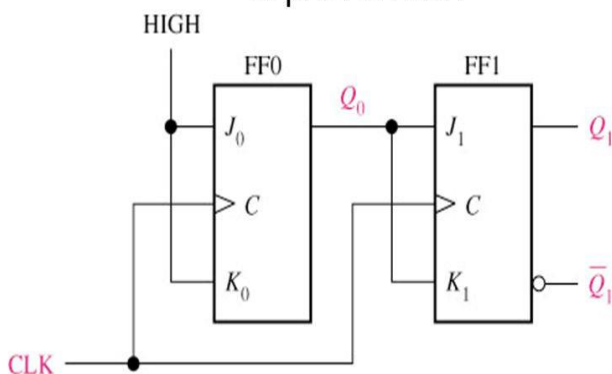
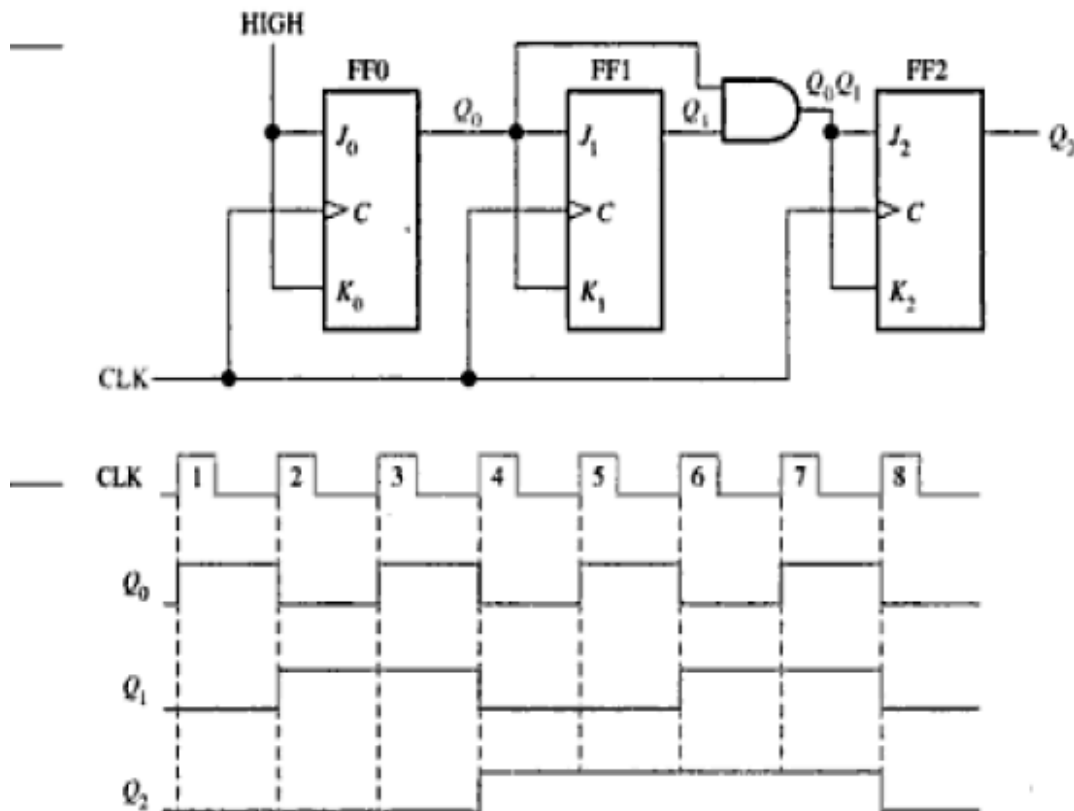


Figure 9--11 A 2-bit synchronous binary counter.

A 3-Bit Synchronous Binary Counter

A 3-bit synchronous binary counter is shown in Figure 8-14, and its timing diagram is shown in Figure 8-15. You can understand this counter operation by examining its sequence of states as shown in Table 8-3.

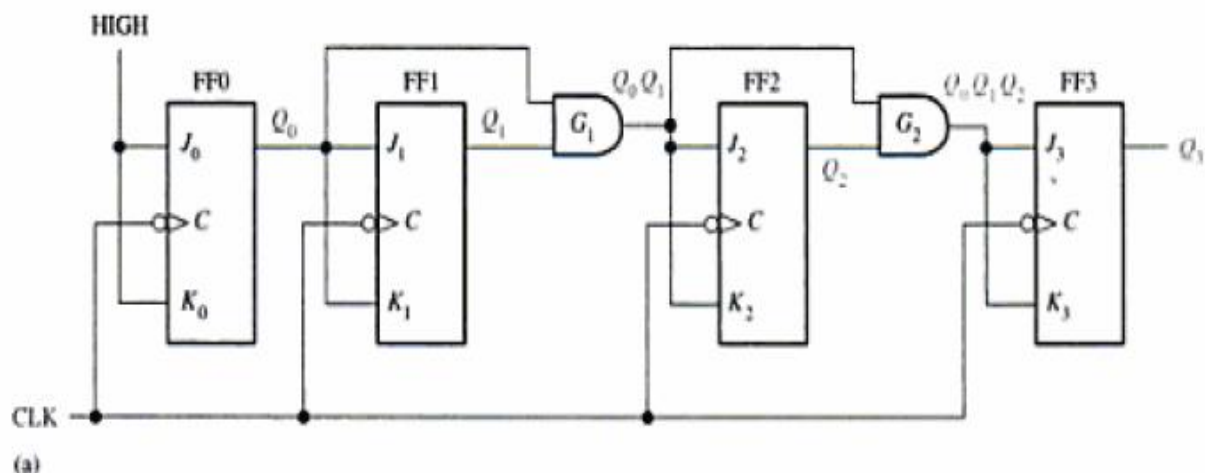


Sequence of States:

CLOCK PULSE	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

A 4-Bit Synchronous Binary Counter

Figure 8-16(a) shows a 4-bit synchronous binary counter, and Figure 8-16(b) shows its timing diagram. This particular counter is implemented with negative edge-triggered flip-flops. The reasoning behind the J and K input control for the first three flip-flops is the same as previously discussed for the 3-bit counter. The fourth stage, FF3, changes only twice in the sequence. Notice that both of these transitions occur following the times that Q_0 , Q_1 , and Q_2 are all HIGH. This condition is decoded by AND gate G_2 so that when a clock pulse occurs, FF3 will change state. For all other times the J_3 and K_3 inputs of FF3 are LOW, and it is in a no-change condition.



You can understand the counter operation by examining the sequence of states in Table 8-4 and by following the implementation in Figure 8-17. First, notice that FF0 (Q_0) toggles on each clock pulse, so the logic equation for its J_0 and K_0 inputs is

$$J_0 = K_0 = 1$$

This equation is implemented by connecting J_0 and K_0 to a constant HIGH level.

Next, notice in Table 8-4 that FF1 (Q_1) changes on the next clock pulse each time $Q_0 = 1$ and $Q_3 = 0$, so the logic equation for the J_1 and K_1 inputs is

$$J_1 = K_1 = Q_0 \bar{Q}_3$$

This equation is implemented by ANDing Q_0 and $\bar{Q}_3$ and connecting the gate output to the J_1 and K_1 inputs of FF1.

► TABLE 8-4

CLOCK PULSE	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (recycles)	0	0	0	0

Flip-flop 2 (Q_2) changes on the next clock pulse each time both $Q_0 = 1$ and $Q_1 = 1$. This requires an input logic equation as follows:

$$J_2 = K_2 = Q_0 Q_1$$

This equation is implemented by ANDing Q_0 and Q_1 and connecting the gate output to the J_2 and K_2 inputs of FF2.

Finally, FF3 (Q_3) changes to the opposite state on the next clock pulse each time $Q_0 = 1$, $Q_1 = 1$, and $Q_2 = 1$ (state 7), or when $Q_0 = 1$ and $Q_3 = 1$ (state 9). The equation for this is as follows:

$$J_3 = K_3 = Q_0 Q_1 Q_2 + Q_0 Q_3$$

This function is implemented with the AND/OR logic connected to the J_3 and K_3 inputs of FF3 as shown in the logic diagram in Figure 8-17. Notice that the differences between this decade counter and the modulus-16 binary counter in Figure 8-16 are the $Q_0 \bar{Q}_3$ AND gate, the $Q_0 Q_3$ AND gate, and the OR gate; this arrangement detects the occurrence of the 1001 state and causes the counter to recycle properly on the next clock pulse.

A 4-Bit Synchronous Binary Counter

The 74HC163 is an example of an integrated circuit 4-bit synchronous binary counter. A logic symbol is shown in Figure 8-19 with pin numbers in parentheses. This counter has several features in addition to the basic functions previously discussed for the general synchronous binary counter.

First, the counter can be synchronously preset to any 4-bit binary number by applying the proper levels to the parallel data inputs. When a LOW is applied to the $\overline{LOAD}$ input, the counter will assume the state of the data inputs on the next clock pulse. Thus, the counter sequence can be started with any 4-bit binary number.

Also, there is an active-LOW clear input ($\overline{CLR}$), which synchronously resets all four flip-flops in the counter. There are two enable inputs, $\overline{ENT}$ and $\overline{ENP}$. These inputs must both be HIGH for the counter to sequence through its binary states. When at least one input is LOW, the counter is disabled. The ripple clock output (RCO) goes HIGH when the counter reaches a terminal count of fifteen ($TC = 15$). This output, in conjunction with the enable inputs, allows these counters to be cascaded for higher count sequences, as will be discussed later.

► FIGURE 8-19

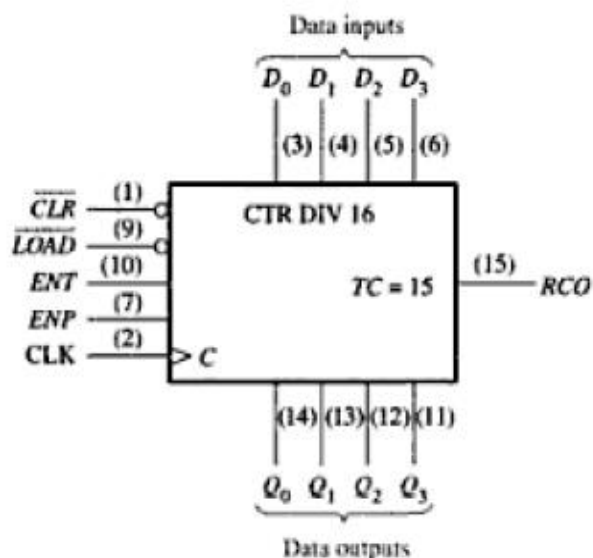
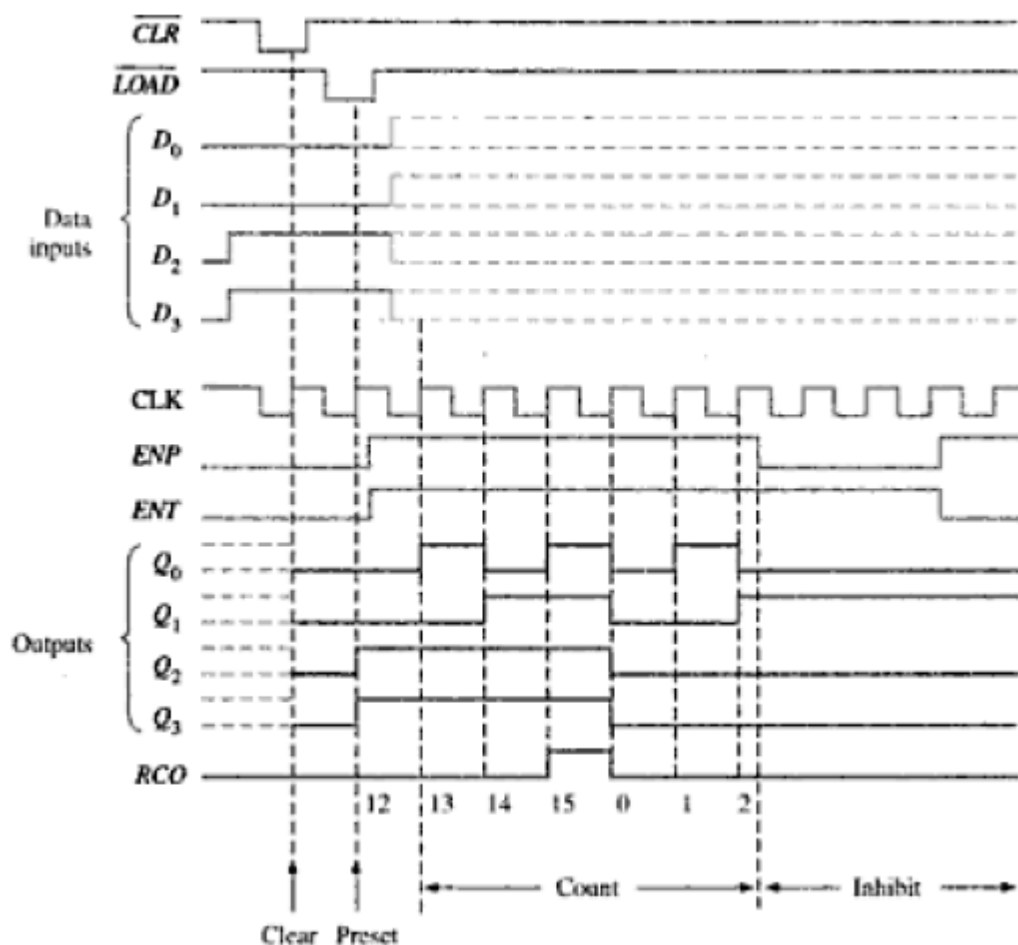


Figure 8-20 shows a timing diagram of this counter being preset to twelve (1100) and then counting up to its terminal count, fifteen (1111). Input D_0 is the least significant input bit, and Q_0 is the least significant output bit.

Let us examine this timing diagram in detail. This will aid you in interpreting timing diagrams found later in this chapter or on manufacturers' data sheets. To begin, the LOW level pulse on the $\overline{CLR}$ input causes all the outputs (Q_0 , Q_1 , Q_2 , and Q_3) to go LOW.

Next, the LOW level pulse on the $\overline{LOAD}$ input synchronously enters the data on the data inputs (D_0 , D_1 , D_2 , and D_3) into the counter. These data appear on the Q outputs at the time of the first positive-going clock edge after $\overline{LOAD}$ goes LOW. This is the preset operation. In this particular example, Q_0 is LOW, Q_1 is LOW, Q_2 is HIGH, and Q_3 is HIGH. This, of course, is a binary 12 (Q_0 is the LSB).

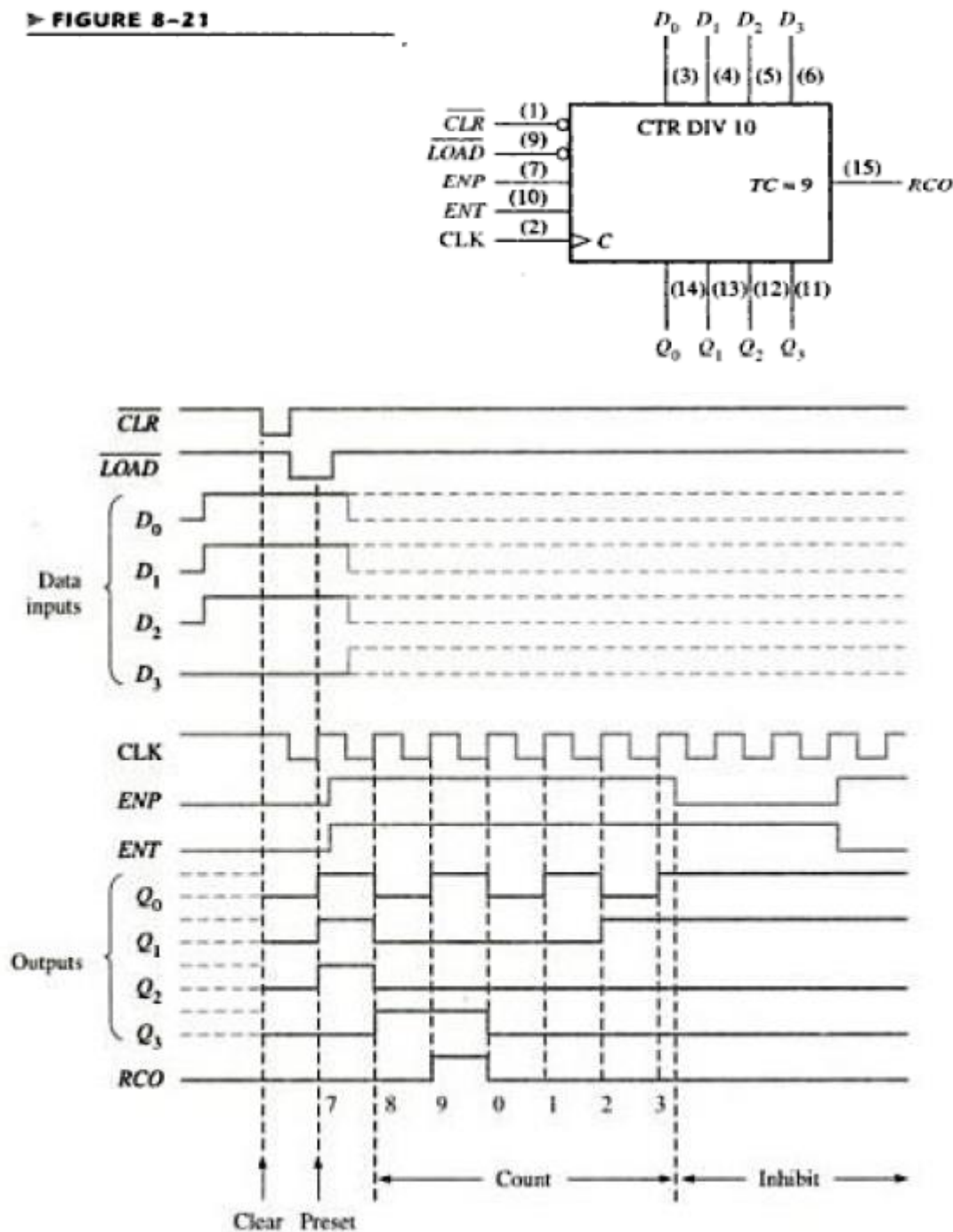
The counter now advances through states 13, 14, and 15 on the next three positive-going clock edges. It then recycles to 0, 1, 2 on the following clock pulses. Notice that both ENP and ENT inputs are HIGH during the state sequence. When ENP goes LOW, the counter is inhibited and remains in the binary 2 state.



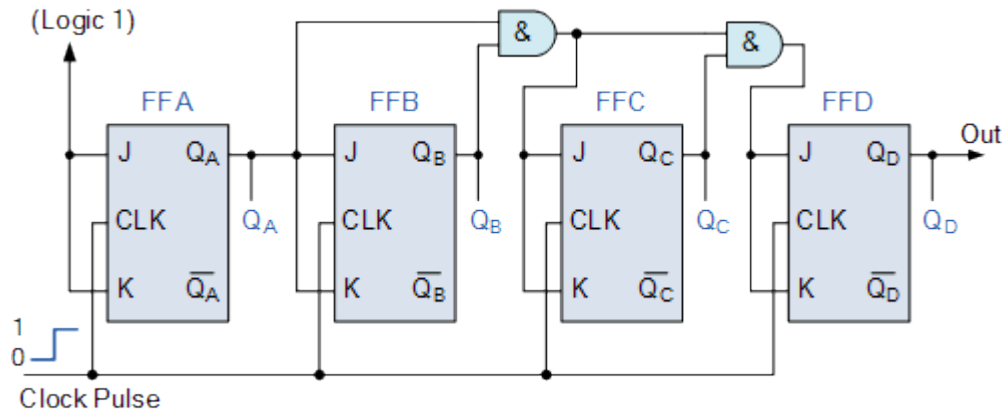
A Synchronous BCD Decade Counter

The 74LS160 is an example of a decade counter, which has the same inputs and outputs as the 74HC163 binary counter previously discussed. It can be preset to any BCD count by the use of the data inputs and a LOW on the $\overline{LOAD}$ input. A LOW on the asynchronous $\overline{CLR}$ will reset the counter. The enable inputs ENP and ENT must both be HIGH for the counter to advance through its sequence of states in response to a positive transition on the CLK input. As in the 74HC163, the enable inputs in conjunction with the ripple clock output RCO (terminal count of 1001) provide for cascading several decade counters. Figure 8-21 shows the logic symbol for the 74LS160 counter, and Figure 8-22 is a timing diagram showing the counter being preset to count 7 (0111). Cascaded counters will be discussed in Section 8-5.

► FIGURE 8-21



Binary 4-bit Synchronous Up Counter:



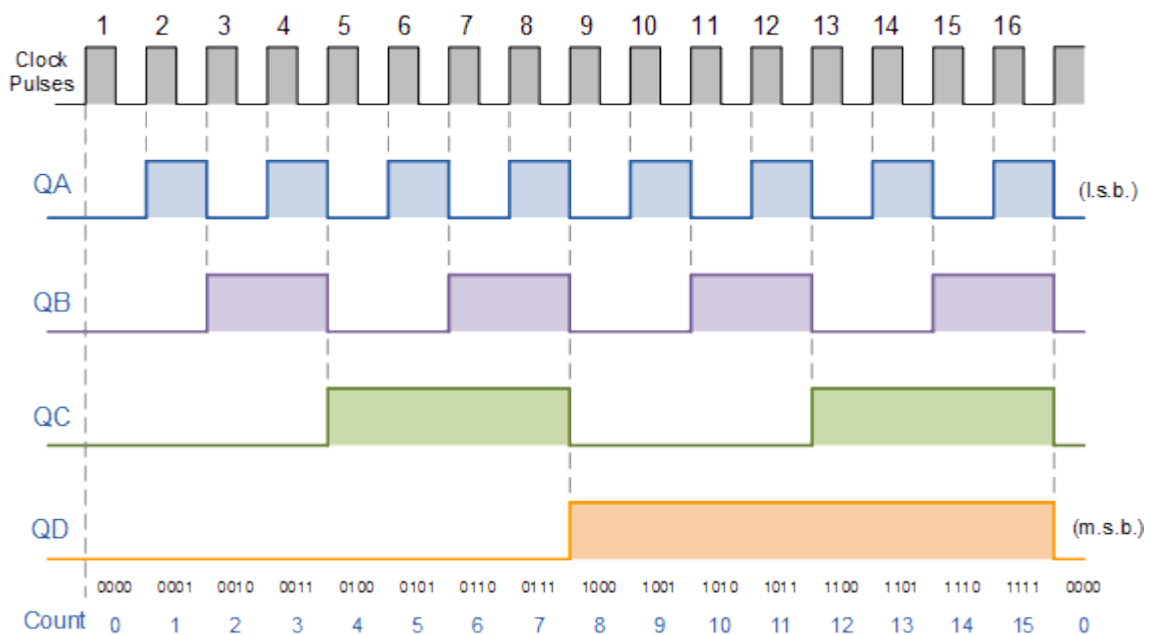
It can be seen above, that the external clock pulses (pulses to be counted) are fed directly to each of the **J-K flip-flops** in the counter chain and that both the J and K inputs are all tied together in toggle mode, but only in the first flip-flop, flip-flop FFA (LSB) are they connected HIGH, logic "1" allowing the flip-flop to toggle on every clock pulse. Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse.

The J and K inputs of flip-flop FFB are connected directly to the output Q_A of flip-flop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage. These additional AND gates generate the required logic for the JK inputs of the next stage.

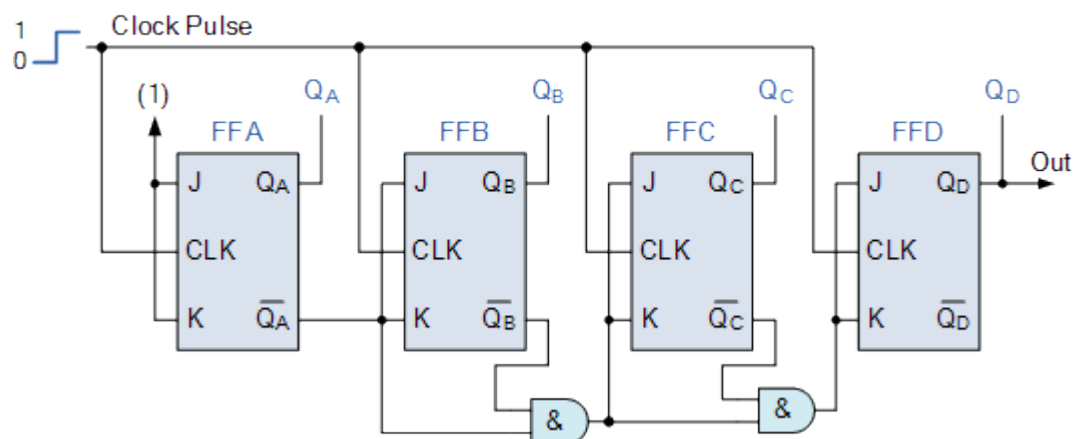
If we enable each JK flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are "HIGH" we can obtain the same counting sequence as with the asynchronous circuit but without the ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time.

Then as there is no inherent propagation delay in synchronous counters, because all the counter stages are triggered in parallel at the same time, the maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit.

4-bit Synchronous Counter Waveform Timing Diagram

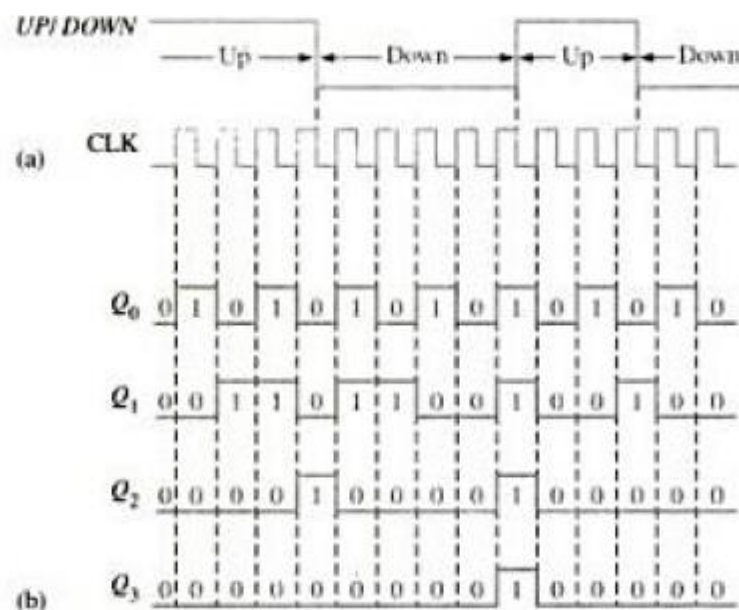


Binary 4-bit Synchronous Down Counter



As synchronous counters are formed by connecting flip-flops together and any number of flip-flops can be connected or “cascaded” together to form a “divide-by- n ” binary counter, the modulo’s or “MOD” number still applies as it does for asynchronous counters so a Decade counter or BCD counter with counts from 0 to 2^n-1 can be built along with truncated sequences. All we need to increase the MOD count of an up or down synchronous counter is an additional flip-flop and AND gate across it.

Show the timing diagram and determine the sequence of a 4-bit synchronous binary up/down counter if the clock and *UP/DOWN* control inputs have waveforms as shown in Figure 8–24(a). The counter starts in the all 0s state and is positive edge-triggered.



▲ FIGURE 8–24

The timing diagram showing the Q outputs is shown in Figure 8–24(b). From these waveforms, the counter sequence is as shown in Table 8–6.

► TABLE 8–6

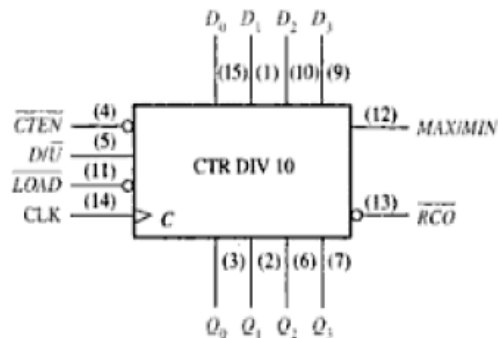
Q_3	Q_2	Q_1	Q_0	
0	0	0	0	UP
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	DOWN
0	0	1	1	
0	0	1	0	
0	0	0	1	
0	0	0	0	UP
1	1	1	1	
0	0	0	0	
0	0	0	1	
0	0	1	0	DOWN
0	0	0	1	
0	0	0	0	
0	0	0	0	

UP/DOWN COUNTER USING IC 74HC190:

AN UP/DOWN DECADE COUNTER

Figure 8–25 shows a logic diagram for the 74HC190, an example of an integrated circuit up/down synchronous counter. The direction of the count is determined by the level of the up/down input ($D/\bar{U}$). When this input is HIGH, the counter counts down; when it is LOW, the counter counts up. Also, this device can be preset to any desired BCD digit as determined by the states of the data inputs when the $\overline{LOAD}$ input is LOW.

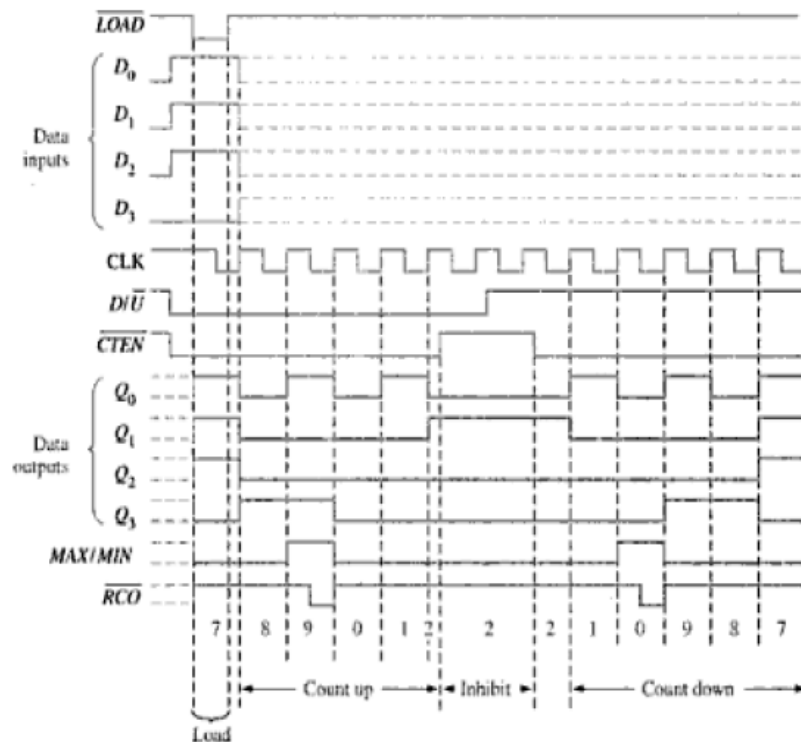
► FIGURE 8–25



The MAX/MIN output produces a HIGH pulse when the terminal count nine (1001) is reached in the UP mode or when the terminal count zero (0000) is reached in the DOWN mode. This MAX/MIN output, along with the ripple clock output ($\overline{RCO}$) and the count enable input ($\overline{CTEN}$), is used when cascading counters. (Cascaded counters are discussed in Section 8–5.)

Figure 8–26 is an example timing diagram that shows the 74HC190 counter preset to seven (0111) and then going through a count-up sequence followed by a count-down sequence. The MAX/MIN output is HIGH when the counter is in either the all-0s state (MIN) or the 1001 state (MAX).

► FIGURE 8–26



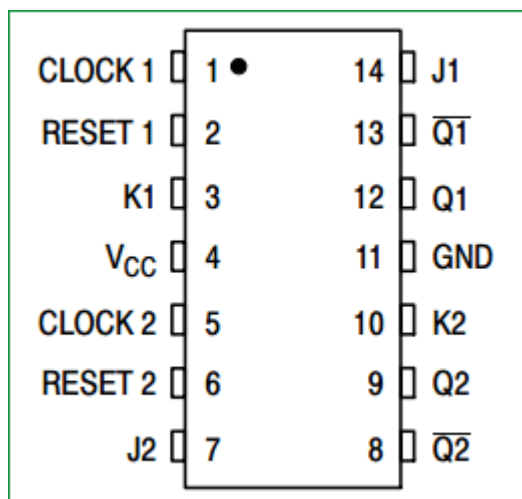
Applications of Counters:

Some of the applications of counters in a sequential circuits are as follows:

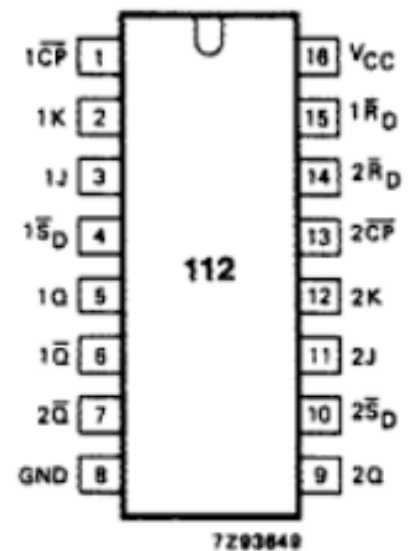
- To count the number of occurrences
- Generating Timing sequences
- Count up or down
- Increment or decrement count
- Sequence events
- Divide frequency
- Address memory
- As temporary memory

Flip Flop ICs:

Pin Diagram of IC MC74HC73A-JK FF



74HC112-DUAL JK FF:

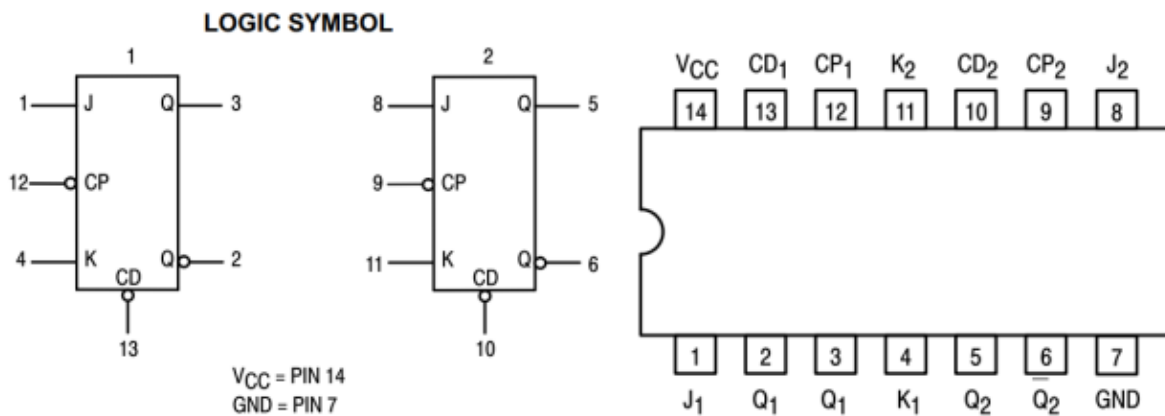


IC7474-JK FF:

Learn about D Flip-Flop IC 7474. Draw truth table for the output Q and Q'. Consider all inputs including PRESET and CLEAR.

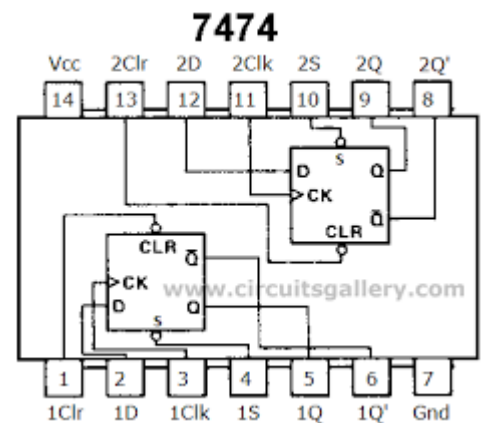
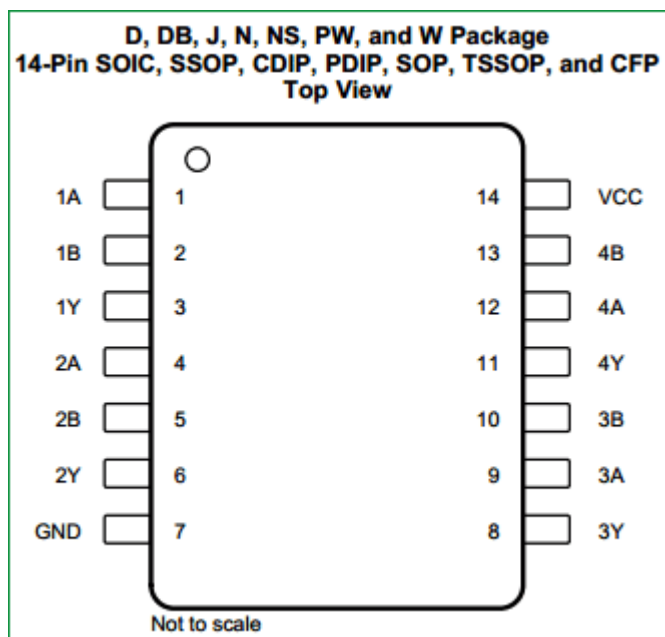
Question 2: JK-FF

Below are the logic symbol and IC diagram of the JK-FF.



SR FF IC-74HC00N

7474-D FF



DECADE COUNTERS

(BCD COUNTER OR MOD-10/ASYNCHRONOUS COUNTER)

A **decade counter** is one that counts in decimal digits, rather than binary. It counts from 0 to 9 and then resets to zero. The **counter** output can be set to zero by pulsing the reset line low. The **count** then increments on each clock pulse until it reaches 1001 (decimal 9).

Decade counter". A BCD counter can count 0000, 0001, 0010, 1000, 1001, 1010, 1011, 1110, 1111, 0000, and 0001 and so on.

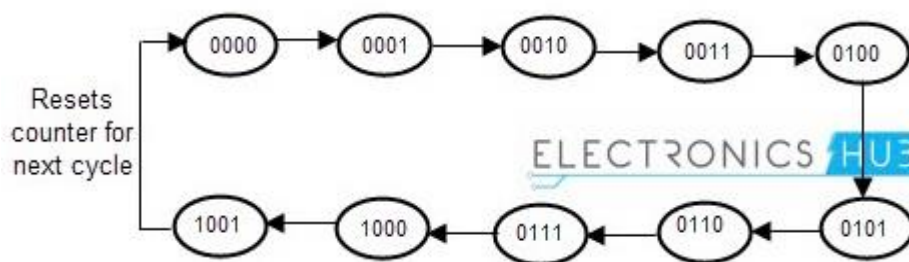
Decade Counter Operation:

When the Decade counter is at REST, the count is equal to 0000. This is first stage of the counter cycle. When we connect a clock signal input to the counter circuit, then the circuit will count the binary sequence. The first clock pulse can make the circuit to count up to 9 (1001). The next clock pulse advances to count 10 (1010).

Then the ports A and C will be high. As we know that for high inputs, the NAND gate output will be low. The NAND gate output is connected to clear input, so it resets all the flip flop stages in decade counter. This means the pulse after count 9 will again start the count from count 0.

State Diagram of Decade Counter

The state diagram of Decade counter is given below.



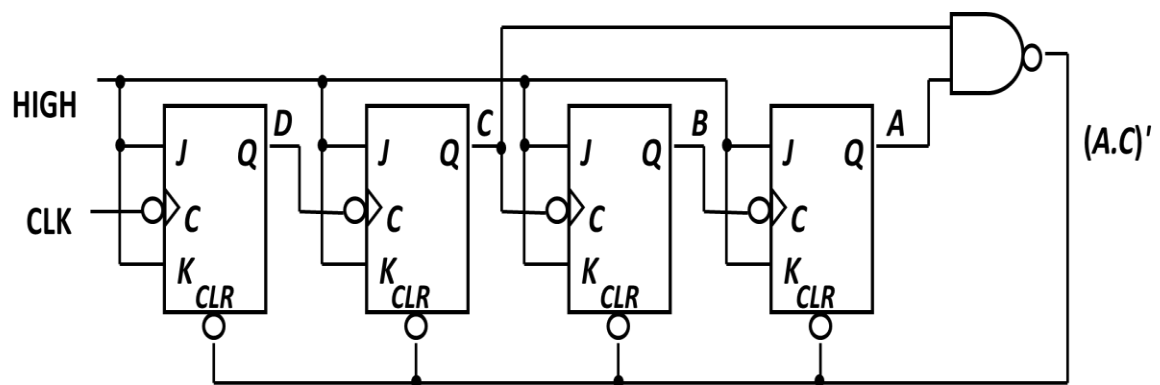
TRUTH TABLE:

Input Pulses	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
0	0	0	0	0 (resets)

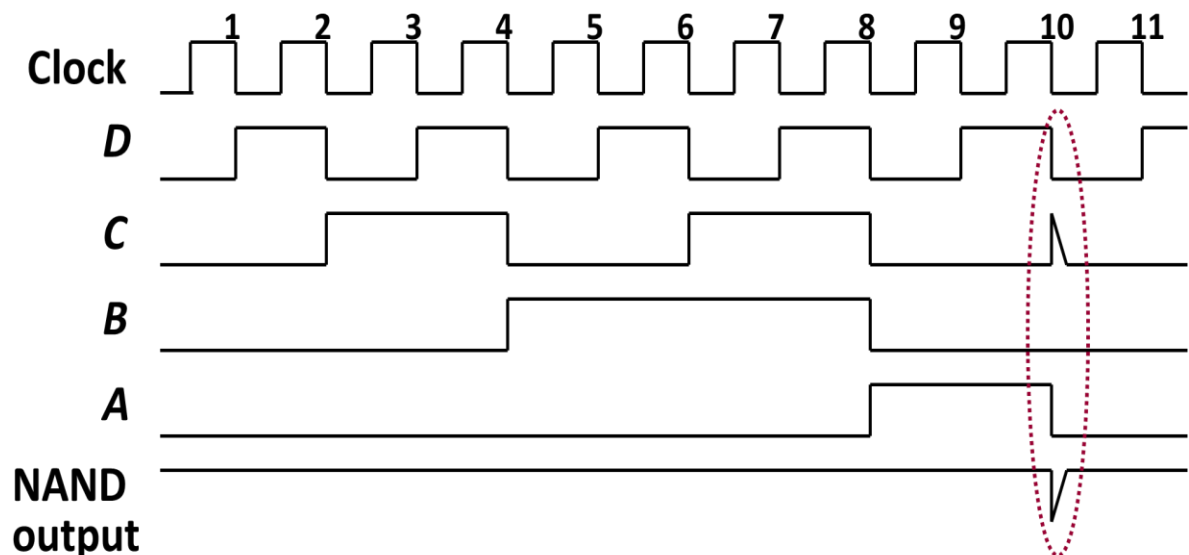
The above table describes the counting operation of Decade counter. It represents the count of circuit for decimal count of input pulses. The NAND gate output is zero when the count reaches 10 (1010).

The count is decoded by the inputs of NAND gate A and C. After count 10, the logic gate NAND will trigger its output from 1 to 0, and it resets all flip flops.

LOGIC DIAGRAM:



Timing Diagram:



IC 7490 is a 4-bit, ripple-type decade counter. It consists of four master/slave flip-flops, which are internally connected to form a divide-by-two section and a divide-by-five section.

Each section has a separate clock input to change the output states of the counter on a high-to-low clock transition.

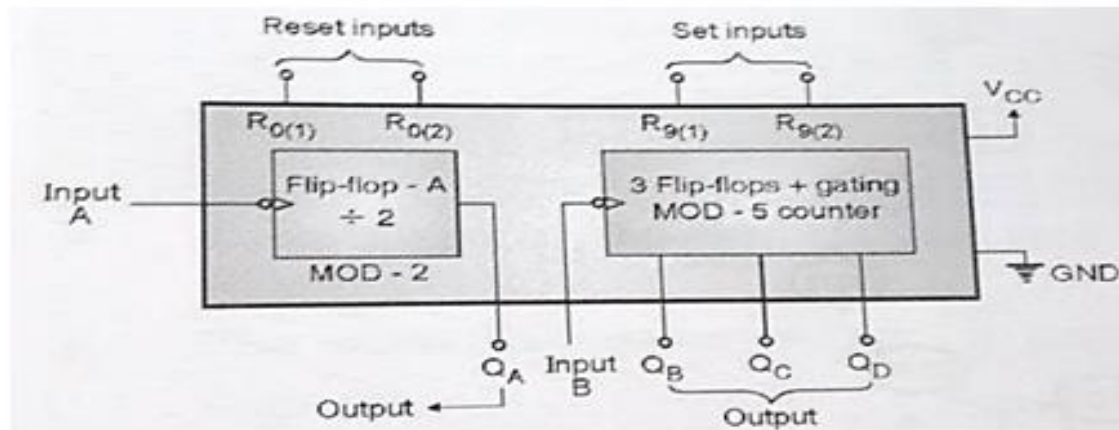
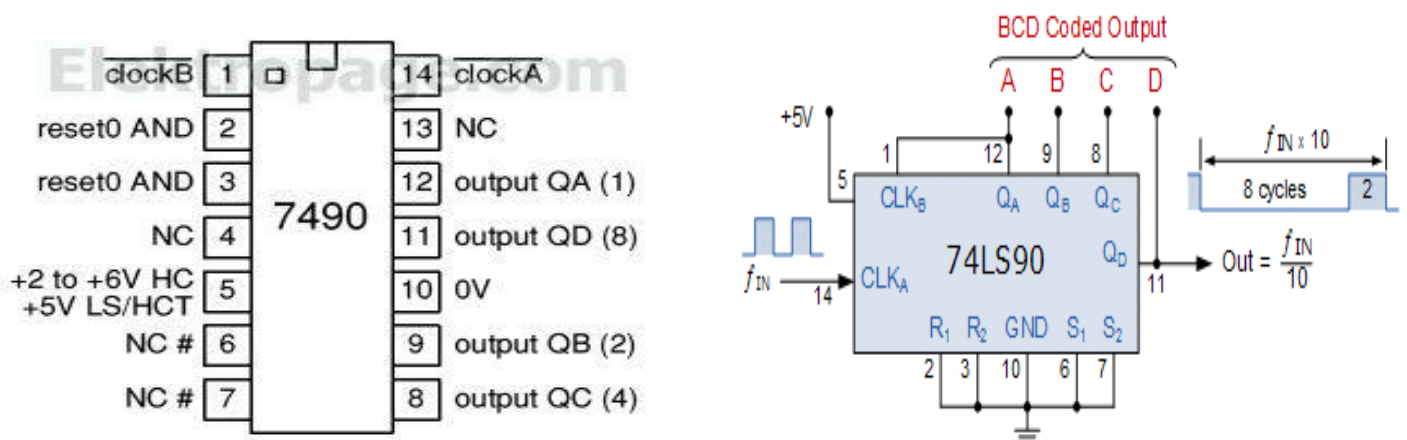


Fig10. The basic internal structure of IC 7490



Pin No	Function	Name
1	Clock input 2	Input2
2	Reset1	R1
3	Reset2	R2
4	Not connected	NC
5	Supply voltage; 5V (4.75V – 5.25V)	Vcc
6	Reset3	R3
7	Reset4	R4
8	Output 3, BCD Output bit 2	Q _C
9	Output 2, BCD Output bit 1	Q _B
10	Ground (0V)	Ground
11	Output 4, BCD Output bit 3	Q _D
12	Output 1, BCD Output bit 0	Q _A
13	Not connected	NC
14	Clock input 1	Input1

It is a simple counter which can count from 0 – 9. As it is a 4 bit binary decade counter, it has 4 output ports QA, QB, QC and QD. When the count reaches 10, the binary output is reset to 0 (0000), every time and another pulse starts at pin number 9. The Mod of the IC 7490 is set by changing the RESET pins R1, R2, R3, R4.

If any one of R1 & R2 is at high or R3 & R4 are at ground, the counter will reset all the outputs QA, QB, QC and QD to 0. If the pins R3 & R4 are high, then the count on QA, QB, QC and QD is 1001.

As we studied earlier, we can increase the counting capability of a Decade number by connecting more ICs in series; we can count 99 with two 7490 ICs connected in series. This 7490 IC has inbuilt Divide by 2 and Divide by 5 counters in it.

It can also be used as divide by 10 counter by connecting by connecting clock input 2 and QA and connecting all rest pins to ground and giving pulse input to 1. It is used as divide by 6 counter by supplying pulse at input 1 and grounding reset pins R3 and R4 and connecting QA with input 2. 7490 IC can work like bi –quinary counter, which is used to store decimal digits in the form of 4 bit binary numbers.

4017 CMOS decade counter IC description

Applications of BCD Counter or Decade Counters:

The key advantages and benefits of BCD counters are

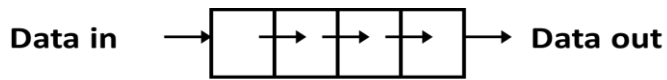
- Clock generation
- Clock division
- Integrated oscillator
- Low power CMOS
- TTL compatible inputs
- In frequency counting circuits

SHIFT REGISTERS

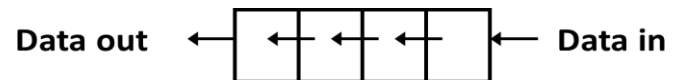
Shift Registers are devices that store and move data bits in serial (to the left or the right), Each *stage* (flip-flop) in a shift register represents one bit of storage, and the shifting capability of a register permits the movement of data from stage to stage within the register, or into or out of the register upon application of clock pulses.

- A simple **Shift Register** can be made using only D-type flip-Flops, one flip-Flop for each data bit.
- The output from each flip-Flop is connected to the D input of the flip-flop at its right.
- Shift registers hold the data in their memory which is moved or “shifted” to their required positions on each clock pulse.
- Each clock pulse shifts the contents of the register one bit position to either the left or the right.
- The data bits can be loaded one bit at a time in a series input (SI) configuration or be loaded simultaneously in a parallel configuration (PI).
- Data may be removed from the register one bit at a time for a series output (SO) or removed all at the same time from a parallel output (PO).
- One application of shift registers is in the conversion of data between serial and parallel, or parallel to serial.
- Shift registers are identified individually as SIPO, SISO, PISO, PIPO, or as a Universal Shift Register with all the functions combined within a single device.

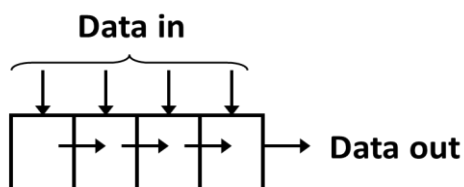
Basic data movement in shift registers (four bits are used for illustration).



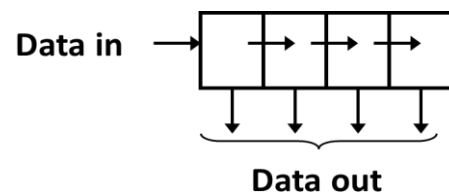
(a) Serial in/shift right/serial out



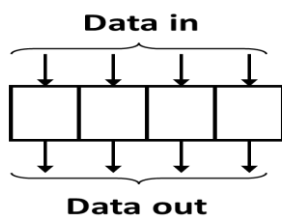
(b) Serial in/shift left/serial out



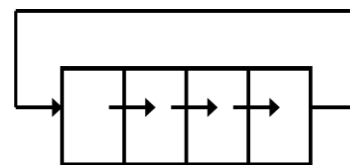
(c) Parallel in/serial out



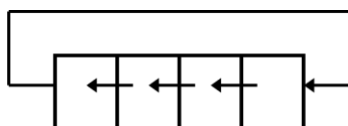
(d) Serial in/parallel out



(e) Parallel in / parallel out



(f) Rotate right



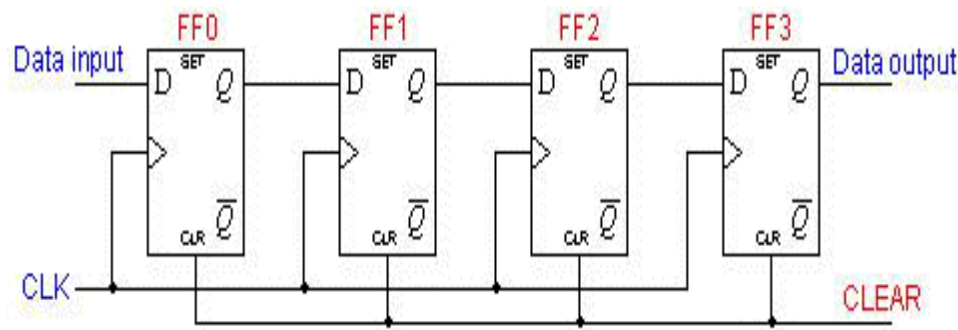
(g) Rotate left

Types of Shift Registers:

- SISO: Serial In, Serial Out
- SIPO: Serial In, Parallel Out
- PISO: Parallel In, Serial Out
- PIPO: Parallel In, Parallel Out

Serial In/Serial Out Shift Registers:

The serial in/serial out shift register accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.



A basic four-bit shift register can be constructed using four D flip-flops, as shown in Figure

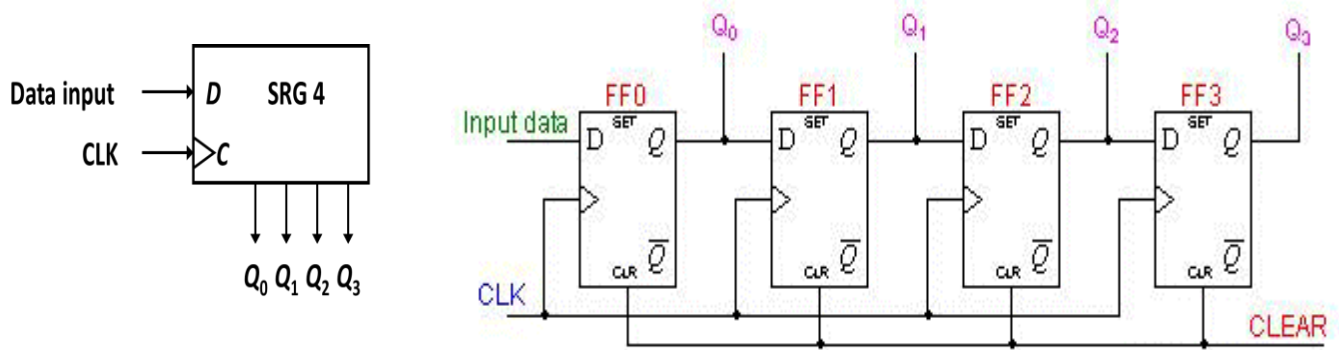
The operation of the circuit is as follows.

- The register is first cleared, forcing all four outputs to zero.
- The input data is then applied sequentially to the D input of the first flip-flop on the left (FF0).
- During each clock pulse, one bit is transmitted from left to right.
- Assume a data word to be 1001.
- The least significant bit of the data has to be shifted through the register from FF0 to FF3.

Timing Pulse	Shift register A	Shift register B	Serial output of B
Initial value	1 0 1 1	0 0 1 0	0
After T_1	1 1 0 1	1 0 0 1	1
After T_2	1 1 1 0	1 1 0 0	0
After T_3	0 1 1 1	0 1 1 0	0
After T_4	1 0 1 1	1 0 1 1	1

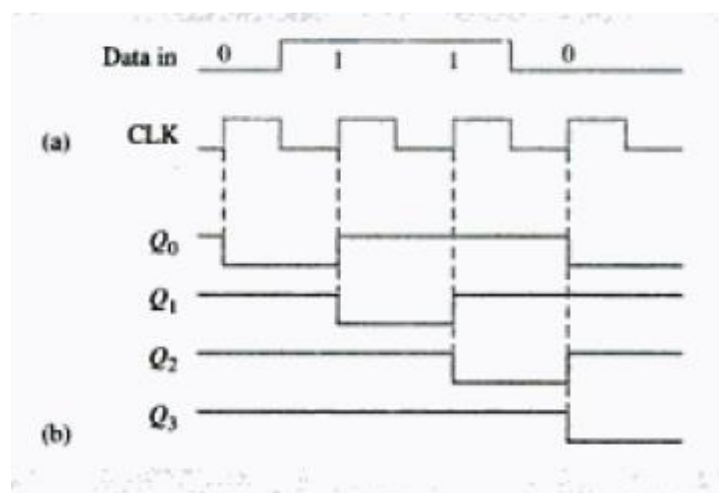
Serial In/Parallel Out Shift Registers

Data bits are entered serially in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. A construction of a four-bit serial in - parallel out register is shown below.



In the table below, we can see how the four-bit binary number 1001 is shifted to the Q outputs of the register.

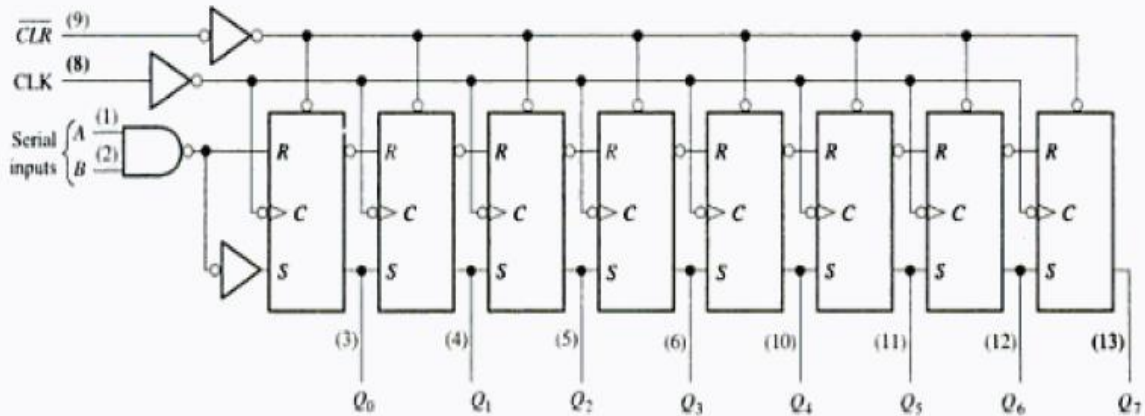
Clear	FF0	FF1	FF2	FF3
1001	0	0	0	0
	1	0	0	0
	0	1	0	0
	0	0	1	0
	1	0	0	1



AN 8-BIT SERIAL IN/PARALLEL OUT SHIFT REGISTER

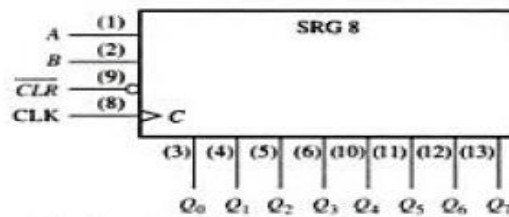
The 74HC164 is an example of an IC shift register having serial in/parallel out operation. The logic diagram is shown in Figure 9-10(a), and a typical logic block symbol is shown in part (b). Notice that this device has two gated serial inputs, A and B , and a clear ($\overline{CLR}$) input that is active-LOW. The parallel outputs are Q_0 through Q_7 .

A sample timing diagram for the 74HC164 is shown in Figure 9-11. Notice that the serial input data on input A are shifted into and through the register after input B goes HIGH.



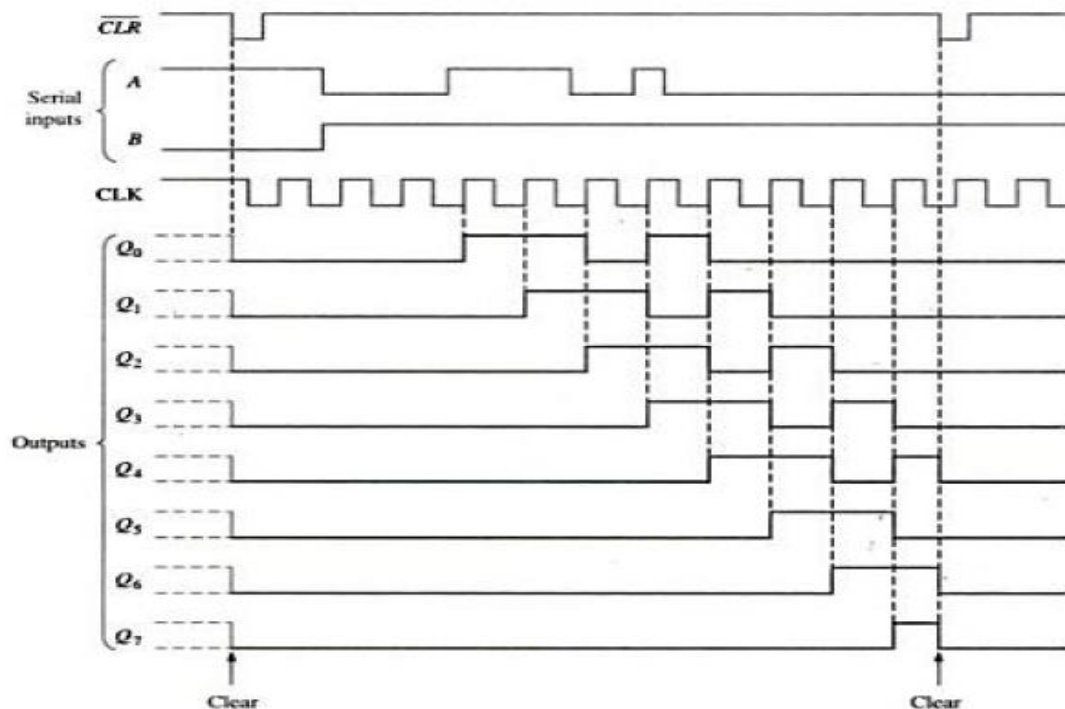
(a) Logic diagram

▲ FIGURE 9-10



(b) Logic symbol

▲ FIGURE 9-10 (continued)

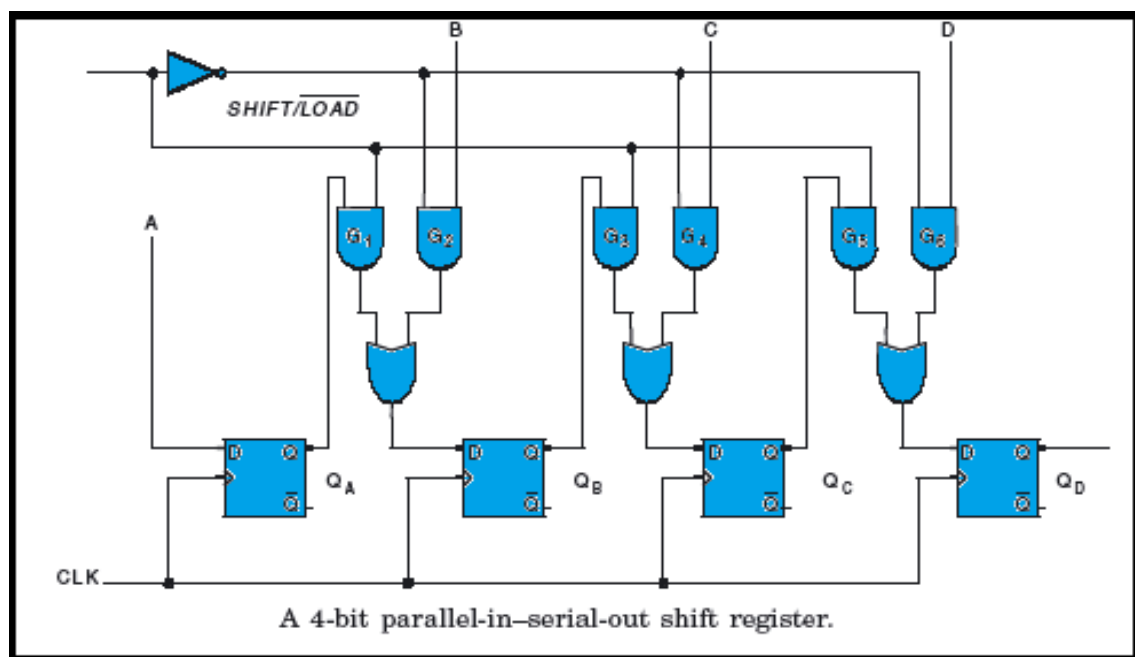
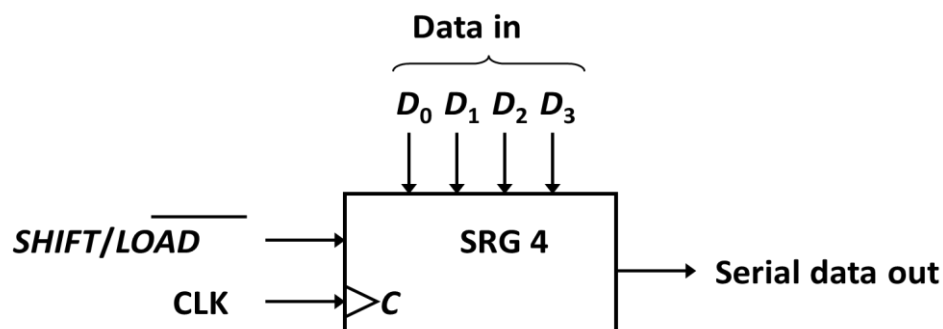


Parallel In/Serial Out Shift Registers

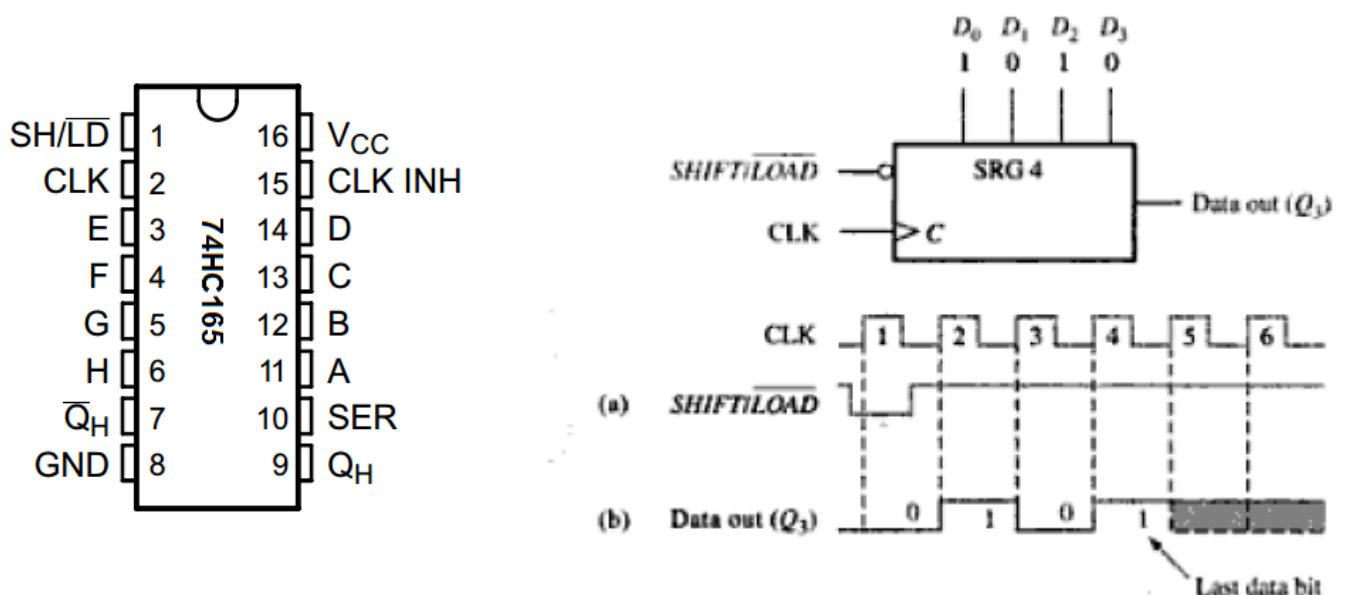
A four-bit parallel in - serial out shift register is shown below. The circuit uses D flip-flops and AND gates for entering data (ie writing) to the register.

The parallel-in/ serial-out shift register stores data, shifts it on a clock by clock basis, and delays it by the number of stages times the clock period.

In addition, parallel-in/ serial-out really means that we can load data in parallel into all stages before any shifting ever begins. This is a way to convert data from a *parallel* format to a *serial* format. By parallel format we mean that the data bits are present simultaneously on individual wires, one for each data bit as shown below. By serial format we mean that the data bits are presented sequentially in time on a single wire or circuit as in the case of the “data out” on the block diagram below.



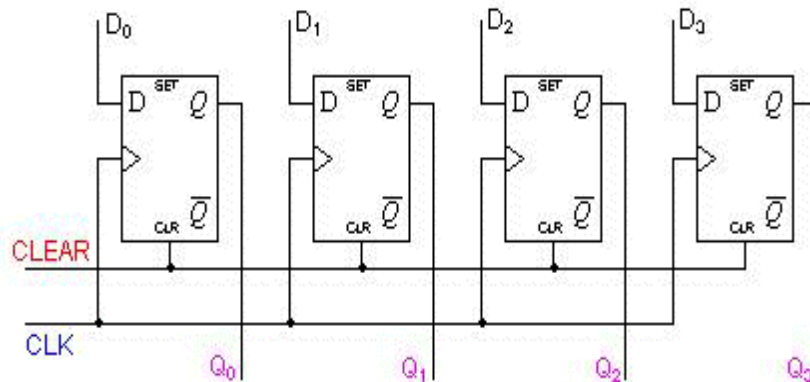
Now from above 4 bit parallel in serial out shift register we can see, A, B, C, and D are the four parallel data input lines and *SHIFT / LOAD* (*SH / LD*) is a control input that allows the four bits of data at A, B, C, and D inputs to enter into the register in parallel or shift the data in serial. When *SHIFT / LOAD* is HIGH, AND gates G1, G3, and G5 are enabled, allowing the data bits to shift right from one stage to the next. When *SHIFT / LOAD* is LOW, AND gates G2, G4, and G6 are enabled, allowing the data bits at the parallel inputs. When a clock pulse is applied, the flip-flops with D = 1 will be set and the flip-flops with D = 0 will be reset, thereby storing all the four bits simultaneously. The OR gates allow either the normal shifting operation or the parallel data-entry operation, depending on which of the AND gates are enabled by the level on the *SHIFT / LOAD* input.



- 74HC595 is a shift register which works on PArallel In and Serial OUT Protocol.
- It has 8 input pins where you can connect different sensors etc. and then it has 1 Serial Output Pin, which should be connected to the Microcontroller.
- With the help of Clock Pin, we can receive all these parallel 8 inputs serially from a single output into the microcontroller.
- We can also connect multiple 74HC165 in parallel to increase the input pins.
- Let's say if I have connected 3 shift registers in parallel then the input pins will increase by $8 \times 3 = 24$.
- So, we can control 24 digital sensors by a single Arduino Pin.
- Let's have a look at the 74HC595 Pinout:

Parallel In - Parallel Out Shift Registers

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by D flip-flops.

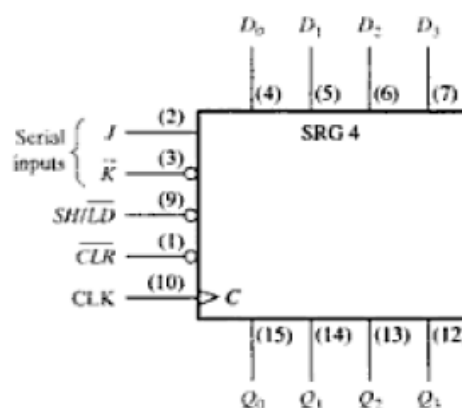


The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously.

A 4-BIT PARALLEL-ACCESS SHIFT REGISTER

The 74HC195 can be used for parallel in/parallel out operation. Because it also has a serial input, it can be used for serial in/serial out and serial in/parallel out operations. It can be used for parallel in/serial out operation by using Q₃ as the output. A typical logic block symbol is shown in Figure 9-17.

► FIGURE 9-17

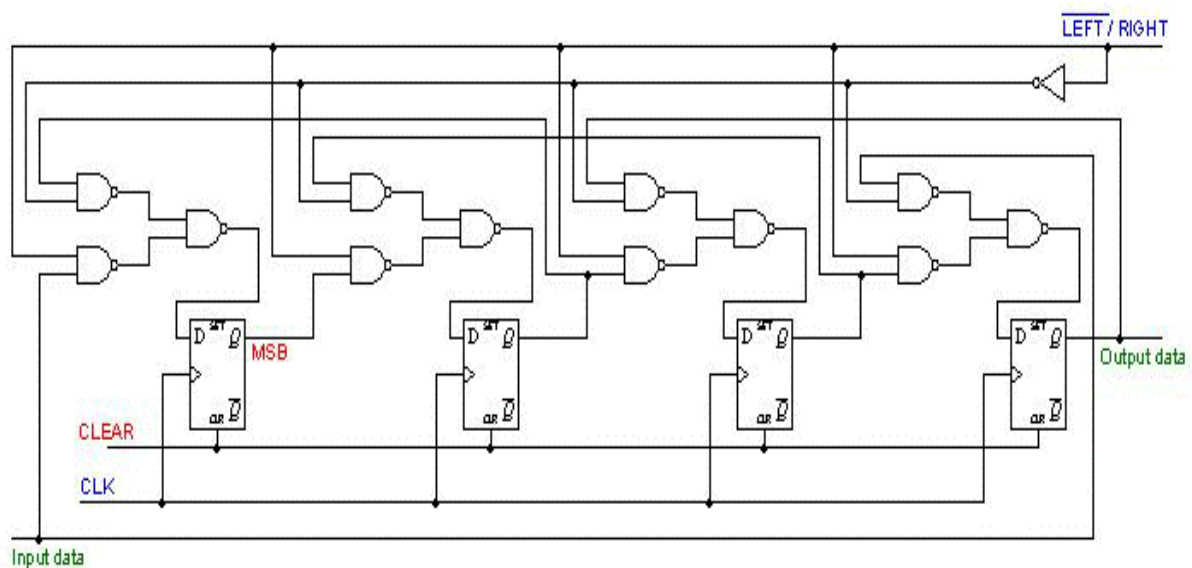


When the *SHIFT/LOAD* input (*SH/LD*) is LOW, the data on the parallel inputs are entered synchronously on the positive transition of the clock. When *SH/LD* is HIGH, stored data will shift right (Q₀ to Q₃) synchronously with the clock. Inputs J and K are the serial data inputs to the first stage of the register (Q₀); Q₃ can be used for serial output data. The active-LOW clear input is asynchronous.

The timing diagram in Figure 9-18 illustrates the operation of this register.

Bidirectional Shift Registers:

Each right shift operation has the effect of successively dividing the binary number by two. If the operation is reversed (left shift), this has the effect of multiplying the number by two. With suitable gating arrangement a serial shift register can perform both operations. A bidirectional, or reversible, shift register is one in which the data can be shift either left or right. A four-bit bidirectional shift register using D flip-flops is shown below. Here a set of NAND gates are configured as OR gates to select data inputs from the right or left adjacent bistables, as selected by the LEFT/RIGHT control line.



A 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The 74HC194 is an example of a universal bidirectional shift register in integrated circuit form. A **universal shift register** has both serial and parallel input and output capabilities. A logic block symbol is shown in Figure 9-21, and a sample timing diagram is shown in Figure 9-22.

FIGURE 9-21

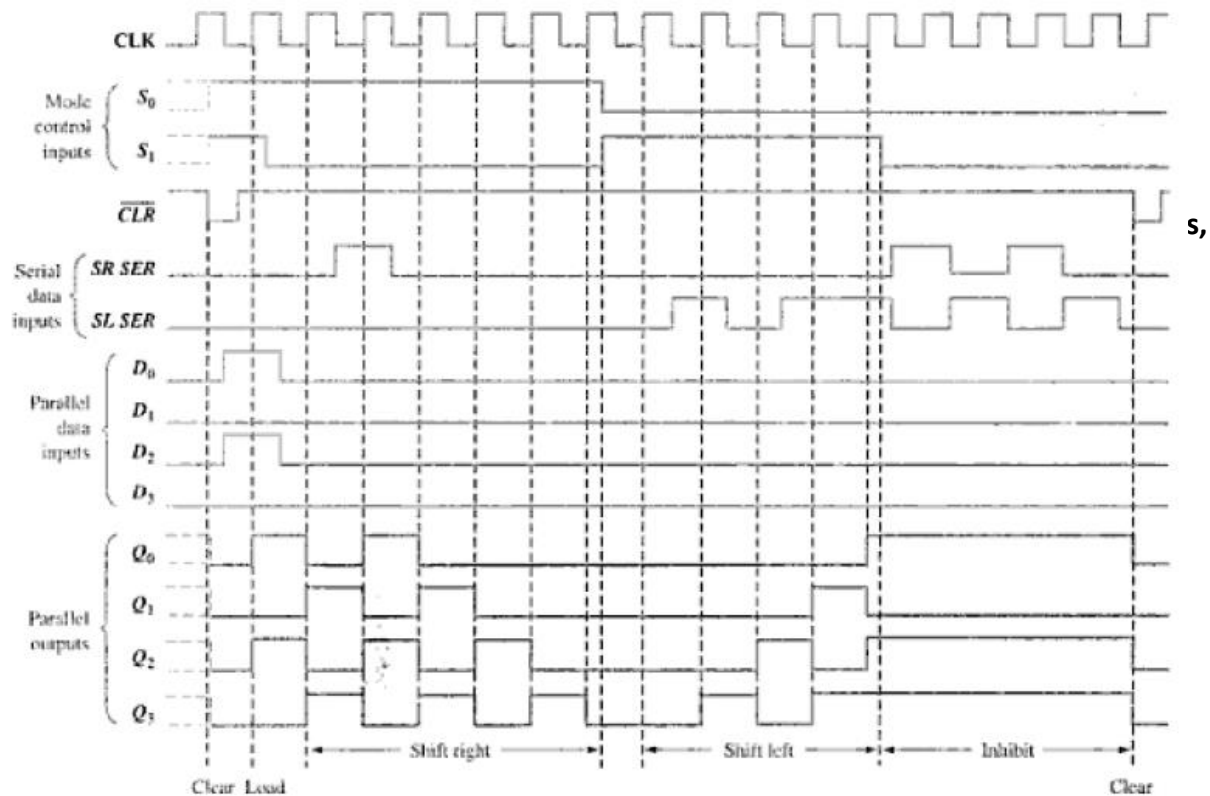
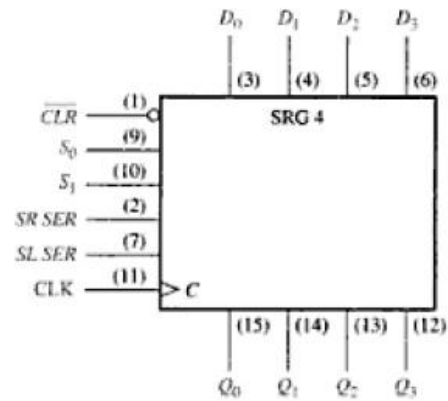


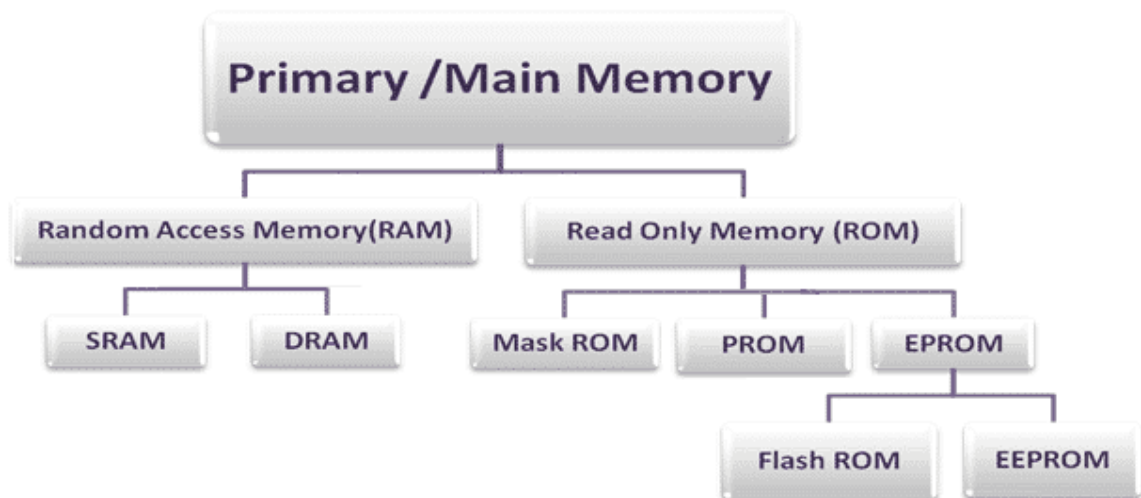
FIGURE 9-22

MEMORY

Memory is the portion of a system for storing binary data in large quantities. Semiconductor memories consist of arrays of storage elements that are generally either latches or capacitors. Units of Binary data: Bits, Bytes, Nibbles, and Words.

Units of Binary Data: Bits, Bytes, Nibbles, and Words

As a rule, memories store data in units that have from one to eight bits. The smallest unit of binary data, as you know, is the **bit**. In many applications, data are handled in an 8-bit unit called a **byte** or in multiples of 8-bit units. The byte can be split into two 4-bit units that are called **nibbles**. A complete unit of information is called a **word** and generally consists of one or more bytes. Some memories store data in 9-bit groups; a 9-bit group consists of a byte plus a parity bit.



Terms:

- Memory Cell – A device or an electrical circuit used to store a single bit (0 or 1)
- Memory Word – A group of bits in a memory (word sizes typically range from 4 to 64).
- Byte – a group of 8 bits
- Address – a number that identifies the location of a word in memory
- Read Operation – the operation whereby a word stored in a specified memory location is sensed and then transferred to another device.

- Write Operation – the operation whereby a new word is placed or stored into a particular memory location.
- Volatile Memory – any type of memory that requires the application of electrical power in order to store information. If the electrical power is removed, all information stored in the memory will be lost.

ROM Definition: Read Only Memory (ROM) is an integrated circuit which is pre-programmed with specific functional data at manufacturing time. It is an example of nonvolatile memory. It is a class of storage medium used in computers and other electronic devices. *Read Only Memory (ROM)*, also known as firmware, The instructions for starting the computer are housed on Read only memory chip.

Why Need ROM?

ROM chips are used not only in computers, but in most other electronic items as well. Because data is fully incorporated at the ROM chip's manufacture, data stored can neither be erased nor replaced. This means permanent and secure data storage. However, if a mistake is made in manufacture, a ROM chip becomes unusable. The most expensive stage of ROM manufacture, therefore, is creating the template.

If a template is readily available, duplicating the ROM chip is very easy and affordable. A ROM chip is also non volatile so data stored in it is not lost when power is turned off. ROM is a semiconductor memory that is capable of operating at electronics speed.

Difference between RAM and ROM

ROM can hold data permanently and RAM cannot. ROM chip is a non-volatile and RAM chip is volatile in nature.

Block Diagram of Memory:

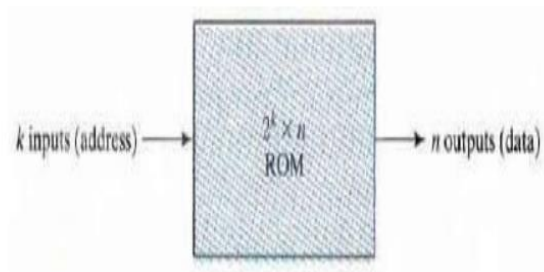
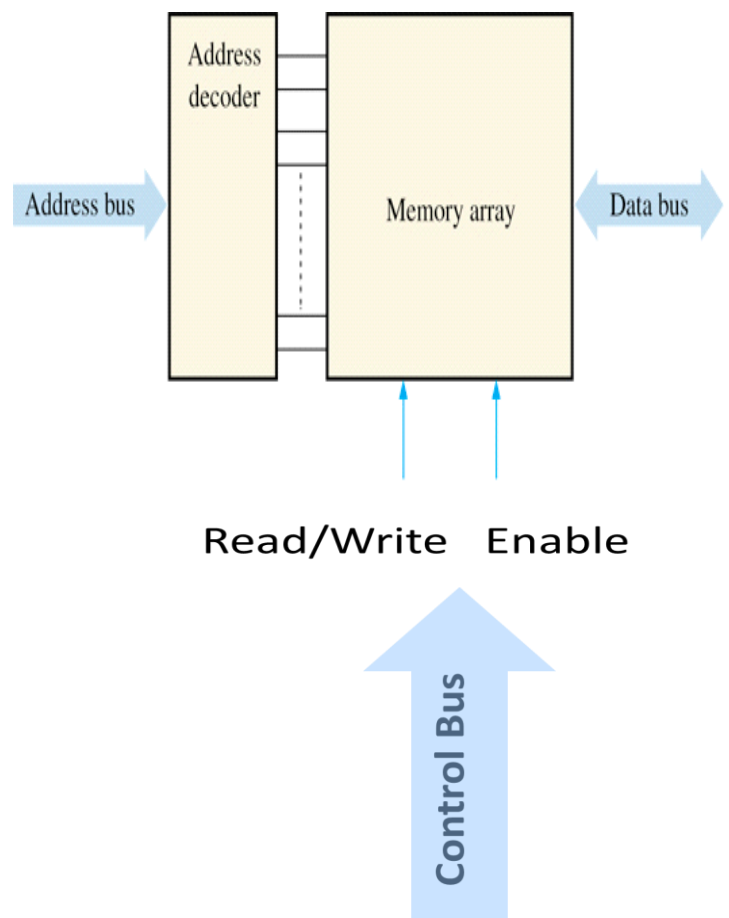


Fig: ROM block diagram



Block diagram of a memory showing address bus, address decoder, bidirectional data bus, and read/write inputs, Every memory system requires I/O lines to provide the following functions:

Select memory address being accessed for Read or Write operation, Select either a Read or Write operation Supply input data to be stored during a Write, Hold output data from memory during a Read Enable or disable memory so that it will or will not respond to read/write commands

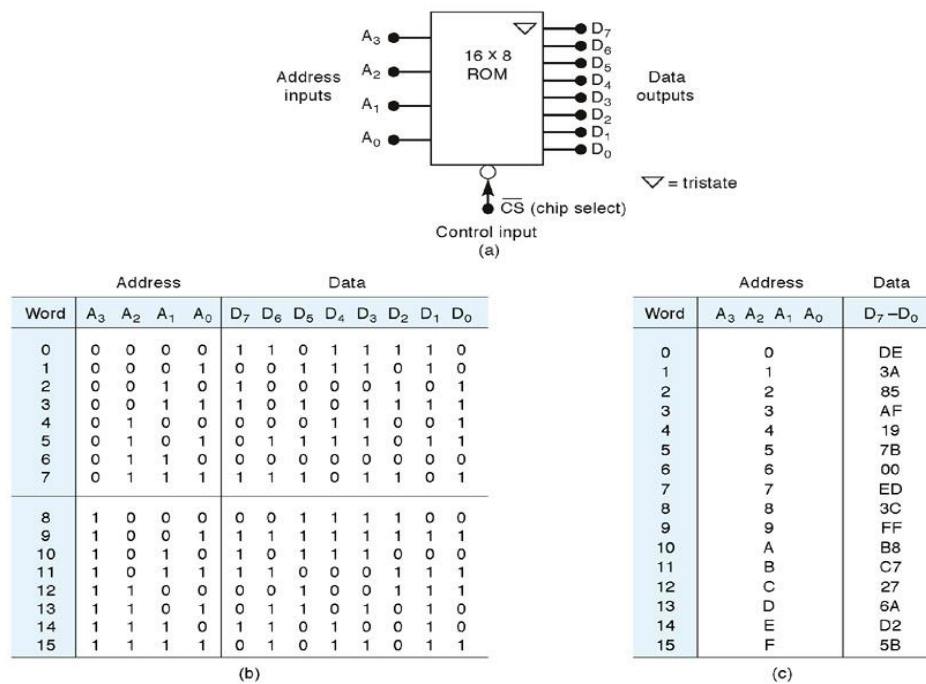
System bus functions:

Address bus – unidirectional, carries address outputs from CPU to memory

Data bus – bi-directional, carries data between CPU and memory ICs

Control bus – unidirectional, carries controls signals (such as R/W) from CPU to memory

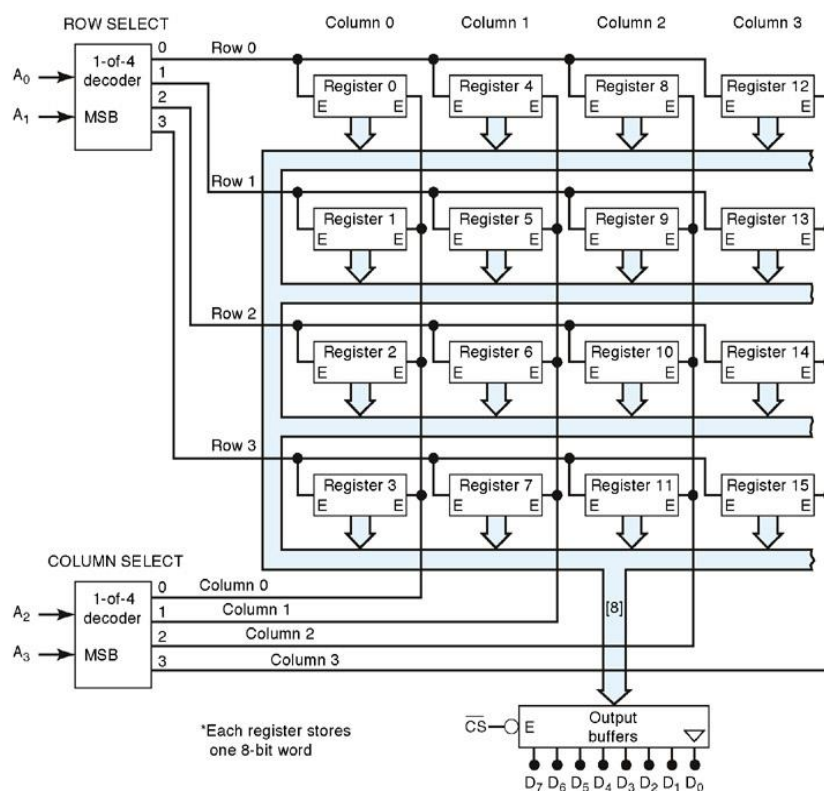
16*8 ROM:



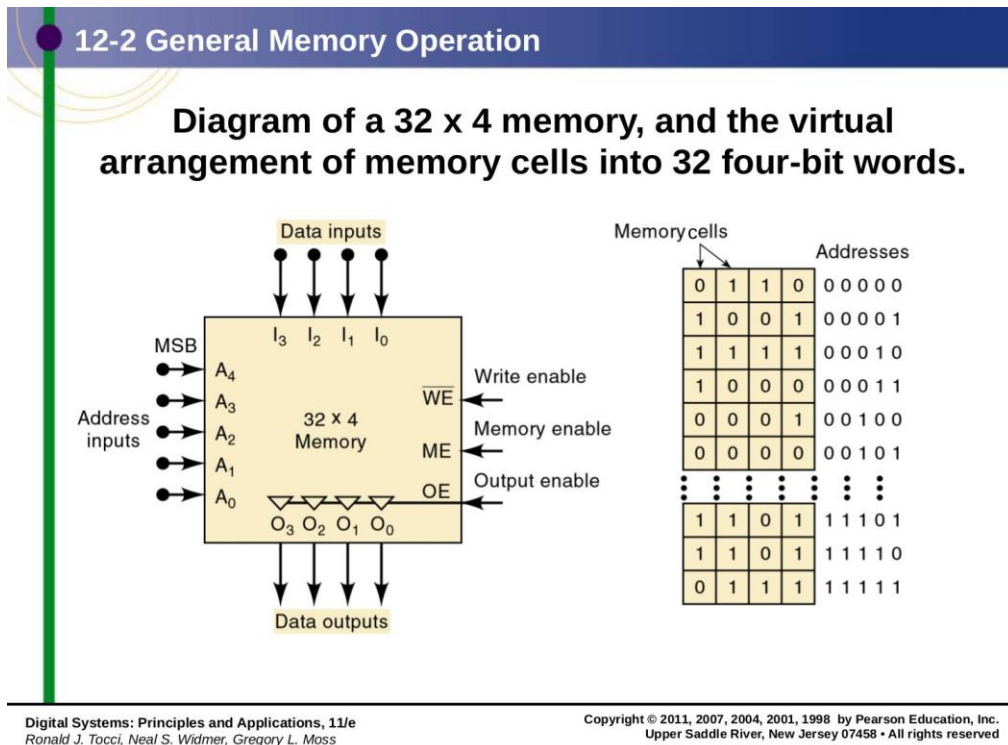
16 8-bit words can be stored.

- (a) Typical ROM block symbol: (b) table showing binary data at each address location; (c) the same table in hex.

Architecture of a 16 × 8 ROM



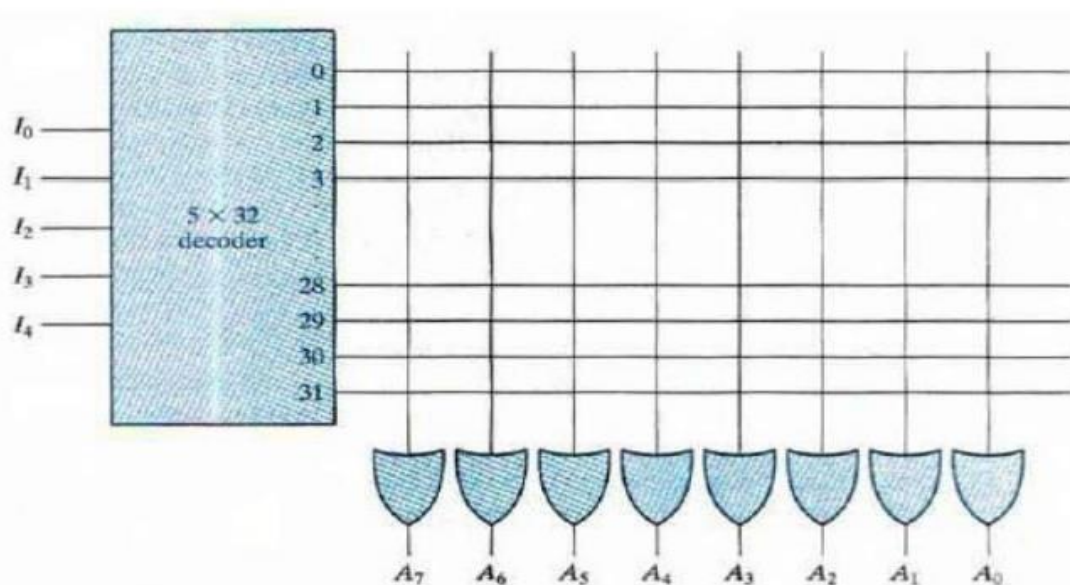
- Register array – stores data programmed into the ROM
- Address decoders – determines which register will be enabled by row and column
- Output buffers - pass data to the external data outputs
- CS – chip select, tri-state output buffers
- 2D memory example – 4 words (8 bits each) on a row (32 bit lines) and 4 word lines



32 X 8 ROM consists of 32 words and of 8 bits each. This means there are 8 output lines and that there are 32 distinct words stored in the unit, each of which may be applied to the output lines.

There are 5 input lines in a 32 X 8 ROM because $2^5 = 32$, and with 5 variables, we can specify 32 addresses or minterms.

If the input address is 00000, word number 0 is selected and appears on the output lines. If the input address is 11111, word number 31 is selected and appears on the output lines. There are 30 other addresses that can select the other 30 words.



Internal logic of a 32x 8 ROM

The five inputs are decoded into 32 distinct outputs by means of a 5 32 decoder. Each output of the decoder represents a memory address. The 32 outputs of the decoder are connected to each of the eight OR gates. Each OR gate must be considered as having 32 inputs. Each output of the decoder is connected to one of the inputs of each OR gate. Since each OR gate has 32 input connections and there are 8 OR gates, the ROM contains $32 \times 8 = 256$ internal connections.

A programmable connection between two lines is logically equivalent to a switch that can be altered to be either closed (meaning that the two lines are connected) or open (meaning that the two lines are disconnected). The programmable intersection between two lines is sometimes called a **cross point**.

ROM Truth Table (Partial)

Inputs					Outputs							
I_4	I_3	I_2	I_1	I_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		$\vdots$							$\vdots$			
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

For example, programming the ROM according to the truth table given by table. Every 0 listed in the truth table specifies the absence of a connection and every 1 listed specifies a path that is obtained by a connection.

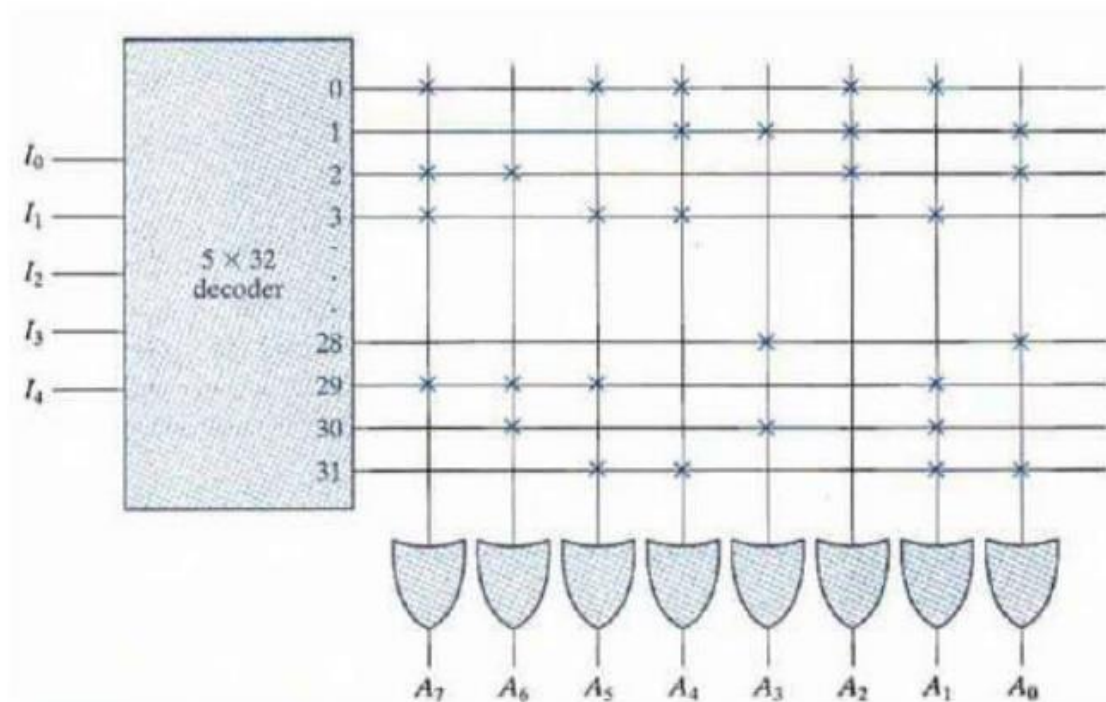
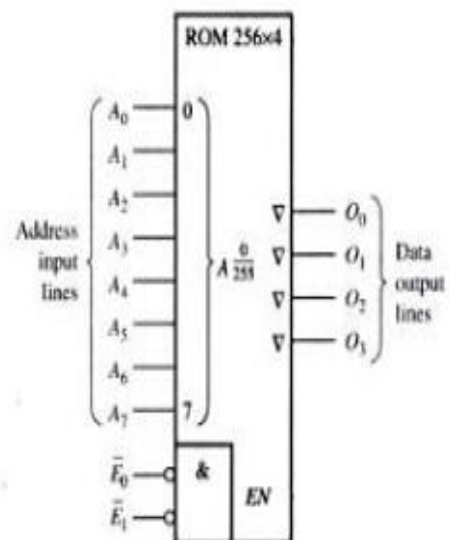


Fig: Programming the ROM according to ROM truth table

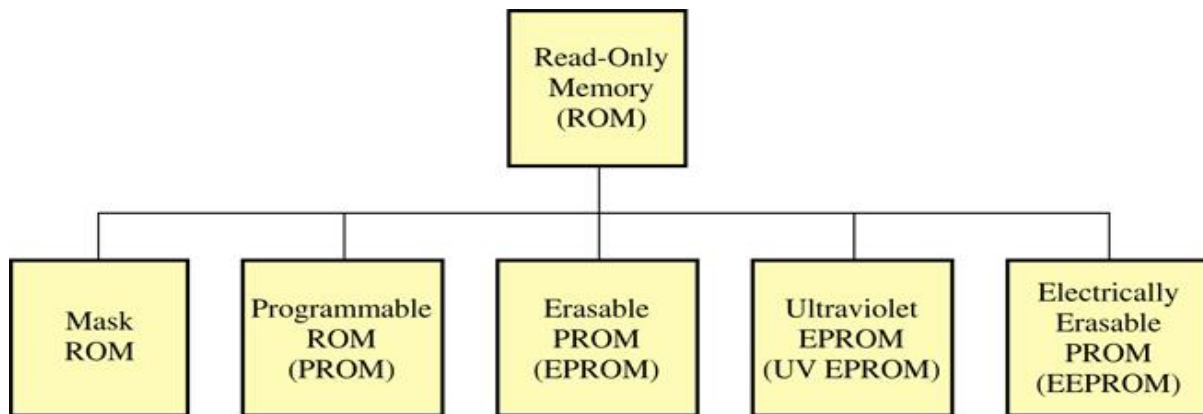
256 × 4 ROM:

► FIGURE 10-25

A 256 × 4 ROM logic symbol



ROM FAMILY:



Types of Read Only Memory (ROM)

ROM is differentiated on the basis of methods used to write data on ROM chips and the number of times they can be written. It can be classified into following types : –

1. Mask Read-Only Memory (MROM)
2. Programmable Read-Only Memory (PROM)
3. Erasable Programmable Read-Only Memory (EPROM)
4. Electrically Erasable Programmable Read-Only Memory (EEPROM)
5. Flash Read-Only Memory (Flash ROM)

Mask Read Only Memory (MROM):

The very first ROMs were hard-wired devices that contained a pre-programmed set of data or instructions. These kind of ROMs are known as masked ROMs. It is inexpensive ROM.

Applications of Mask Read Only Memory (MROM)

The Mask Read-Only Memory (MROM) are used for:

- Network Operating Systems.
- Server Operating Systems.
- Storing fonts for laser printers.
- Storing sound data in electronic musical instruments.

Advantage of Mask Read Only Memory (MROM)

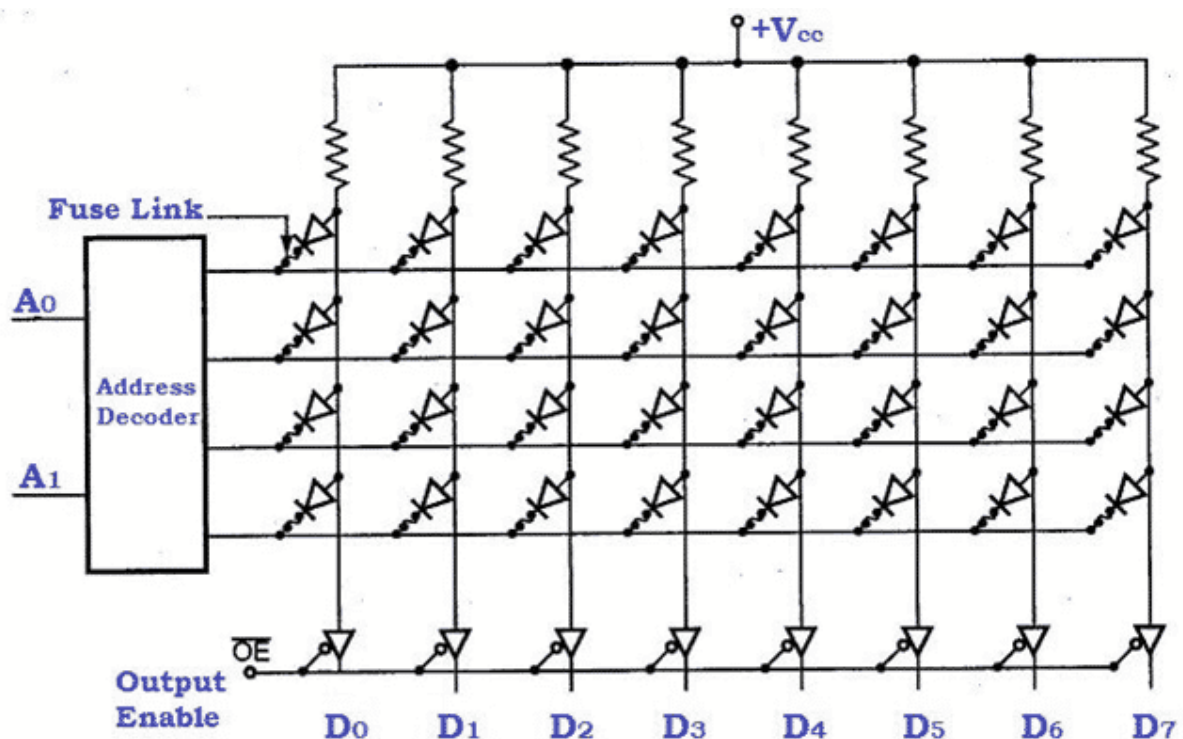
The main advantage of Mask Read-Only Memory (MROM) is its low production cost. The cost of IC depends on its size, per bit. Mask ROM is more compact. It is significantly cheaper than any other kind of secondary memory when large quantities of same ROM are manufactured.

Disadvantage of Mask Read Only Memory (MROM)

Design errors are costly i.e. if an error in the code is detected, the MROM is useless and must be replaced in order to change the code. The life expectancy of MROM is also short, hence requires frequent replacement.

Programmable Read Only Memory (PROM)

PROM stands for Programmable Read Only Memory. PROM is manufactured as a blank memory. And as its name suggests Programmable, it is programmed after manufacturing. The user buys a blank memory and enters the desired contents using a PROM program.



The process of programming a PROM is called burning the PROM. There are tiny fuses in a PROM chip which are burnt open during programming. The data can be programmed only once and cannot be altered. So it is called one- time programming device.

Applications of Programmable Read Only Memory (PROM)

The Programmable ROM (PROM) are used in:

- Mobile Phones for providing User Specific Selections.
- Video game consoles
- Implantable Medical devices.

- Radio-Frequency Identification (RFID)tags.
- High definition Multimedia Interfaces(HDMI)

Advantages of Programmable Read Only Memory (PROM)

The advantages of Programmable ROM (PROM) are: –

- The programming can be done using many types of software and does not rely on hard wiring of the program to the chip.
- Since it is not possible to un-blow the fuse, so the authenticity of the data remains intact and it is impossible to remove or alter the contents.

Disadvantage of Programmable Read Only Memory (PROM)

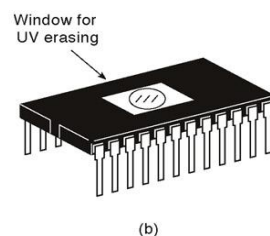
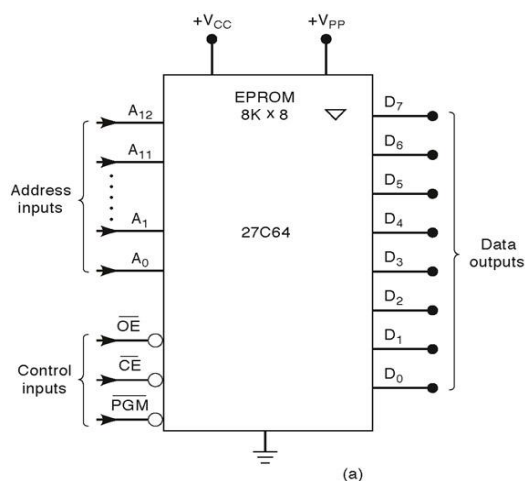
The biggest disadvantage of PROM is that the data once burnt cannot be erased or changed when detected with errors.

Erasable Programmable Read Only Memory (EPROM)

EPROM stands for Erasable Programmable Read-Only Memory. It is a non volatile memory i.e. it can retain data even if the power supply is cut off. The basic limitation being encountered in PROM is that once it is programmed, it cannot be changed or altered. This limitation has been overcome by EPROM.

EPROM can be erased by exposing it to ultra violet light for a particular length of time using an EPROM eraser. After exposing, the chip returns to its initial state and can be reprogrammed.

This procedure can be carried out many times but repeated erasing and rewriting can eventually render the chip useless. Once written, data can be retained for about 10 years.



	Inputs				Outputs
Mode	$\overline{CE}$	$\overline{OE}$	PGM	VPP	D ₇ – D ₀
Read	0	0	1	0–5V	DATA _{out}
Output Disable	0	1	1	0–5V	High Z
Standby	1	X	X	X	High Z
Program	0	1	0	12.75 V	DATA _{in}
PGM Verify	0	0	1	12.75 V	DATA _{out}

(c)

Applications of Erasable Programmable Read Only Memory (EPROM)

The applications of Erasable Programmable ROM (EPROM) includes:

- As program storage chip in Micro controllers.
- For debugging.
- For program development.
- As BIOS chip in computers.
- As program storage chip in modem, video card and many electronic gadgets.

Advantages of Erasable Programmable Read Only Memory (EPROM)

The advantages of Erasable Programmable ROM (EPROM) are:

- It is non-volatile.
- It can be erased and re-programmed.
- It is cost effective as compared to PROM.

Disadvantages of Erasable Programmable Read Only Memory (EPROM)

The disadvantages of Erasable Programmable ROM (EPROM) are:

- The static power consumption is high as the transistors used have higher resistance.
- It is not possible for a particular byte to be erased, instead the entire content is erased.
- UV based EPROM takes time to erase the content.

Electrically Erasable Programmable Read Only Memory (EEPROM)

EEPROM is the short form for Electrically Erasable Programmable Read Only Memory. It is similar to EPROM and thus developed to overcome the drawbacks of EPROMs. It is erased and programmed electrically i.e. it uses electrical signals instead of ultra violet rays.

The erasing and programming of data takes 4 to 10 milliseconds. Any byte can be erased at a time instead of the entire chip. The chip can be erased and re programmed for around ten thousand times, though the process is flexible but slow.

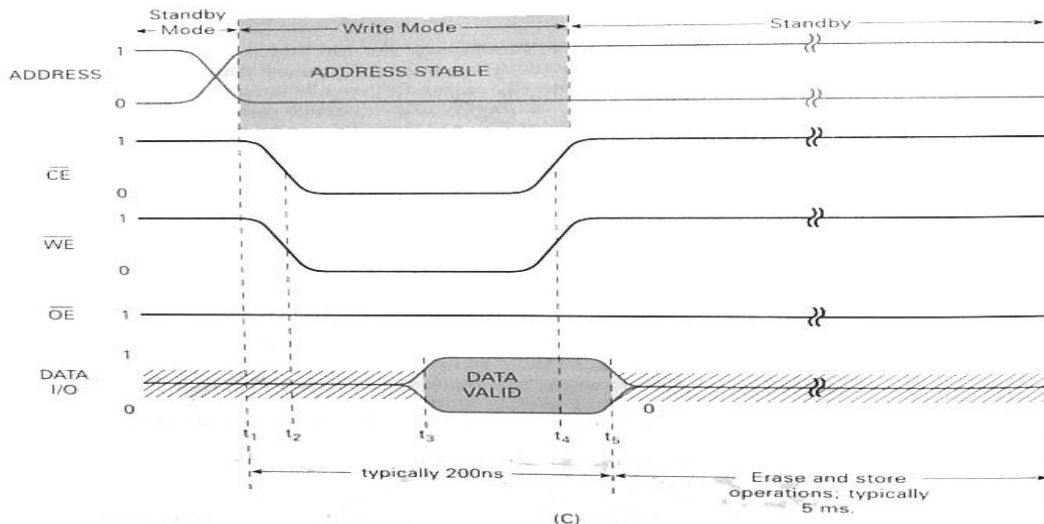
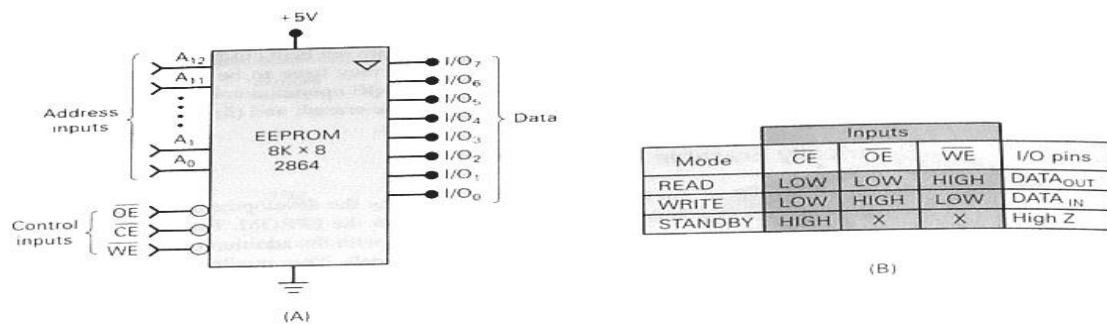


FIGURE 3.10 (A) Symbol for 2864 EEPROM; (B) operating modes; (C) timing for write operation.

Applications of Electrically Erasable Programmable Read Only Memory (EEPROM)

The applications of Electrically Erasable Programmable ROM (EPROM) includes:

- As BIOS chip in computers
- As storage for re-programmable calibration information in test-equipment.
- As storage for in-built self learning functionality in remote operated transmitters.

Advantages of Electrically Erasable Programmable Read Only Memory (EEPROM)

The advantages of Electrically Erasable Programmable ROM (EEPROM) are:

- The method of erasing is electrical and instant.
- Chip can be reprogrammed infinite number of times.
- Byte wise data can be erased instead of entire content on the board.
- To change the data, additional devices are not required.

Disadvantages of Electrically Erasable Programmable Read Only Memory (EEPROM)

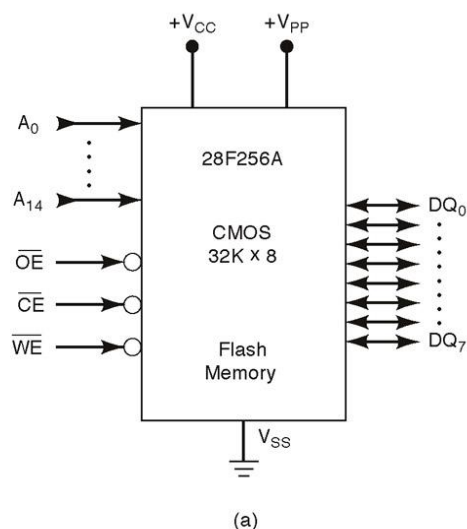
The disadvantages of Electrically Erasable Programmable ROM (EEPROM) are:

- Different voltages are required for erasing, reading and writing the data.
- The data retention period of EEPROM is limited i.e 10 years approx.
- EEPROM devices are expensive compared to others.

Flash Read Only Memory (Flash ROM)

It is a universal flash programming non volatile utility, used in computer as a storage medium. It can be electrically erased and reprogrammed. In this, memory blocks of data (512 bytes) can be deleted and written at a particular time.

- High density than EEPROM
- Faster erase and write time than EEPROM
- 2 mode of erase
 - bulk erase: erase all cell
 - sector erase: specified part of cell to erase e.g. 512 bytes
- Typical 10 usec write time
- Example 28F256A



Mode	Inputs			Data pins
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	
READ	LOW	LOW	HIGH	$DATA_{OUT}$
STANDBY	HIGH	X	X	High Z
WRITE*	LOW	HIGH	LOW	$DATA_{IN}$

*Note: If $V_{PP} \leq 6.5V$ a write operation cannot be performed

Has the in-circuit electrical erase-ability of an EEPROM and the high density and low cost of an EPROM (a single transistor is used at each cell location just like an EPROM).

Blocks or sectors of the memory array are erased at one time. Thereby, only a sector of the memory is erased and written to.

Example: USB FLASH cartridges or “sticks”. 1 GB or more is ~\$30 (Fall 2007).

Applications of Flash Read Only Memory (Flash ROM)

The applications of Flash Read-Only Memory (Flash ROM) are:

- The latest technology computers use BIOS stored on a flash memory chip, called as flash BIOS.
- Modems, pen drives, small cards use flash ROM.

Advantages of Flash Read Only Memory (Flash ROM)

The Advantages of Flash Read-Only Memory (Flash ROM) are:

- High transferring speed.
- It saves data when turns OFF, preserve its state without power.
- Less prone to damage.
- Comparatively economical to other drives in small storage capacities.

Disadvantages of Flash Read Only Memory (Flash ROM)

The disadvantages of Flash Read-Only Memory (Flash ROM) are:

- Comparatively costly than hard disk.
- Number of read/writes are limited.

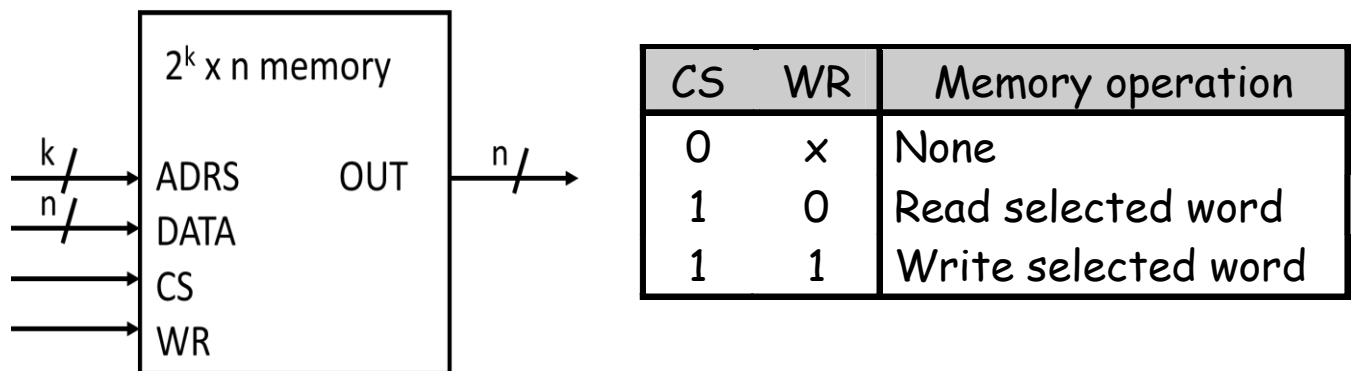
ROM Applications:

- Firmware: OS programs and language interpreters
- Bootstrap Memory: when the computer is powered on, it will execute the instructions that are in bootstrap program
- Data Tables
- Data Converter
- Function Generator
- Auxiliary Storage

RANDOM ACCESS MEMORY(RAM)

- RAM(Random Access Memory) is a part of computer's Main Memory which is directly accessible by CPU.
- RAM is used to Read and Write data into it which is accessed by CPU randomly.
- RAM is volatile in nature, it means if the power goes off, the stored information is lost.
- RAM is used to store the data that is currently processed by the CPU. Most of the programs and data that are modifiable are stored in RAM.

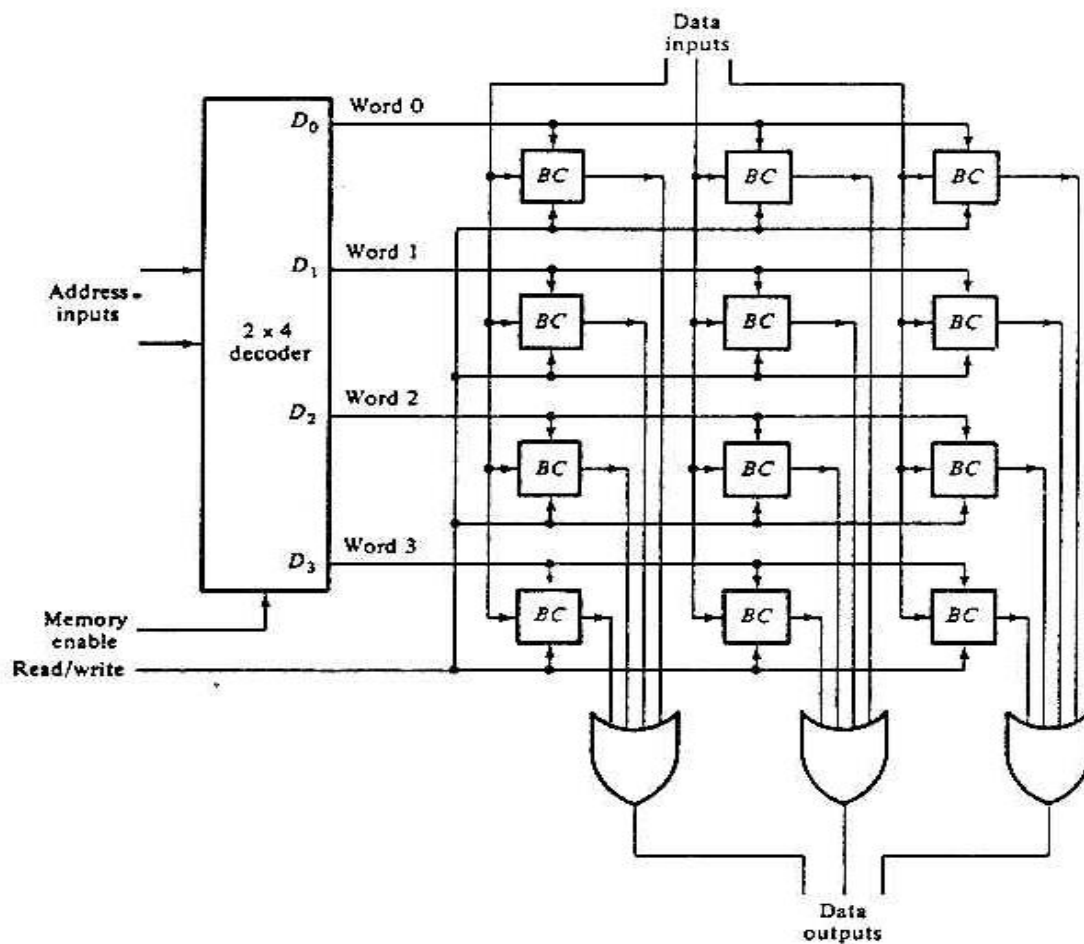
Block diagram of RAM:



This block diagram introduces the main interface to RAM.

- A Chip Select, CS, enables or disables the RAM.
- ADRS specifies the address or location to read from or write to.
- WR selects between reading from or writing to the memory.
- To read from memory, WR should be set to 0.
- OUT will be the n-bit value stored at ADRS.
- To write to memory, we set WR = 1.
- DATA is the n-bit value to save in memory.

Construction of a 4 x 3 RAM (with decoder and OR gates):



- There is a need for decoding circuits to select the memory word specified by the input address.
- During the read operation, the four bits of the selected word go through OR gates to the output terminals.
- During the write operation, the data available in the input lines are transferred into the four binary cells of the selected word.
- A memory with 2^k words of n bits per word requires k address lines that go into $k \times 2^k$ decoder.

RAM architecture:

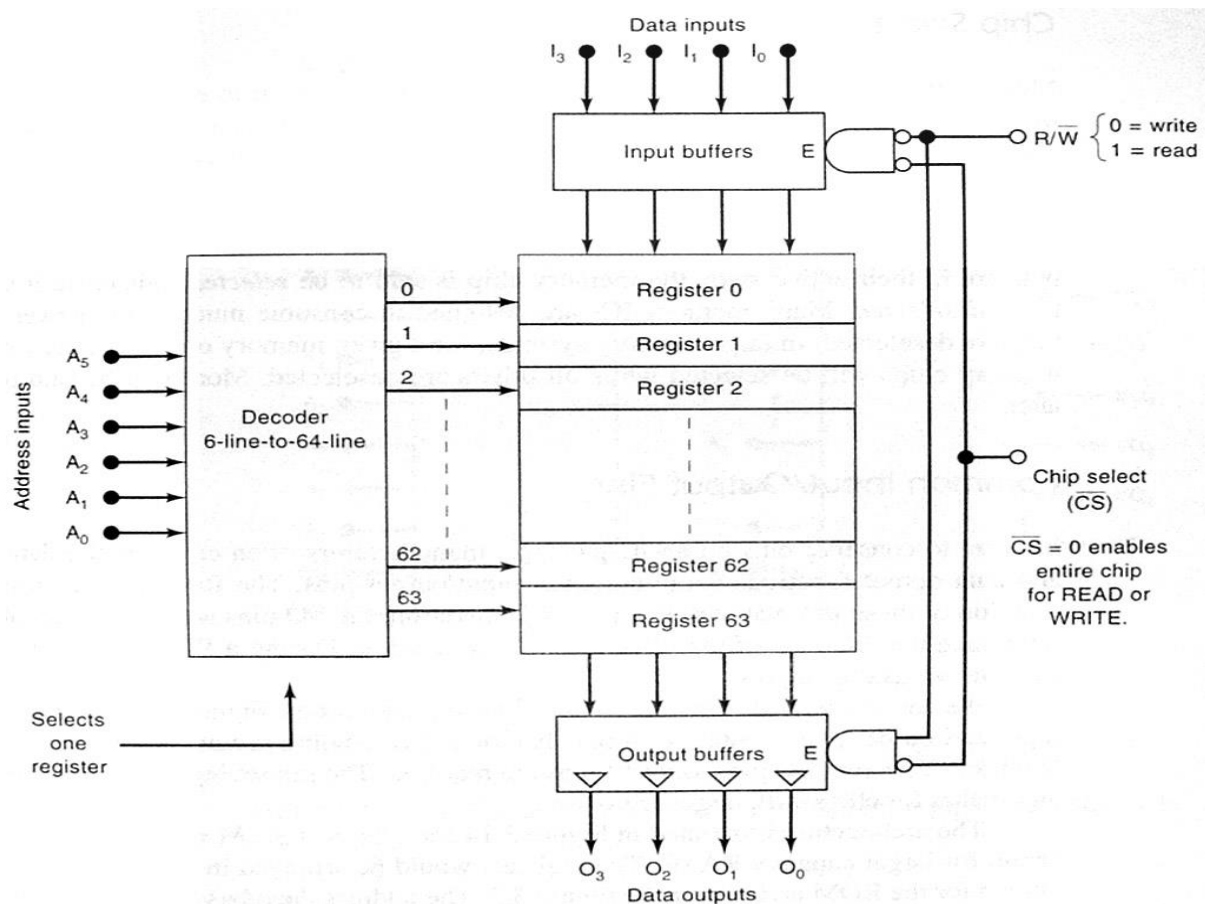


FIGURE 3.14 Internal organization of a 64×4 RAM.

- Set the address code at address bus
- Activate $\overline{CS}$ (Chip Select)
- When Write
 - set Data to Data bus
 - $R/\overline{W}$ set low
- When Read
 - $R/\overline{W}$ set high
 - Data comes out to data bus
 - $\overline{OE}$

TYPES OF RAM

RAM is of two types

- Static RAM (SRAM)
- Dynamic RAM (DRAM)

Static RAM (SRAM):

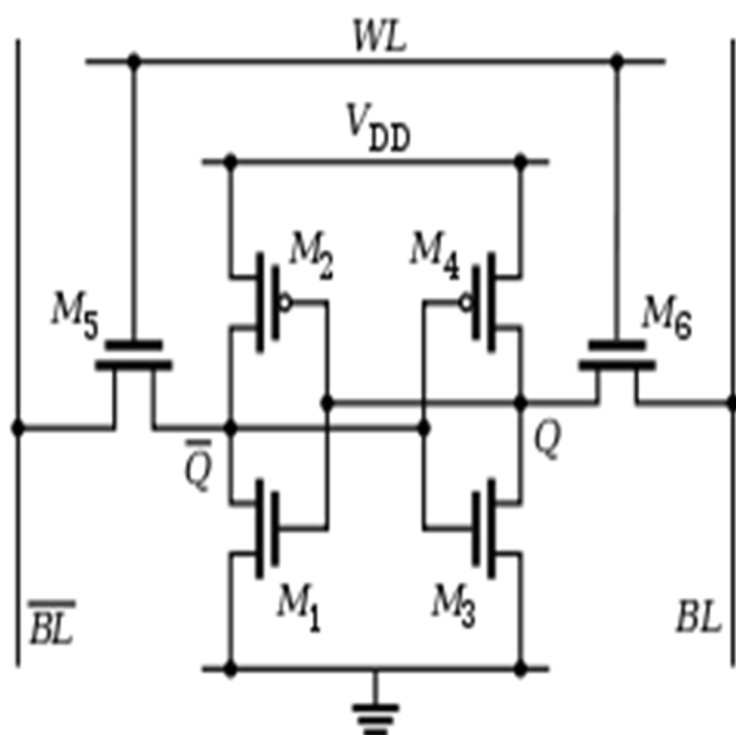
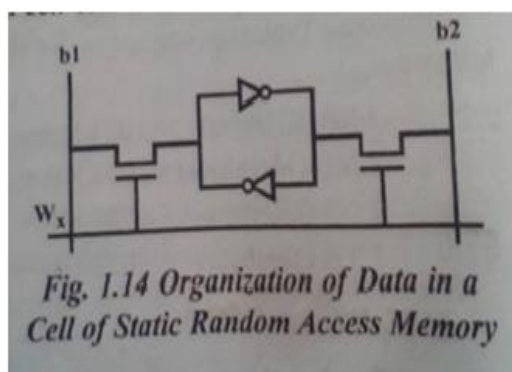
- The word **static** indicates that the memory retains its contents as long as power is being supplied. However, data is lost when the power gets down due to volatile nature.
- SRAM chips use a matrix of 6-transistors and no capacitors. Transistors do not require power to prevent leakage, so SRAM need not be refreshed on a regular basis.
- There is extra space in the matrix, hence SRAM uses more chips than DRAM for the same amount of storage space, making the manufacturing costs higher. SRAM is thus used as cache memory and has very fast access.

Characteristic of Static RAM

- Long life
- No need to refresh
- Faster
- Used as cache memory
- Large size
- Expensive
- High power consumption

Design Of SRAM

- A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (M_1 , M_2 , M_3 , M_4) that form two cross-coupled inverters.
- This storage cell has two stable states which are used to denote 0 and 1.
- Two additional access transistors serve to control the access to a storage cell during read and write operations.
- An SRAM cell has three different states. It can be in: *standby* (the circuit is idle), *reading* (the data has been requested) and *writing* (updating the contents).



Depending on the function performed by SRAM, it can be divided into the following types-

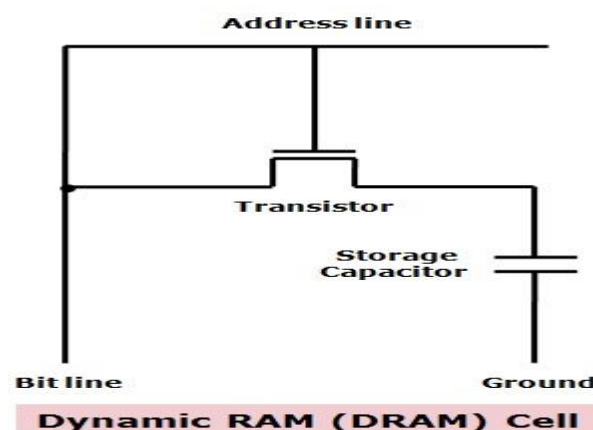
1. **Asynchronous SRAM (ASRAM)** – It performs its operations without the use of system clock. It makes use of three signals for working, namely, chip select (CS), write enable (WE) and output enable (OE). The CS signal enables the processor to select the memory for performing read and write operations. If $CS = 0$, then the memory is enabled to perform the operations. If $CS = 1$, then the memory is disabled and operations, such as reading and writing, cannot be performed. The WE signal makes the decisions related to data, i.e., whether it should be read from or write to the memory. If $WE = 0$, then no data can be read from or written to the memory. The

OE signal is an active low signal. It enables the processor to give the output for the data. If OE = 0, then only it will output the data.

2. **Burst SRAM (BSRAM)** – It works in association with the system clock and is also called synchronous SRAM. BSRAM is most commonly used with high-speed application because the read and write cycles are synchronized with the clock cycles of the processor. The accessed – waiting time gets reduced after the read and write cycles are synchronized with the clock cycles. The speed and the cost of BSRAM increases or decreases simultaneously.
3. **Pipeline Burst SRAM (PBSRAM)** – It uses pipeline technology in which a large amount of data is broken up in the form of different packets containing data. These packets are arranged in a sequential manner in the pipeline and are sent to the memory simultaneously. PBSRAM can handle a large amount of data at a very high speed. It is the fastest type of SRAM, since it can operate at bus rates as high as 66 MHz

Dynamic RAM (DRAM):

- In DRAM , the binary data is stored as charge in capacitor where the presence and absence of charge determines the value of stored bit .
- But data in capacitor cannot be stored for a long time because a capacitor holds an electrical charge for a limited amt. of time as the charge gradually drains away.
- DRAM cells require a periodic refreshing of the stored data .
- The use of capacitor as the primary storage device generally enables the DRAM cell to be realized on a much smaller area.
- Access devices or switches are used for RD/WR



Characteristics of Dynamic RAM:

- Short data lifetime
- Needs to be refreshed continuously
- Slower as compared to SRAM
- Used as RAM
- Smaller in size
- Less expensive
- Less power consumption

The DRAM can be divided into the following types-

1. **Synchronous DRAM (SDRAM)** – SDRAM performs its operations in the synchronous mode, i.e., in association with the clock cycle of the processor bus. It has two internal memory banks such that if the address lines are sent from the first bank, then the address can be read by using the second bank. The internal banks are used since the row and column address lines need to be charged for reading an address. SDRAM provides a synchronous interface in which it waits for a clock signal before responding to a control input. In general, it is used with the processors for storing the data in a continuous manner. The continuous form of data storage helps in processing more number of instructions per unit time that increases the speed of data access.
2. **Rambus DRAM (RDRAM)** – It is designed by Rambus Inc. it work at a faster speed, as compared to SDRAM. It is compact in size and uses 16-bit address bus. It provides the facility to transfer data at a maximum speed of 800 MHz. it contains multiple address and data lines that help in increasing the speed of data access. These multiple address and data lines help in performing different read and write operations simultaneously. It is not famous among users because of its high cost and low compatibility.
3. **Extended Data Out DRAM (EDODRAM)** – It can access more than one bit of data at one time which helps in achieving faster data access rates. It provides the facility to perform various operations at one time such as reading, writing, etc. it starts accepting the next bit of data immediately after getting the first bit of data for performing read or write operating.

4. **Fast Page Mode DRAM (FPMDRAM)** – It makes use of paging in which read or write operation is performed by selecting the address of the data from the rows and the columns of a matrix. Once the data is read, the address of the particular column is incremented to read the next part of the data. The paging concept in FPMDRAM does not allow to work with the buses at the memory speed more than 66 MHz. consequently, a lot of time is consumed in reading and writing the data from the matrix.

Difference between SRAM & DRAM:

DRAM	SRAM
1. Constructed of tiny capacitors that leak electricity.	1.Constructed of circuits similar to D flip-flops.
2.Requires a recharge every few milliseconds to maintain its data.	2.Holds its contents as long as power is available.
3.Inexpensive.	3.Expensive.
4. Slower than SRAM.	4. Faster than DRAM.
5. Can store many bits per chip.	5. Can not store many bits per chip.
6. Uses less power.	6.Uses more power.
7.Generates less heat.	7.Generates more heat.
8. Used for main memory.	8. Used for cache.

Difference between SRAM and DRAM