LINEAR AND DIGITAL INTEGRATED CIRCUITS

LECTURE NOTES

B.TECH
(III YEAR – I SEM)
(2020-21)

Prepared by:
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OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
Recognized under 2(f) and 12 (B) of UGC ACT 1956
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MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

III Year B.Tech. EEE-I Sem	L	T/P/D	C
	3	1/-/-	4

(R18A0409) LDIC

COURSE OBJECTIVES:

The main objectives of the course are:

1. To introduce the basic building blocks of linear integrated circuits.
2. To teach the linear and non-linear applications of operational amplifiers.
3. To teach the theory of ADC and DAC.
4. To introduce the concepts of waveform generation and introduce some special function ICs.
5. To understand and implement the working of basic digital circuits.

UNIT - I:

OPERATIONAL AMPLIFIER: Ideal and Practical Op-Amp, Op-Amp Characteristics, DC and AC Characteristics, Features of 741 Op-Amp, Block diagram of Op-Amp, Modes of Operation - Inverting, Non-Inverting, Differential, Instrumentation Amplifier, AC Amplifier, Differentiators and Integrators, Comparator and its applications, Schmitt Trigger, Introduction to Voltage Regulators, Features of 723 Regulator, Three Terminal Voltage Regulators.

UNIT - II:

OP-AMP, IC-555 & IC 565 APPLICATIONS: Introduction to Active Filters, Characteristics of Band pass, Band reject and All Pass Filters, Analysis of 1st order LPF& HPF Butterworth Filters, waveform Generators - Triangular, Saw-tooth, Square wave, IC555 Timer - Functional Diagram, Monostable and Astable Operations, Applications, IC565 PLL - Block Schematic, Description of Individual Blocks, Applications.

UNIT - III:

DATA CONVERTERS: Introduction, Basic DAC techniques, Different types of DACs-Weighted resistor DAC, R-2R ladder DAC, Inverted R-2R DAC, Different Types of ADCs - Parallel Comparator Type ADC, Counter Type ADC, Successive Approximation ADC and Dual Slope ADC, DAC and ADC Specifications.

UNIT - IV:

DIGITAL INTEGRATED CIRCUITS: Classification of Integrated Circuits, Combinational Logic ICs - Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs - Code Converters, Decoder, Encoder, Priority Encoder, Multiplexer, De-multiplexer, Parallel Binary Adder/ Subtractor, Magnitude Comparator.

UNIT - V:

SEQUENTIAL LOGIC IC'S AND MEMORIES: Familiarity with commonly available 74XX & CMOS 40XX Series ICs - All Types of Flip-flops, conversion of Flip-flops, Synchronous Counter, Decade Counter, Shift Register.

Memories - ROM Architecture, Types of ROMS & Applications, RAM Architecture, Static & Dynamic RAMs.

TEXT BOOKS:

1. Linear Integrated Circuits – D. Roy Chowdhury, New Age International (p) Ltd, 2nd Edition,2003.
2. Op-Amps & Linear ICs - Ramakanth A. Gayakwad, PHI, 2003.
3. Digital fundamentals – Floyd and Jain, Pearson Education,8th Edition ,2005.

REFERENCE BOOKS:

1. Op Amps & Linear Integrated circuits-Concepts and Applications James M.Fiore,Cengage Learning/Jaico,2009.
2. Operational Amplifiers with linear integrated circuits by K.Lal kishore-Pearson,2009.
3. Linear integrated circuits and applications-Salivahana,TMH.
4. Modern digital electronics-RP Jain-4/e-TMH,2010.
5. Digital design principles and practices-John.F.Wakerly 3/e,2005.
6. Operational amplifiers with linear integrated cuircuits,4/e William D.Stanley,Pearson education India,2009.

COURSE OUTCOMES:

On completion of this course, the students will have:

1. A thorough understanding of operational amplifiers with linear integrated circuits.
2. Understanding of the different families of digital integrated circuits and their characteristics.
3. Also students will be able to design circuits using operational amplifiers for various applications

Subject: LDIC Notes

Unit 1 : Operational Amplifier

Introduction of ICs

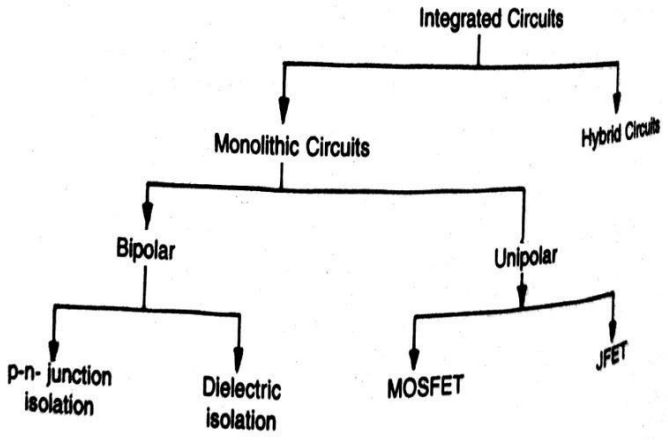


Fig. 1.1 Classification of ICs

Invention of transistor (Ge)		1947
Development of Silicon transistor		1955–1959
Silicon Planar Technology	Junction transistor diode	1959
First ICs, Small Scale Integration (SSI)	3 to 30 gates/chip approx. or 100 transistors/chip (Logic gates, Flip-flops)	1960–65
Medium Scale Integration (MSI)	30 to 300 gates/chip or 100 to 1000 transistors/chip (Counters, Multiplexers, Adders)	1965–1970
Large Scale Integration (LSI)	300 to 3000 gates/chip or 1000–20,000 transistors/chip (8 bit microprocessors, ROM, RAM)	1970–1980
Very Large Scale Integration (VLSI)	More than 3000 gates/chip or 20,000–1,00,00,00 transistors/chip (16 and 32 bit microprocessors)	1980–1990
Ultra Large Scale Integration (ULSI)	$10^6 - 10^7$ transistors/chip (Special processors, Virtual reality) machines, Smart sensors	1990–2000
Giant-Scale Integration (GSI)	$> 10^7$ transistors/chip	

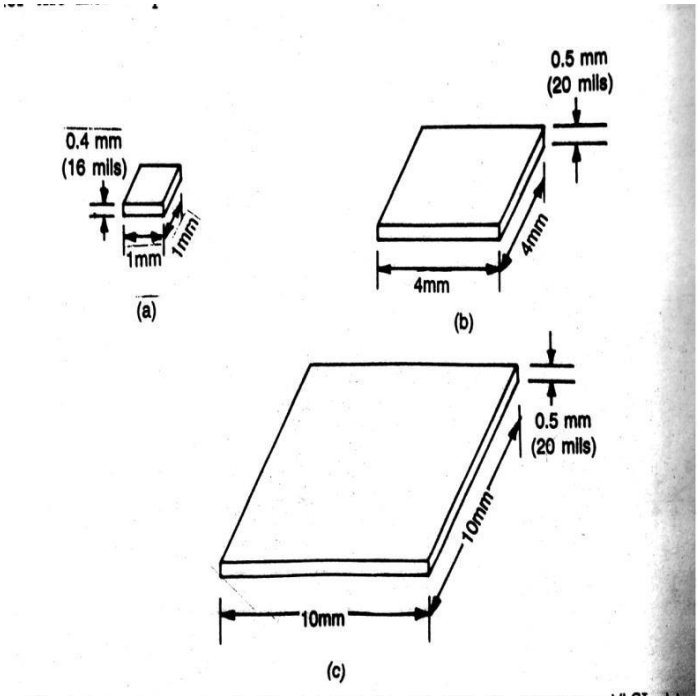


Fig. 1.2 Integrated circuit chips (a) SSI chip (b) MSI chip (c) LSI or VLSI chip

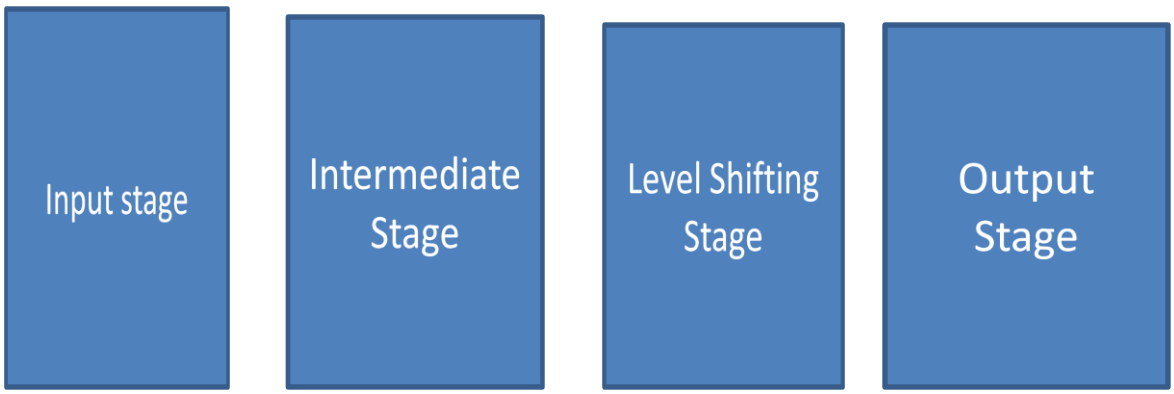
Operational Amplifier

- An operational amplifier is a direct coupled high gain amplifier usually consisting of one or more differential amplifier and usually followed by a level translator and an output stage.
- An operational amplifier is available as a single integrated circuit package.
- The operational amplifier is a versatile device that can be used to amplify DC as well as AC input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication and integration.
- With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications such as AC and DC signal amplification, active filters, oscillator, comparators and regulators, and others

Block Diagram of Op-amp.

Since an op-amp is a multi stage amplifier it can be represented by a block diagram as shown in the following figure.

Non-inverting input terminal



- The input stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp
- Because of the direct coupling used, the DC voltage at the output of the intermediate stage is well above the ground potential. Therefore, generally, the level translator circuit is used after the intermediate stage
- The final stage is usually a push-pull complimentary amplifier output stage. The output stage increases the output voltage swing and raises the current supplying capability of op-amp. A well designed output stage also provides low output resistance.

The IDEAL Op-amp

- An IDEAL op-amp would exhibit the following electrical characteristics.
  - Infinite voltage gain, A
  - Infinite input resistance Ri
  - Zero output resistance Ro
  - Zero output voltage when input voltage is zero.

- Infinite bandwidth – any signal can be amplified without attenuation
- Infinite common mode rejection ratio
- Infinite slew rate so that output voltage changes occur simultaneously with input voltage changes.

Practical Op-amp.

Input offset voltage: Input offset voltage Vio is the differential input voltage that exists between two input terminals of an op-amp without any external inputs applied.

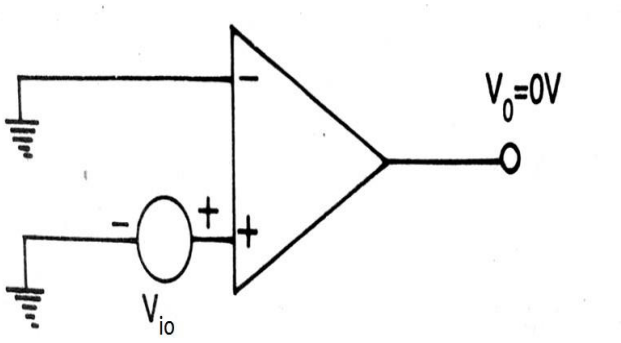


Fig. 3.2 (a) Op-amp showing input offset voltage

Output Offset Voltage:

- The output voltage caused by mismatching between two input terminals is called the output offset voltage Voo.
- The output offset voltage Voo is a DC voltage, it may be +ve or –ve in polarity depending on whether the potential differences between the two input terminals is +ve or –ve.

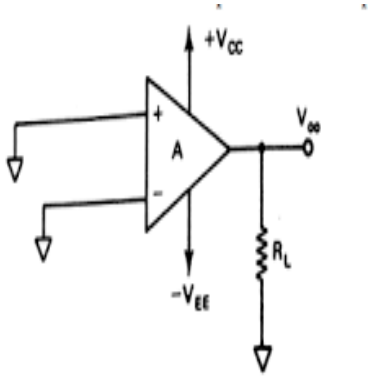
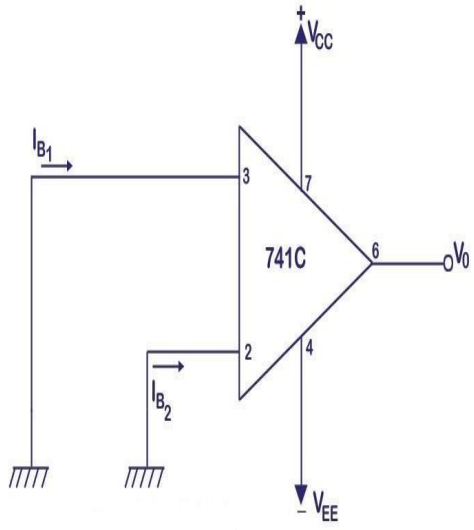


Figure 2 : Output offset voltage in op-amp

- **Input offset Current:**
  - The input offset current Iio is defined as the algebraic difference between two input bias currents Ib1 and Ib2. In equation form it is

Iio = |Ib1 – Ib2|



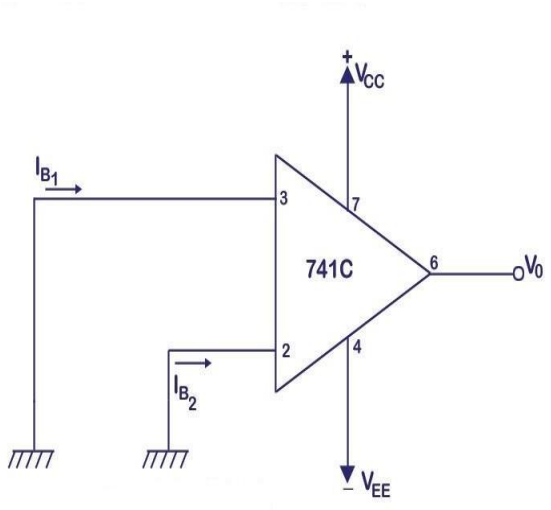
- **Input Bias Current:**
  - An input bias current Ib is defined as the average of the two input bias currents, Ib1 and Ib2 as shown in the following figure.

Ib = (Ib1 + Ib2)/2 [Ib – DC current]

Where Ib1= DC bias current flowing into the non-inverting input

Ib2 = DC bias current flowing into the inverting input

- The value of input bias current Ib is very small, in the range of a few to few hundred nano amp.



- **Thermal Drift:**
  - The average rate of change of input offset voltage per unit change in temperature is called thermal voltage drift, and is denoted by ΔVio/ΔT. Units – µV/°C
  - Similarly, the thermal drift in the input offset current & input bias current are defined as follows.
  - ΔIio/ ΔT= thermal drift in input offset current(pA/°C)
  - ΔIb/ ΔT= thermal drift in input bias current(pA/°C)

- **Supply Voltage Rejection Ratio (SVRR) or Power Supply Rejection Ratio (PSRR):**
  - The change in op-amp's input offset voltage caused by variations in the supply voltages is called Supply voltage Rejection Ratio or Power Supply Rejection Ratio.
  - This is expressed either in microvolts per volt or in decibles
  - For example, SVRR for μA741 is ΔVio/ΔV =150 μV/V maximum and it is 76.48 in DB.
- **Common Mode Rejection Ratio (CMRR)**:
  - It can be defined as the ratio of the differential gain AD to the common mode gain Acm, that is CMRR = Ad/Acm
  - It is a measure of the degree of matching between two input terminals, that is, the larger the value of CMRR, the better is the matching between the two input terminals and the smaller is the output common mode voltage Vocm.

Differences between Ideal and Practical Op-amp

Characteristics	Ideal Op-amp	Practical O
Voltage gain	Infinite	High
Input resistance	Infinite	High
Output resistance	Zero	Low
Output voltage when input voltage is zero	Zero	Low
Band width	Infinite	High
CMRR	Infinite	High
Slew Rate	Infinite	High

Characteristics of Op-amp

DC Characteristics

DC Characteristics include input bias current, input offset current, Input offset voltage, Output offset voltage and Thermal drift.

AC Characteristics:

AC characteristics include

- Frequency Response
- Slew Rate

- **Frequency Response:**
  - Ideally an op-amp should have an infinite band width.
  - The practical op-amp gain, however, decreases at higher frequencies.
  - What is the cause for the gain of the op-amp to roll-off after certain frequency is reached?
  - Obviously, there must be a capacitive component in the equivalent circuit of the op-amp. This capacitace is due to the physical characteristics of the device(BJT or FET) used and internal construction of op-amp.
  - For an op-amp with only one break frequency, all the capacitor effects can be represented by a single capacitor C as shown in figure 3.4 (a).

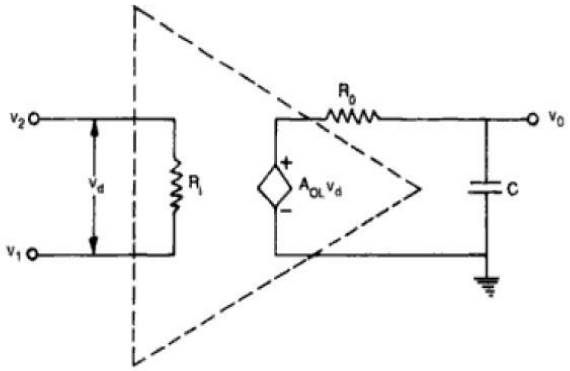


Fig. 3.4 (a) High frequency model of an op-amp with single corner frequency

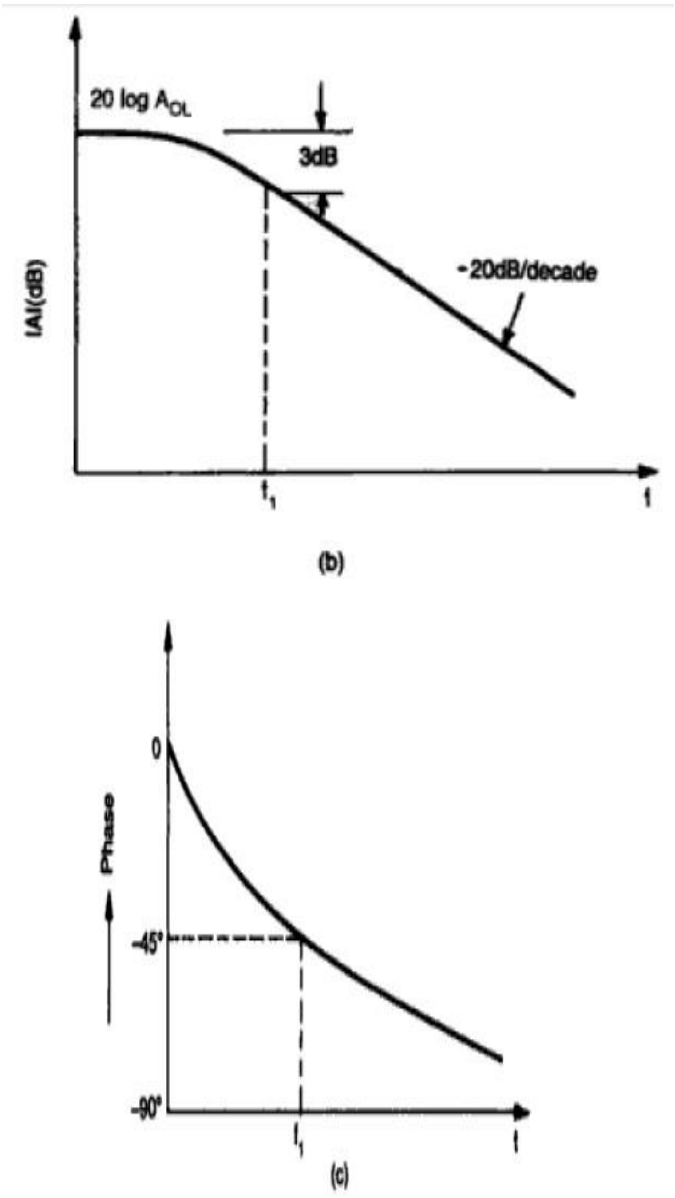


Fig. 3.4 (b) Open loop magnitude characteristics in semilog paper and (c) phase characteristics for an op-amp with single break frequency

- The open loop voltage gain of an op-amp with only one corner frequency is obtained from Figure 3.4(a) as

  $V_o = -j X_c/(R_o - jX_c) A_{ol} V_d$

  $\Rightarrow A = V_o/V_d = A_{ol}/(1+j2\pi f R_o C)$

$A = Aol/(1+jf/f1)$ where $f1 = 1/2\pi Ro C$

- f1 is the corner frequency or the upper 3 dB frequency of the op-amp.
- The magnitude and the phase angle of the open loop voltage gain are function of frequency and can be written as
- $|A| = Aol/(\sqrt{(1+(f/f1)^2)}$ $\phi = -\tan^{-1}(f/f1)$
- these are shown in Fig 3.4(b) and 3.4 (c)
- It can be seen that
- For frequency f<<f1, the magnitude of the gain is 20 log Aol in dB.
- At frequency f = f1, the gain is 3 dB down from the DC value of Aol in dB. This frequency f1 is called corner frequency
- For f>>f1, the gain rolls off at the rate of -20dB/decade.
- It can further be seen from the phase characteristics that the phase angle is zero at frequency f=0.
- At corner frequency f1, the phase angle is -45° and at infinite frequency the phase angle is -90°. This shows that a maximum of 90° phase change can occur in an op-amp with a single capacitor.
- **Slew Rate:**
    - The slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per micro seconds. In equation form, $SR = (dVo/dt)|_{maximum}$ V/μs.
    - Slew rate indicates how rapidly the output of an op-amp can change in response to changes in the input frequency.
    - One of the drawbacks of the 741C is it's low slew rate(0.5 V/μs), which limits its use in relatively high frequency applications, especially in oscillators, comparators and filters
- In high-speed op-amps especially, the slew rate is significantly improved. For instance, the LM138 has a slew rate of 70 V/μs.

- What causes the slew rate? There is usually a capacitor with in or outside an op-amp to prevent oscillation. It is this capacitor which prevents the output voltage from responding immediately to a fast changing input.
- The rate at which the voltage across the capacitor Vc increases is given by dVc/dt = I/C. Here, I is the maximum current furnished by op-amp to the capacitor C. This means that for obtaining faster slew rate, op-amp should have either a higher current or a small compensating capacitor.
- For the 741C, that maximum internal capacitor charging current is limited to about 15 µA. So the slew rate of 741C is

  SR = dVc/dt|max = Imax/C = 15 µA/30 PF = 0.5 V/ µs.

741 Op-amp and It's features

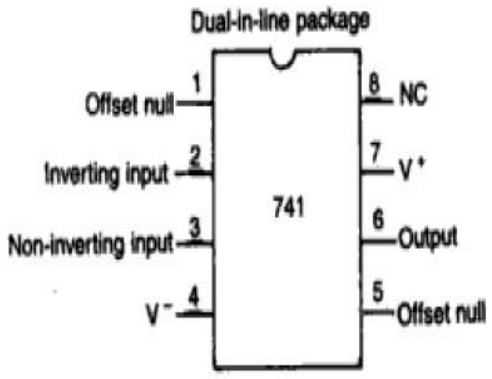


Fig. Pin configuration

- The µA741 is a high performance monolithic operation amplifier constructed using the planar epitaxial process.

The op-amp features are given below

1. High common mode voltage range make the µA741 ideal for use as voltage follower.
2. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.
3. 741 is internally frequency compensated op-amp

4. 741 is available in all 3 packages viz 8-pin metal can, 10-pin flat pack, and 8 or 14 pin DIP.
5. Offset voltage null capability is available.
6. It consumes low power

Modes of op-amp

- Basically there are 2 modes of op-amp. They are
  - Inverting Amplifier
  - Non-Inverting Amplifier

Inverting Amplifier

- There are two types of connecting inverting amplifier. They are
  - Open loop inverting amplifier
  - Closed loop inverting amplifier

Open Loop Inverting Amplifier

- The circuit diagram for the open loop inverting amplifier is shown in figure 3-10.

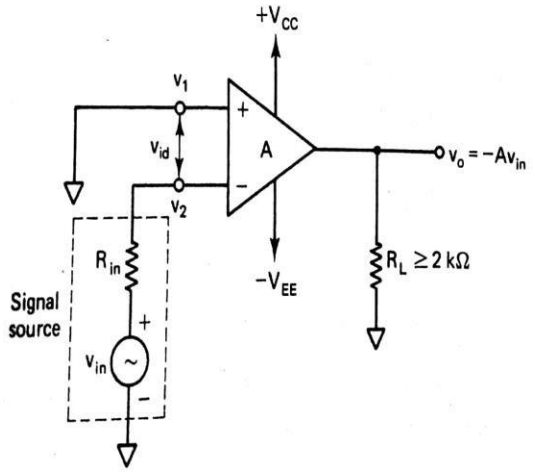


Figure 3–10 Inverting amplifier.

- The equation for the output voltage is given by

  Vo= A(V1 – V2)

  where A – large signal voltage gain

  V1 – voltage at non-inverting input terminal

  V2 – voltage at inverting input terminal

  here V1 = 0 and V2 = Vi therefore

  Vo = A (-Vi) = - A Vi

- The negative sign indicates that the output voltage is out of phase with respect to the input by 180° or is of opposite polarity.
- Thus in the inverting amplifier the input signal is amplified by gain A and is also inverted at the output.

Closed Loop Inverting amplifier

- This is perhaps the most widely used of all the op-amp circuits.
- The circuit is shown in the figure 2.5(a)

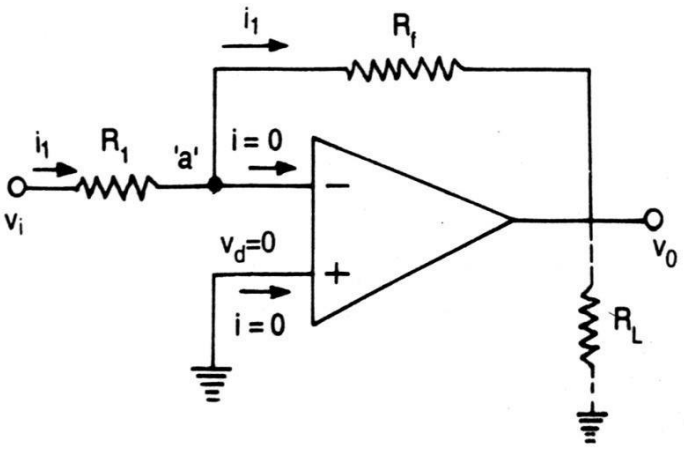


Fig. 2.5 (a) Inverting amplifier

- For simplicity, assume ideal op-amp. As Vd=0, node ‘a’ is at ground potential and the current i1 through R1 is i1 = Vi/R1
- Also since op-amp draws no current, all the current flowing through R1 must flow through Rf. Hence the output voltage is

Vo = -i1 Rf = -(Vi/R1) Rf

therefore the gain of the closed loop inverting amplifier is Acl = Vo/Vi = -Rf/R1

- The –ve sign indicates a phase shift of 180° between Vi and Vo.

Example 2.2:

- In figure 2.5(b), R1 = 10KΩ, Rf = 100KΩ, Vi=1v. A load of 25 KΩ is connected at the output terminal. Calculate (i) I1 (ii) V0 (iii) il and total current io into the output pin

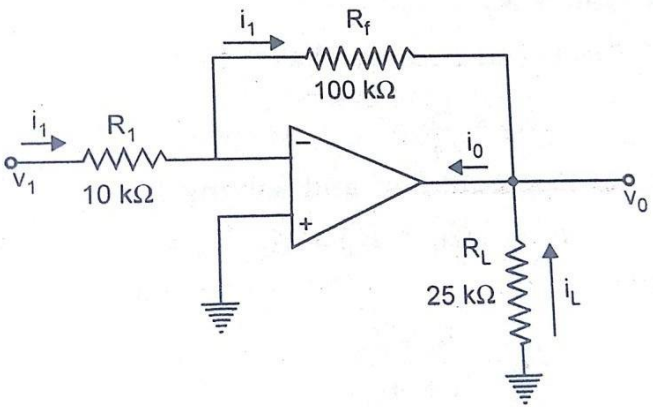


Fig. 2.5 (b) Circuit for Example 2.2

(i) i1 = Vi/R1 = 1V/10KΩ = 0.1 mA

(ii) Vo = -Rf/R1 Vi = -10V

(iii) il = -Vo/Rl = 10V/25 KΩ = 0.4 mA

Therefore Io = i1+ il = 0.1 mA + 0.4 mA = 0.5 mA

Non-Inverting Amplifier:

- There are two types of connecting non-inverting amplifiers. They are
  - Open loop non-inverting amplifier
  - Closed loop non-inverting amplifier

Open Loop Non-inverting amplifier

- Figure 3.11 shows the open loop non-inverting amplifier

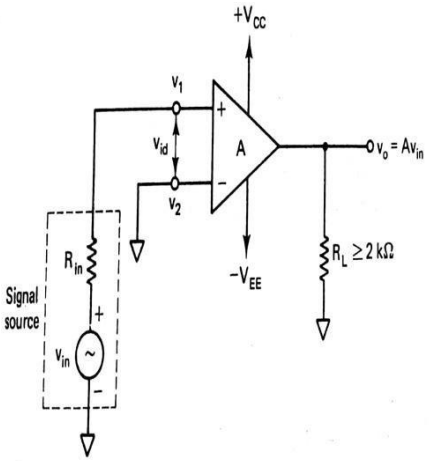


Figure 3-11 Noninverting amplifier.

- Output voltage, Vo = A (V1 – V2)

  here V1 = Vi and V2 = 0 v

  therefore Vo = A Vi

- This means that the output voltage is larger than the input voltage by gain A and is in phase with the input signal.

Closed Loop Non-Inverting Amplifier:

- If the signal is applied to the non-inverting input terminal and feedback is given as shown in Figure 2.7(a), the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier.

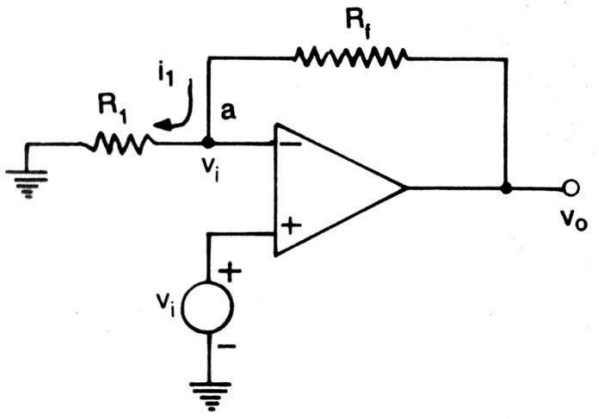


Fig. 2.7 (a) Non-inverting amplifier

- As Vd=0, the voltage at node ‘a’ in Figure 2.7(a) is Vi. Now R1 and Rf forms a potential divider.

  Hence Vi = (Vo/(R1+Rf)) * R1 as no current flows into op-amp.

  therefore Vo/Vi = (R1+Rf)/R1 = 1+ (Rf/R1)

- Thus, for non-inverting amplifier the voltage gain Acl = Vo/Vi = 1 + (Rf/R1)
- The gain can be adjusted to unity or more, by proper selection of resistors Rf and R1.

Difference Amplifier:

- Figure 4.14 shows the diagram of difference amplifier

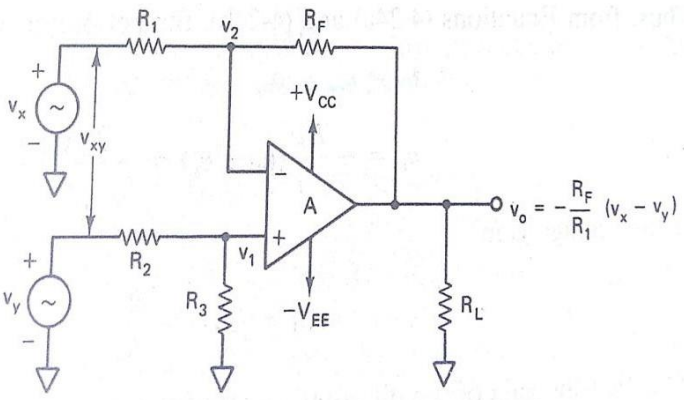


Figure 4–14 Differential amplifier with one op-amp. $R_1 = R_2$ and $R_F = R_3$.

- A close examination of the figure 4-14 reveals that difference amplifier is a combination of inverting and non-inverting amplifiers i.e. when Vx = 0, circuit is a non-inverting amp.

  when Vy = 0, circuit is an inverting amp.

Voltage Gain:

- The circuit in the figure 4-14 has two inputs Vx and Vy. Therefore we use super position theorem in order to establish the relation ship between inputs and output.
- When Vy = 0, the output voltage due to Vx only is Vox = -(Rf/R1) Vx--------eq(1)a

Similarly when Vx=0, the configuration is a non-inverting amplifier having a voltage divider network composed of R2 and R3 at the non-inverting input. Therefore V1 = (R3/R2+R3) (Vy)

the output due to Vy alone is

Voy = (1 + Rf/R1) V1 ➔

Voy= (R1+Rf)/R1 (R3/R2+R3) Vy

Since R1 = R2 and Rf = R3, Voy= (Rf/R1) (Vy) ----- eq(1)b

Thus from equations (1)a and (1)b, the net output voltage is Vo = Vox + Voy
➔ Vo= (-Rf/R1) (Vx – Vy) = - (Rf/R1) Vxy therefore the voltage gain Ad=Vo/Vxy = -Rf/R1

- Note that the gain of the difference amplifier is the same as that of the inverting amplifier.

Input Resistance:

The input resistance Rif of the difference amplifier is the resistance determined looking into either one of the two input terminals with the other grounded

- Therefore with Vy = 0, the input resistance of the inverting amplifier is **Rifx = R1** ------ eq(2)a
- Similarly with Vx=0, the input resistance of non-inverting amplifier is **Rify =R2+R3** -- eq(2)b
- Therefore from eqs 2a and 2b, it is obvious that the input resistances seen by the signal sources Vx and Vy are not the same.
- **Example:** In the circuit of figure 4-14, R1=R2=1KΩ, Rf=R3=10KΩ, and the op-amp is a 741C, a) what are the gain and input resistance of the amplifier?

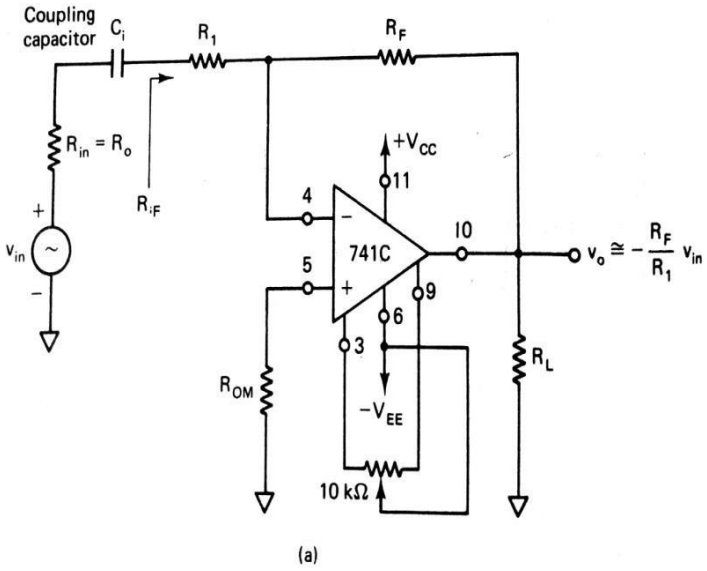
  (b) Calculate the output voltage Vo if Vx=2.7 Vpp and Vy= 3 Vpp sine waves at 100Hz.

  Solution: (a) Ad= -Rf/R1=-10KΩ/1KΩ = -10 Rifx = R1 = 1KΩ and Rify = R2 + R3 = 11KΩ

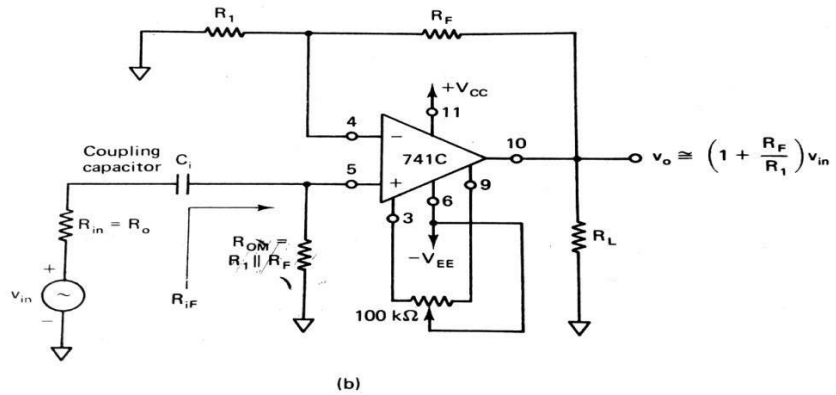
  (b) Output voltage Vo= Ad Vxy = Ad(Vx-Vy) = -10(2.7 – 3) = -10(-0.3) = 3 V peak to peak sine wave at 100Hz.

AC Amplifier

- If an AC input is riding on some DC level, it is necessary to use an AC amplifier with a coupling capacitor to block the DC amplification.
- For example, in an audio receiver system that consists of a number of stages, because of thermal drift, component tolerances, and variations the DC level is produced.
- To prevent the amplification of such DC levels, the coupling capacitors must be used between the stages.
- The figure 7-3 shows the AC inverting and non-inverting amplifiers with coupling capacitors.



(a)



(b)

Figure 7–3 (a) AC inverting amplifier. (b) AC noninverting amplifier. (Pin numbers are for the 14-pin DIP.)

- The coupling capacitor not only blocks the DC voltage but also set the low frequency cut off limit which is given by

  $f_L = 1/2\pi C_i(R_{if}+R_o)$

Derivation of fL:

- The input circuit of AC inverting amplifier of Figure 7-3a is drawn in figure C-1.

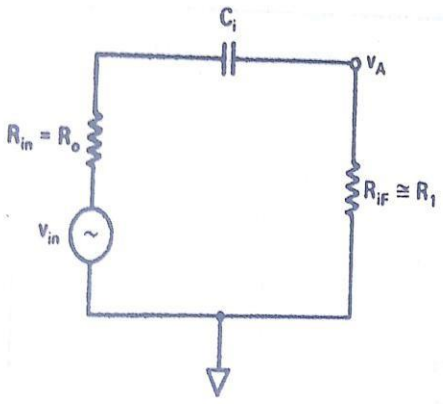


Figure C–1 Input circuit for the ac inverting amplifier of Figure 7-3(a).

- The voltage VA is amplified by the AC inverting amplifier, hence it is necessary to determine VA as a function of input voltage Vin
- Using voltage divider rule, we get

  $V_A = R_{if} V_{in}/(R_o + 1/jwC_i + R_{if})$ ----------eq(1)

  where Rif – input resistance of inverting amplifier

  Ro – Source resistance, Rin

Rearranging eq (1)

$V_A = j (R_{if} w C_i) V_{in}/j(R_{if} + R_o) w C_i + 1$

$= j (2\pi f C_i R_{if}) (V_{in}) / j ((2\pi f C_i)(R_{if}+R_o) + 1)$

$V_A = j(2\pi f C_i R_{if}) (V_{in})/(j(f/f_L)+1)$

where f – Input frequency (Hz)

$f_L = 1/2\pi C_i(R_{if} + R_o)$

where fL = low frequency cut-off or low end of bandwidth

Ci= DC blocking capacitor

Rif = AC input resistance of second stage

Ro = AC output resistance of 1st stage or Rin

- The high end of the bandwidth is given by

  fH = UGB (K)/ |Acl|

  where UGB – Unity gain bandwidth = 10^6

  K = 0.909 = Constant factor

  Acl = closed loop gain

Therefore bandwidth of the amplifier is

BW = fH – fL

- The Resistor Rom is used to minimize the effect of output offset voltage
- Since the reactance of Ci is negligible with in the bandwidth, the closed loop gain of the AC inverting amplifier is **Acl = -Rf/R1**
- And the closed loop gain of the AC non-inverting amplifier is

Acl = 1 + Rf/R1

Example : in the circuit of Fig 7.3(a) Rin=50Ω, Ci= 0.1 μF, R1=100 Ω, Rf= 1 KΩ, Rl=10KΩ and supply voltages=+ or – 15 V. Determine the bandwidth of the amplifier

Solution: Band width = fH – fL

where fH = (UGB) (K)/|Acl|

Acl = -Rf/R1 = - 1KΩ / 100 Ω = -10

therefore fH = 10^6(0.909)/10 = 90.9 KHz and

fL= 1/2πCi(Rif+Ro)

where Rif = input resistance of the inverting amplifier with feedback

Rif=R1=100Ω

Ro= Source resistance = Rin = 50 Ω

therefore fL= 1/2π (10^-7) (100+50) = 10.6 KHz

Therefore bandwidth = 90.9 KHz – 10.6 KHz = 80.3 KHz

Differentiator

- A differentiator is a circuit in which the output waveform is the derivative of input waveform. A differentiator circuit is shown in the figure 4.21(a).

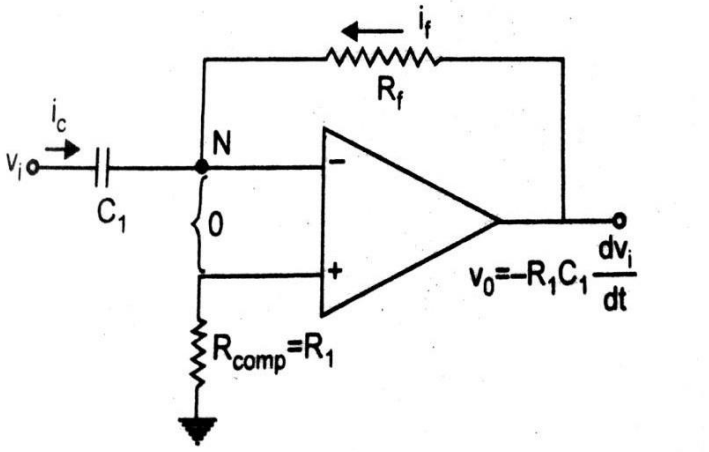


Fig. 4.21 (a) Op-amp differentiator

Analysis:

- The node N is at virtual ground potential ie Vn=0. The current ic through the capacitor is ic= C1 d(Vi-Vn)/dt = C1 dVi/dt
- The current If(not the English word if) through the feedback resistor = Vo/Rf and there is no current into the op-amp

Therefore nodal equation at node N is

C1 dVi/dt + Vo/Rf = 0

==> Vo= -Rf C1 dVi/dt --------- eq(1)

- The minus sign indicates a 180° phase shift of the output waveform Vo with respect to the input signal.

- The phasor equivalent of equation (1). is

  Vo(s) = - Rf C1 S Vi(s) where Vo & Vi are the phasor representation of vo & vi.

  In steady state put s=jw. Now the magnitude of gain A of the differentiator is

  |A| = |Vo/Vi| = |-jw Rf C1| = w Rf C1 ----- eq(2)

  Eq (2) may be written as

  |A| = f/fa where fa = 1/2π Rf C1

  At f = fa, |A| = 1 ie = 0 dB, and the gain increases at a rate of +20dB/decade.

  Thus at high frequency, a differentiator may become unstable and break into oscillations .

- There is one more problem in the Differentiator of figure 4.21(a).
- The input impedance (ie 1/wC1) decreases with increase in frequency there by making the circuit sensitive to high frequency noise.

Practical Differentiator:

- A practical differentiator of the type shown in Figure 4.21b eliminates the problem of stability and high frequency noise.

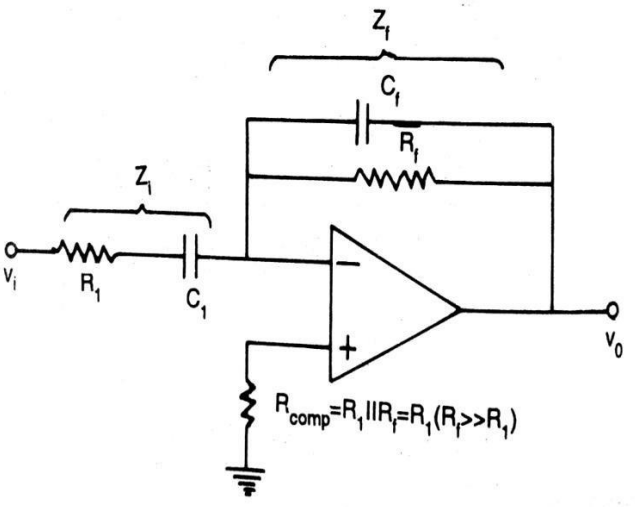


Fig. 4.21 (b) Practical differentiator

The transfer function for the circuit in Figure 4.21b is mentioned as

Vo(s)/Vi(s) = -Zf/Zi = -sRfC1/(1+ sRfCf)(1+sR1C1)

For RfCf = R1C1, we get

Vo(s)/Vi(s)= -sRfC1/(1+sR1C1)^2

=-sRfC1/(1+jf/fb)^2 ----- eq(3) where fb=1/2πR1C1

from eq(3), it is evident that the gain increases at + 20 dB/decade for frequency f < fb and decreases at -20 dB/decade for f > fb as shown by dashed lines in figure 4.21(c)

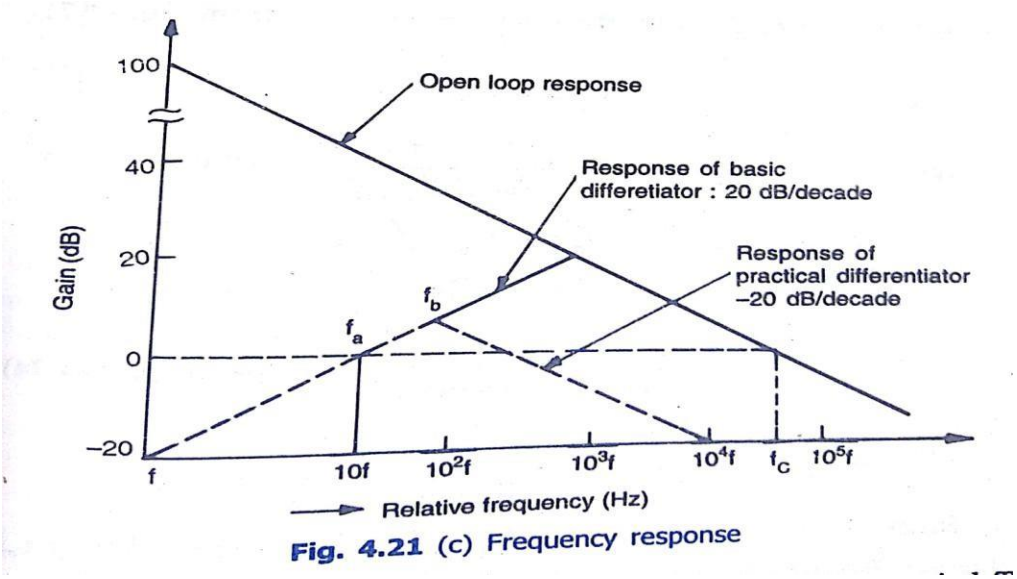


Fig. 4.21 (c) Frequency response

- This 40 dB/decade change in gain is caused by R1C1 and RfCf factors.
- For the basic differentiator of Fig.4.21(a) the frequency response would have increased continuously at the rate of +20dB/decade even beyond fb causing stability problem at high frequency.
- Thus the gain at high frequency is reduced significantly, thereby avoiding the high frequency noise and stability problems.
- The value of fb should be selected such that

  fa < fb < fc

  where fc is the unity bandwidth of the op-amp in open loop configuration.

- A resistance Rcomp is normally connected to the (+) input terminal to compensate for the input bias current.

A good differentiator may be designed as per the following steps.

1. Choose fa equal to the highest frequency of the input signal. Assume a practical value of C1 (< 1 μF) and then calculate Rf fa = 1/2π Rf C1
2. Choose fb = 10 fa (say). Now calculate the value of R1 from fb = 1/2π R1 C1 and Cf so that

R1C1 = RfCf

Example: (a) Design an op-amp differentiator that will differentiate an input signal with fmax = 100 Hz.

(b) Draw the output waveform for a sine wave of 1V peak at 100 Hz applied to the differentiator

(c) Repeat part (b) for a square wave input.

- **Solution:**

a) Select fa = fmax = 100 Hz = 1/2π Rf C1

let C1 = 0.1 μF

Then Rf = 1/2π(10^2)(10^-7) = 15.9 KΩ

Now choose fb = 10 fa = 10 (100 Hz) = 1 KHz

= 1/2π R1 C1

Therefore R1 = 1/2π (10^3)(10^-7) = 1.59 KΩ

since Rf Cf = R1 C1

We get Cf =1.59 (10^3) (10^-7)/15.9(10^3) = 0.01μF

(b) Vi = 1 sin 2π (100) t

from eq (1), Vo = -Rf C1 dVi/dt

Vo = -(15.9 KΩ) (0.1 μF) d[1 v sin 2π (10^2) t] /dt

= -(15.9 KΩ) (0.1 μF) 2π (10^2) cos[2π(100)t]

= - 0.999 cos[2π (100) t]

= - 1 cos[2π (100) t]

The input and output waveforms are shown in Figure 4.22

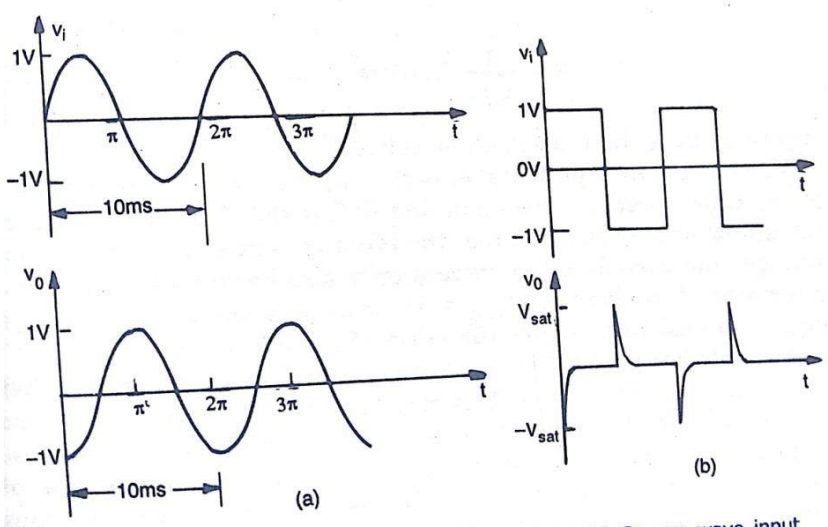


Fig. 4.22 (a) Sine-wave input and cosine output (b) Square wave input and spike output

Integrator

- By interchanging the resistor and capacitor of the Differentiator, we get the circuit of an integrator which is shown in the figure 4.23(a).

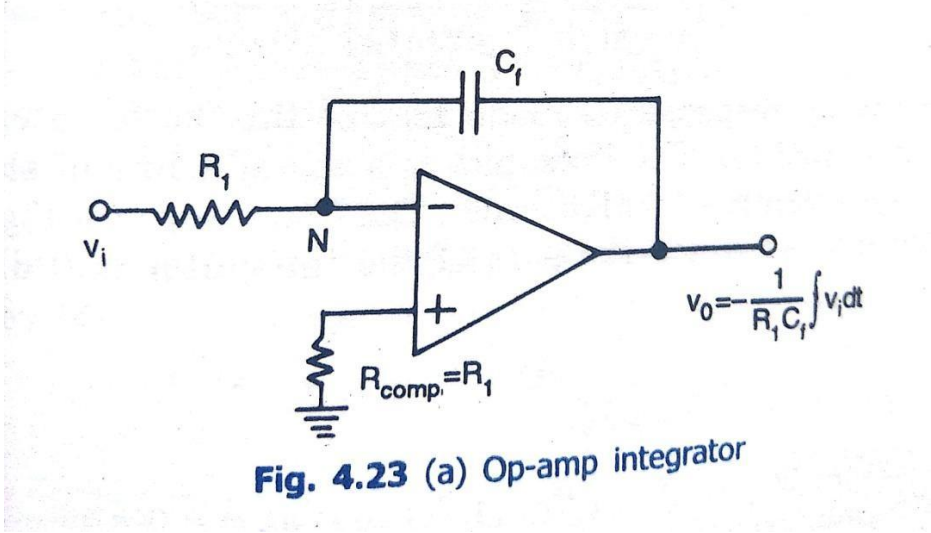


Fig. 4.23 (a) Op-amp integrator

- The nodal equation at node N is

$(Vi/R1) + Cf\, dVo/dt = 0$

➔ $dVo/dt = -(1/R1\, Cf)\, Vi$

➔ ${}_0\int^t dVo = (-1/R1Cf)\, {}_0\int^t Vidt$

$Vo(t) = (-1/R1Cf)\, {}_0\int^t Vi(t)dt + Vo(0)$------ eq(1)

where Vo(0) is the initial o/p voltage.

- Here R1Cf is the time constant of the integrator
- Here –ve sign is present, hence it is called inverting integrator.
- Rcomp is the resistor to minimize the effect of input bias current.
- The operation of the integrator can also be studied in the frequency domain. In phasor notation the equation (1) can be written as

  $Vo(s) = -(1/sR1Cf)\, Vi(s)$

  In steady state, put s=jw and we get

  $Vo(jw) = -(1/jwR1Cf)\, Vi(jw)$

- So the magnitude of the gain is

  $|A| = |Vo(jw)/Vi(jw)| = |-1/jwR1Cf|$

  $= 1/wR1Cf = 1/(f/fb)$

  Where $fb = 1/2\Pi\, R1Cf$

  The frequency response is shown in the figure 4.23b

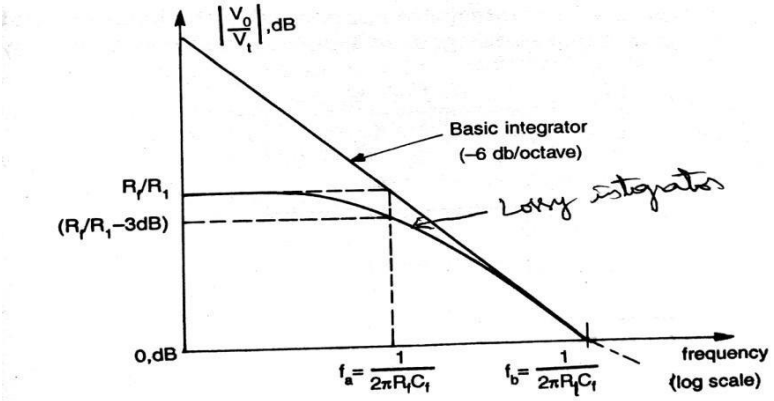


Fig. 4.23 (b) Frequency response of a basic and Lossy integrator

- The Bode plot of basic integrator is a straight line of slope -20 dB/decade.
- The frequency fb is the frequency at which the gain of the integrator is 0 dB and is given by

  fb = 1/2Π R1Cf

- As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in the differentiator. However, at low frequencies such as DC (w=0), the gain becomes infinite (ie saturates). The solution to this problem is a practical integrator circuit.

Practical Integrator Circuit (Lossy Integrator):

- The gain of an integrator at low frequency (DC) can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance Rf as shown in the Figure 4.23c

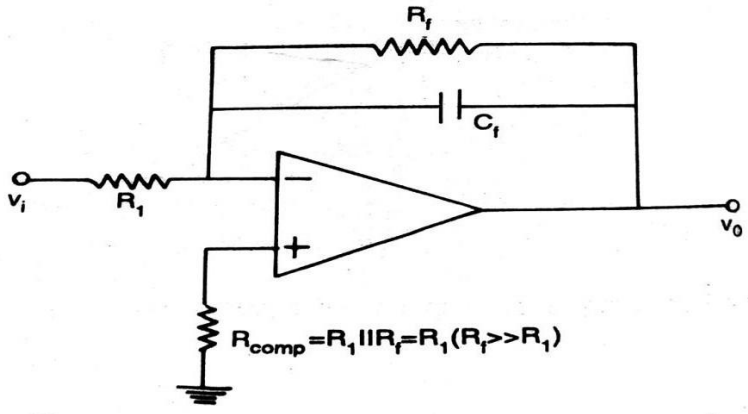


Fig. 4.23 (c) Practical or lossy integrator circuit

- The parallel combination of Rf and Cf behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason, this circuit is also called as a Lossy integrator.
- The resistor Rf limits the low frequency gain to –Rf/R1 (generally Rf = 10 R1) and thus provides DC stabilization.

Analysis:

- The nodal equation at the inverting input terminal of the op-amp is

$$(Vi(s)/R1) + sCf\ Vo(s) + (Vo(s)/Rf) = 0$$

From which we have

$$Vo(s) = -\ (1/(sR1Cf + R1/Rf))\ Vi(s)$$

- If Rf is large, the lossy integrator approximates the ideal integrator.
- For S=jw, the magnitude of the gain of Lossy integrator is given by

$$|A| = |Vo/Vi| = 1/(\sqrt{w2R1^2\ Cf^2 + R1^2/Rf^2})$$

$$= (Rf/R1)/(\sqrt{(1+(wRf\ Cf)^2)} \text{--------- eq(2)}$$

- The Bode plot of the Lossy Integrator is also shown in the Figure 4.23b. At low frequencies the gain is constant at Rf/R1.
- The break frequency (f = fa) at which the gain is 0.707 (Rf/R1) is calculated from eq(2) as

$$\sqrt{(1+ w\ Rf\ Cf)^2} = \sqrt{2}$$

$$\rightarrow wRf\ Cf = 1 \rightarrow f = 1/2\Pi Rf\ Cf$$

solving for f = fa, we get $fa = 1/2\ \Pi Rf\ Cf$

- This frequency tells us where the useful integration range starts in Figure 4.23b
- If the input frequency is lower than fa, the circuit acts like a simple inverting amplifier and no integration results.
- At the input frequency equal to fa, 50% accuracy results.
- The practical thumb rule is that if the input frequency is 10 times fa, then 99% accuracy can result.

Comparator

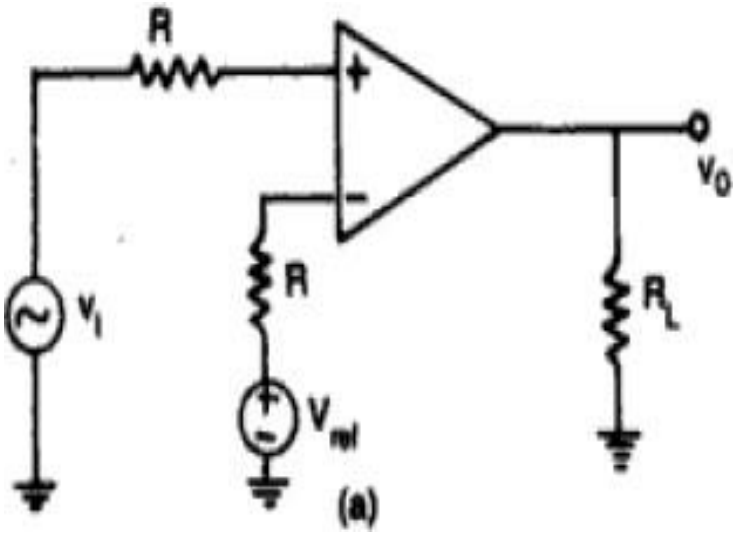
- A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input.
- There are basically two types of comparators.

1. Non-inverting comparator
2. Inverting comparator

Non-Inverting Comparator:

The circuit of figure 5.2a is called a non-inverting comparator.

- A fixed reference voltage Vref is applied to – input and a time varying signal Vi is applied to +input.
- There are 3 conditions for a comparator. They are Vi < Vref → Vo = -Vsat
- Vi > Vref → Vo = +Vsat
- Vi = Vref → changes the state of op-amp
- The output waveform for a sinusoidal input signal applied to the +ve input is shown in figure 5.2 (b) and (c) for +ve and –ve Vref respectively.



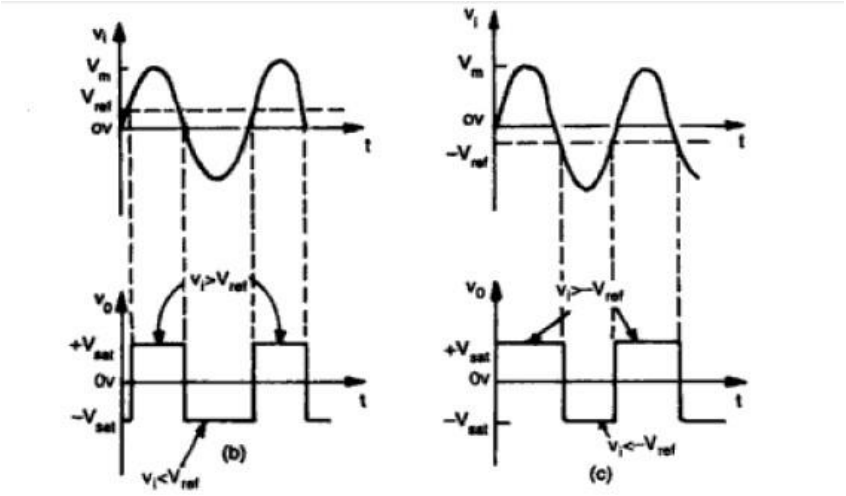
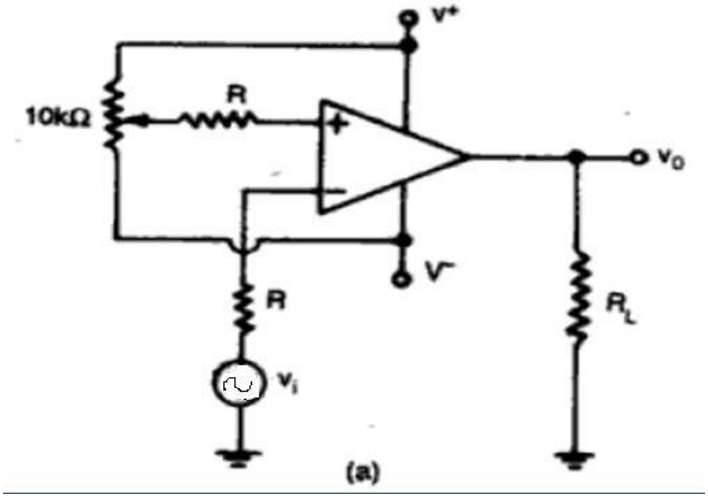


Fig. 5.2 (a) Non-inverting comparator. Input and output waveforms for (b) V_{ref} positive (c) V_{ref} negative

Inverting Comparator:

- Figure 5.3(a) shows a practical inverting comparator in which the reference voltage Vref is applied to the +input and Vi is applied to the –ve input.
- For a sinusoidal input signal, the output waveform is shown in figure 5.3(b) and 5.3(c) for Vref +ve and –ve respectively.



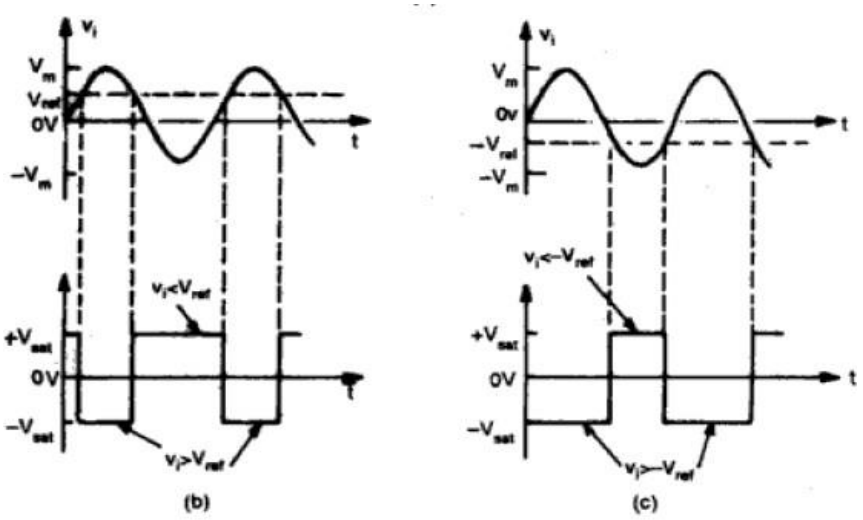


Fig. 5.3 (a) Inverting comparator. Input and output waveforms (b) $V_{ref} > 0$ (c) $V_{ref} < 0$

Applications of Comparator

- Some important applications of comparator are
  - Zero crossing detector
  - Window detector
  - Time marker generator
  - Phase meter.

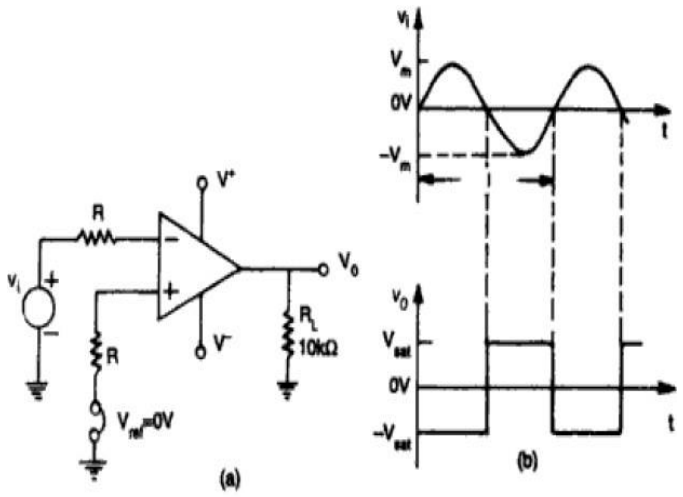


Fig. 5.4 (a) Zero crossing detector (b) Input and output waveforms

- The basic comparators either non-inverting or inverting can be used as a zero crossing detector provided that Vref is set to zero. An inverting zero-crossing detector is shown in figure 5.4 (a).
- The input and output waveforms are shown in Figure 5.4 (b).
- The circuit is also called as a sine to square wave generator.

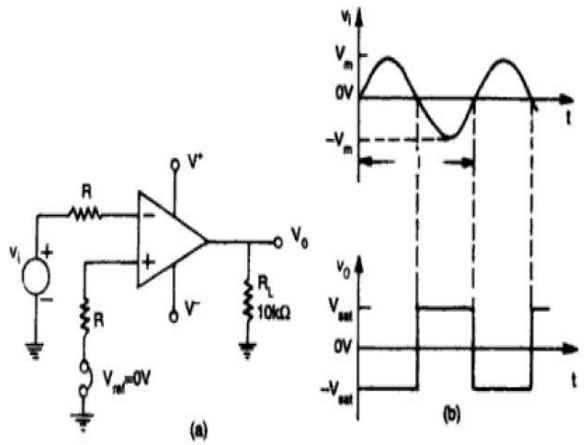


Fig. 5.4 (a) Zero crossing detector (b) Input and output waveforms

- The basic comparators either non-inverting or inverting can be used as a zero crossing detector provided that Vref is set to zero. An inverting zero-crossing detector is shown in figure 5.4 (a).
- The input and output waveforms are shown in Figure 5.4 (b).
- The circuit is also called as a sine to square wave generator.

Regenerative Comparator (Schmitt Trigger)

- If positive feedback is added to the comparator circuit, gain can be increased greatly.
- Figure 5.8 (a) shows a regenerative comparator. The circuit is also known as Schmitt trigger

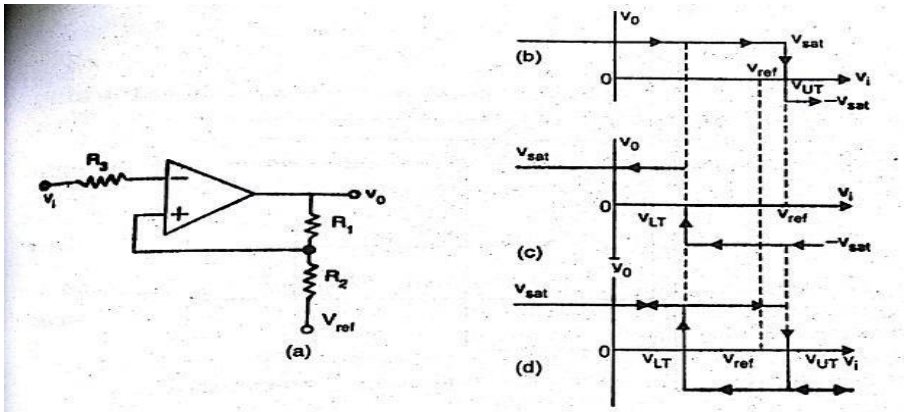


Fig. 5.8 (a) An inverting Schmitt trigger (b, c) Transfer characteristics for V_i increasing and V_i decreasing (d) composite input-output curve

- The input voltage Vi triggers the output Vo every time it crosses certain voltage levels. These voltage levels are called Upper threshold voltage (Vut) and Lower threshold voltage (Vlt).
- The hysteresis width is the difference between these two threshold voltages ie Vut – Vlt. These threshold voltages are calculated as follows.
- Suppose that the output voltage Vo is +Vsat. The voltage at +ve input terminal will be

  Vref + (R2/(R1+R2)) (Vsat – Vref) = Vut
- This voltage is called as Upper threshold voltage Vut

- As long as Vi is less than Vut, the output Vo remains constant at +Vsat. When Vi is just greater than Vut, the output regeneratively switches to – Vsat and remains at this level as long as Vi > Vut as shown in Figure 5.8 (b).
- For Vo = -Vsat, the voltage at +ve input terminal is

  Vref + (R2/R1+R2) (-Vsat – Vref) = Vlt

  Vref - (R2/R1+R2) (Vsat + Vref) = Vlt

  this voltage is referred to as lower threshold voltage Vlt
- The input voltage Vi must become lesser than Vlt in order to cause Vo to switch from – Vsat to +Vsat. A regenerative transition takes place as shown in Figure 5.8(c) and the output Vo returns from –Vsat to +Vsat almost instantaneously.
- The complete transfer characteristics are shown in Figure 5.8 (d).
- Note that Vlt < Vut and the difference between these two voltages is the hysteresis width Vh and can be written as

  Vh = Vut – Vlt = 2R2 Vsat/(R1+R2)
- The resistor R3 in figure 5.8(a) is chosen equal to R1||R2 to compensate for the input bias current.
- A non-inverting Schmitt trigger is obtained if Vi and Vref are interchanged in figure 5.8(a).

Voltage Regulators

- A voltage regulator is a circuit that supplies constant voltage regardless of changes in load currents
- Although voltage regulators can be designed using op-amps, it is quicker and easier to use IC voltage regulators.
- Furthermore, IC voltage regulators are versatile and relatively inexpensive and are available with features such as programmable output, current/voltage boosting, internal short-circuit current limiting, thermal shutdown and floating operation for high voltage applications.
- IC voltage regulators are of the following types
    - Fixed output voltage regulators: +ve and/or –ve output voltage
    - Adjustable output voltage regulators: +ve or –ve output voltage
    - Switching regulators
    - Special regulators
- Except for the switching regulators, all other types of regulators are called LINEAR regulators.
- The impedance of a linear regulator's active element may be continuously varied to supply a desired current to the load.
- On the other hand, in the switching regulator a switch is turned on and off at a rate such that the regulator delivers the desired average current in periodic pulses to the load.
- Because the switching element dissipates negligible power in either the ON or OFF state, the switching regulator is more efficient than the linear regulator.
- Nevertheless, in switching regulators the power dissipation is substantial during the switching intervals (ON to OFF or OFF to ON). In addition, most loads can not accept the average current in periodic pulses. Therefore, most practical regulators are of the linear type.
- Voltage regulators are commonly used for laboratory-type power supplies.

- Almost all power supplies use some type of voltage regulator IC because voltage regulators are simple to use, reliable, low in cost, and, above all, available in a variety of voltage and current ratings.

Performance Parameters

There are four typical performance parameters

for voltage regulators. They are LINE regulation,

LOAD regulation, temperature stability and

ripple rejection.

- **LINE or INPUT regulation:** it is defined as the change in output voltage for a change in the input voltage and is usually expressed in milli volts or as a percentage of output voltage Vo.
- **LOAD Regulation:** It is the change in output voltage for a change in load current and is also expressed in milli volts or as a percentage of Vo
- **Temperature stability:** It is the change in output voltage per unit change in the temperature and is expressed in either milli volts/°C or parts per million (ppm)/°C
- **Ripple Rejection:** it is the measure of a regulator's ability to reject ripple voltages. It is usually expressed in decibels.

  The smaller the values of line regulation, load regulation and the temperature stability, the better the regulator.
- **Dropout Voltage:** It is the difference between input and output voltages.

Types of Voltage Regulators

- **Fixed Output Voltage Regulators:**
  - **Positive Output voltage regulator series:**

Device Type	O/P Voltage (Volts)	Max .Input Voltage (Volts)
7805	5.0	35
7806	6.0	35
7808	8.0	35
7812	12.0	35
7815	15.0	35
7818	18.0	35
7824	24.0	40

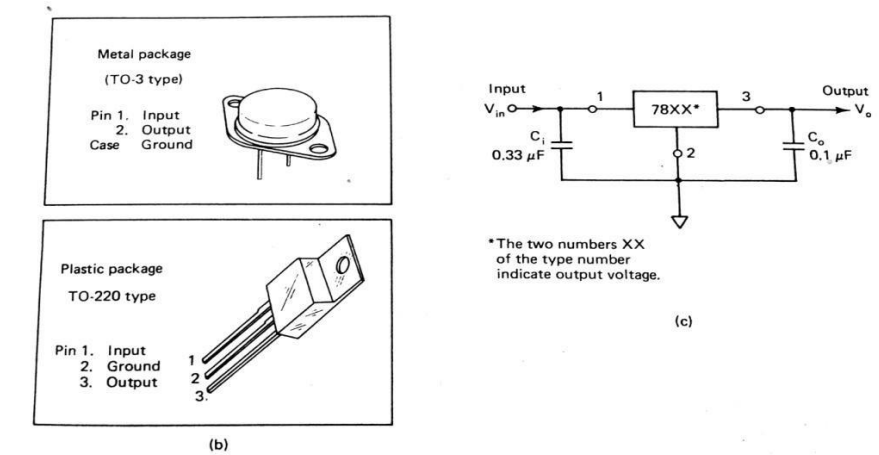


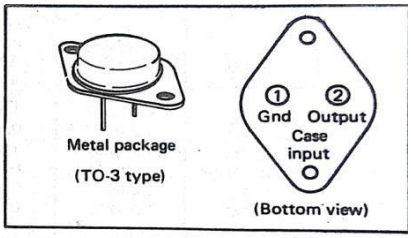
Figure 10–43 The 7800 series regulators. (a) Voltage options. (b) Package types. (c) Standard application. (Courtesy of Motorola Semiconductor.)

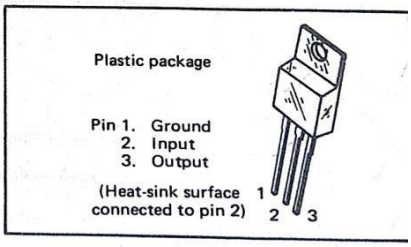
- **Negative Output voltage regulator series:**

Device Type	O/P Voltage (Volts)	Max .Input Voltage (Volts)
7902	-2.0	-35
7905	-5.0	-35
7905.2	-5.2	-35
7906	-6.0	-35
7908	-8.0	-35
7912	-12.0	-35
7915	-15.0	-35
7918	-18.0	-35
7924	-24.0	-40

Device type	Output voltage (V)	Maximum input voltage (V)
7902	−2.0	−35
7905	−5.0	
7905.2	−5.2	
7906	−6.0	
7908	−8.0	
7912	−12.0	
7915	−15.0	
7918	−18.0	
7924	−24.0	−40

(a)





(b)

Figure 10–45 The 7900 series voltage regulators. (a) Voltage options. (b) Package types. (Courtesy of Motorola Semiconductor.)

Adjustable Output Voltage Regulators:

- In the case of fixed voltage regulators, for each voltage a separate device is to be used. This increases the inventory and hence the cost.
- Therefore, Adjustable voltage regulators came into picture. These regulators provide many voltages ranging from 1.2 to 57 volts.
- In addition, these have more versatility, more performance and more reliability than fixed voltage regulators.
- Adjustable +ve Voltage Regulators – LM317 and Adjustable –ve Voltage Regulators – LM337

Switching Regulators:

- Switching regulators are called so because these use a switch in the circuit.
- Switching regulators come in various circuit configurations including the Fly-back, Feed-forward, Push-pull, and non-isolated single-ended or single-polarity types.
- Switching regulators can operate in any of three modes: Step-up, step-down or polarity inverting.
- Switching regulator is often referred to as a DC transformer.
- Eg: IC μA78S40 from Fairchild.

Special Regulators:

- It is used as
  - Voltage References: It is used as a reference voltage in A/D and D/A converters
  - Voltage Inverter: It is used in Data Acquisition and Microprocessor-based systems in which a +ve supply is available and an additional –ve supply is required.

IC 723 Regulator and It's Features

- 3 terminal voltage regulators are capable of producing only fixed +ve or –ve output voltages. Moreover, such regulators do not have short circuit protection.
- Therefore these 3 terminal regulators evolved into dual polarity variable voltage regulators and further evolved into the monolithic linear voltage regulators and monolithic switching regulators.
- One example for monolithic linear voltage regulator is IC723.
- IC723 general purpose regulator overcomes the limitations of 3 terminal fixed voltage regulators
- IC723 is a low current device.
- 150 mA o/p current without external pass transistor.
- o/p currents in excess of 10A possible by adding external transistors
- Input voltage 40 V maximum.
- O/p voltage adjustable from 2V to 37 V.
- Can be used as either a linear or a switching regulator.

Limitations: it has no built-in thermal protection.

End of Unit I

Unit 2

Op-Amp, IC-555 & IC565Applications

Introduction to Filters

- Based on the components used in the circuit the filters are divided into following categories.
  - Active filters
  - Passive filters

Active Filters:

- Active filters employ transistors or op-amps in addition to resistors and capacitors.

Passive Filters:

- Here the type of element used dictates the operating frequency range of the filter.

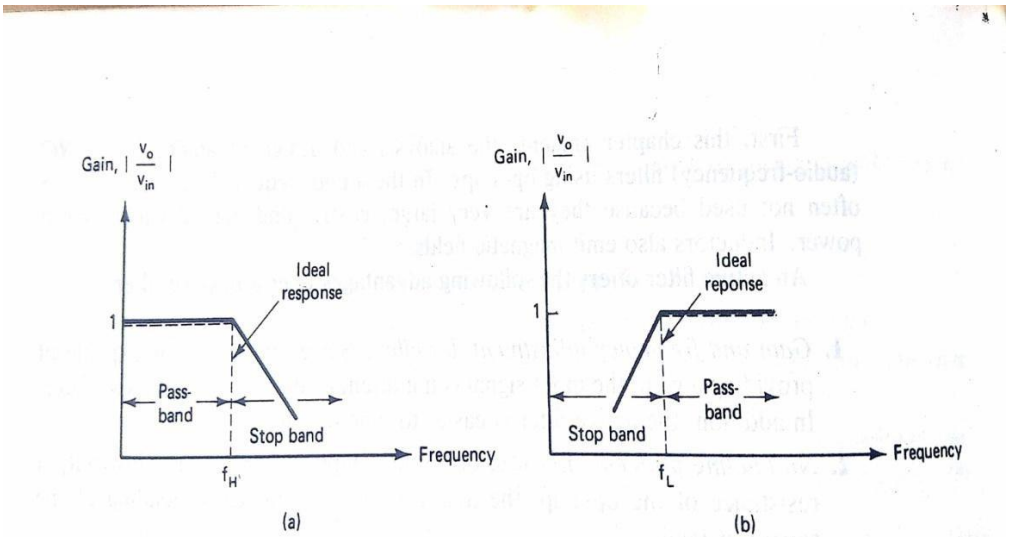
Eg:

- RC filters are used for audio or low frequency operation.
- LC or Crystal filters are used at RF or High frequencies.

An active filter offers the following advantages over a Passive filter.

- **Gain and Frequency adjustment flexibility:** Since the op-amp is capable of providing a gain, the input signal is not attenuated as it is in a passive filter. In addition, the active filter is easier to tune or adjust.
- **No Loading problem:** Because of the high input resistance and low output resistance of the op-amp, the active filter does not cause loading of the source or load.
- **Cost:** Typically, active filters are more economical than passive filters. This is because of the variety of cheaper op-amps and the absence of the inductors.
- Although active filters are most extensively used in the field of Communications and Signal processing, they are employed in one form or another in almost all sophisticated electronic systems.

- The different systems that use Active filters are Radio, television, telephone, Radar, Space satellites, and bio-medical equipment.
- Based on the operating frequency the filters are classified as follows.
  - Low pass filter
  - High pass filter
  - Band pass filter
  - Band stop filter
  - All pass filter
- Each of these filters uses an op-amp as an active element and resistors and capacitors as passive elements.
- Figure 8.1 shows the frequency response characteristics of the five types of filters.



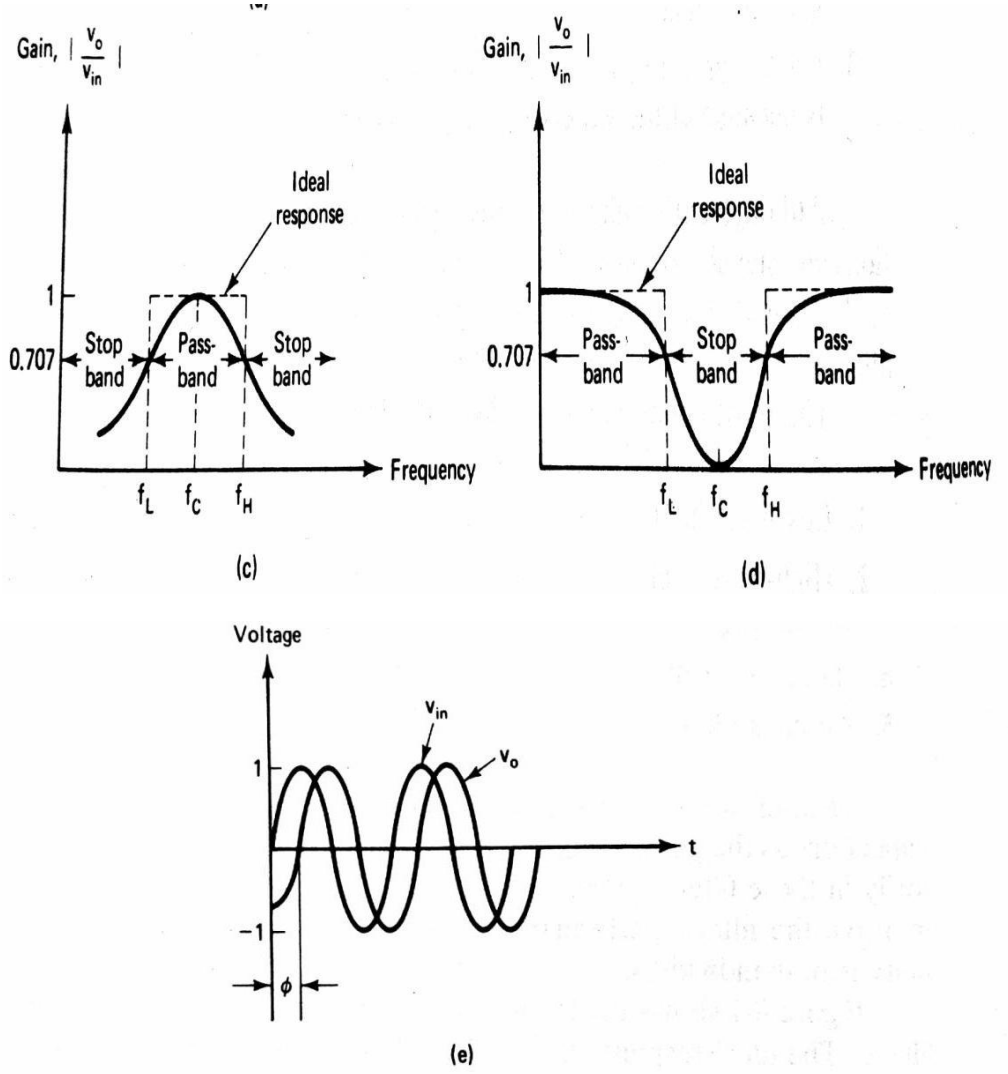


Figure 8–1 Frequency response of the major active filters. (a) Low pass. (b) High pass. (c) Band pass. (d) Band reject. (e) Phase shift between input and output voltages of an all-pass filter.

- Figure 8-1(a) shows the frequency response of low pass filter. As indicated by dashed line, an ideal filter has a zero loss in its pass band and infinite loss in its stop band
- Unfortunately, ideal filter response is not practical. However, it is possible to obtain a practical response that approximates the ideal filter response by using special design techniques as well as precision component values and high speed op-amps.
- Butterworth, chebyshev and caver filters are some of the most commonly used practical filters that approximate the ideal response.

- The key characteristics of Butterworth filters is that it has a flat pass band as well as stop band. For this reason, it is sometimes called a flat-flat filter.
- Figure 8-1(b) shows a high pass filter with a stop band $0 < f < fL$ and pass band $f > fL$.
- A band pass filter has a pass band between two cut-off frequencies fH and fL, where $fH > fL$ and two stop bands $0<f<fL$ and $f>fH$.

  Band width of the band pass filter – fH-fL.
- The band reject filter performs exactly opposite to the band pass, ie it has a band stop between two cut off frequencies fH and fL and two pass bands $0<f<fL$ and $f>fH$.
- The band reject filter is also called as band stop or band elimination filter
- Figure 8-1(e) shows the phase shift between input and output voltages of an all pass filter. This filter passes all frequencies equally well ie input and output voltages are equal in amplitude for all frequencies, with the phase shift between the two a function of frequency.
- As shown in figure 8-1 (a) – (d), the actual response curves of the filters in the stop band either steadily decrease or increase or both with increase in frequency.
- The rate at which the gain of the filter changes in the stop band is determined by the order of the filter.
- For first order low pass filter, gain decreases by 20 dB/decade in the stop band.
- For second order low pass filter, gain decreases by 40 dB/decade in the stop band.
- By contrast, for first order high pass filter, gain increases by 20 dB/decade in the stop band.
- For second order high pass filter, gain increases by 40 dB/decade.

First Order Low pass Butterworth filter

- Figure 8-2 shows a first order low pass Butter worth filter that uses an RC network for filtering. Note that the op-amp is used in the non-inverting configuration, hence it does not load down the RC network. Resistors R1 and Rf determine the gain of the filter.

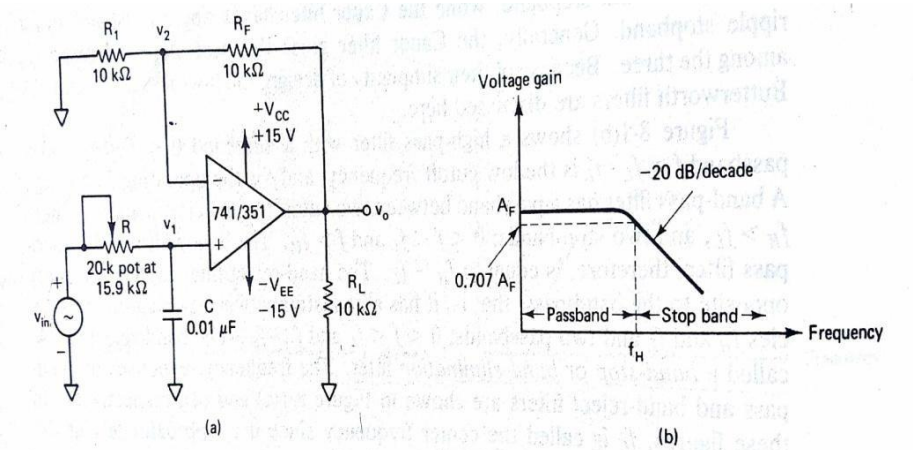


Figure 8–2 First-order low-pass Butterworth filter. (a) Circuit. (b) Frequency response.

- According to the voltage divider rule, the voltage at the non-inverting terminal (across capacitor C) is

  V1 = -jXc/(R-jXc) Vin ---------- eq(1)

  where j=√-1 and –jXc = 1/j2ΠfC

  simplifying eq(1), we get

  V1 = Vin / 1+ j2ΠfRC

  Output voltage Vo= (1 + (Rf/R1)) V1

  ie Vo = (1+(Rf/R1)) (Vin/(1+j2ΠfRC))

Vo/Vin = Af/(1+j (f/fH)) ---------eq(2)

where Vo/Vin = gain of the filter as a function of frequency.

Af= 1+ (Rf/R1) = pass band gain of the filter

f = frequency of the input signal

fH = 1/2ΠRC = high cutoff frequency of the filter.

- The gain magnitude and phase angle equations of the low pass filter can be obtained by converting eq(2) into it's equivalent polar form, as follows.

|Vo/Vin| = Af/√(1+(f/fH)^2) ------eq(3)

ϕ = - tan^-1(f/fH)

Where ϕ is the phase angle in degrees

- The operation of the low pass filter can be verified from the gain magnitude equation (3).
- At very low frequencies, that is, f<fH

  |Vo/Vin| = Af
- At f = fH, |Vo/Vin| = 0.707 Af
- At f>fH, |Vo/Vin| < Af
- Thus the low pass filter has a constant gain Af from 0 Hz to the almost high cutoff frequency fH
- At fH, the gain is 0.707 Af, and after fH it decreases at a constant rate with as increase in frequency [see fig 8-2 b]
- The frequency f =fH is called the cutoff frequency because the gain of the filter at this frequency is down by 3 dB from 0 Hz.
- Other equivalent terms for cut off frequency are -3dB frequency, break frequency or corner frequency.

Filter Design

A low pass filter can be designed by implementing the following steps

1 Choose a value of high cut off frequency fH

2 Select a value of C less than or equal to 1 µF

(Mylar or tantalum capacitors are recommended for better performance)

3 Calculate the value of R using R = 1/2Π fH C

4 Finally, select values of R1 and Rf dependant on the desired pass band gain Af using

Af = 1+ (Rf/R1)

Example 1: Design a low pass filter at a cut off frequency of 1 KHz with a pass band gain of 2

Solution:

Follow the preceding design steps

1 fH = 1 KHz

2 Let C = 0.01 µF

3 Then R = 1/2 Π (10^3) (10^-8) = 15.9 KΩ (use a 20 KΩ pot.)

4 Since the pass band gain is 2, R1 and Rf must be equal. Therefore, let R1 = Rf = 10 KΩ

The complete circuit with components values is shown in Fig 8-2 a.

- Once a filter is designed there may sometimes be a need to change its cut off frequency. The procedure used to convert an original cut off frequency fH to a new cut off frequency fH1 is called frequency scaling.
- Frequency scaling is accomplished as follows
- To change a high cut off frequency, multiply R or C but not both, by the ratio of original cut off frequency to new cut off frequency.

Example 2:

Using the frequency scaling technique, convert 1 KHz cut off frequency of the low pass filter of Example 1 to a new cut off frequency of 1.6 KHz

Solution: To change a cut off frequency from 1 KHz to 1.6 KHz, we multiply the 15.9 KΩ resistor by

Original cut off frequency/new cut off frequency = 1 KHz/1.6 KHz = 0.625

Therefore, new resistor R = 15.9 KΩ * 0.625 = 9.94 KΩ

However, 9.94 KΩ is not a standard value.

Therefore, use R= 10KΩ potentiometer and adjust it to 9.94 KΩ.

Thus the new cut off frequency is

fH1 = 1/ 2Π (0.01 µF) (9.94 KΩ) = 1.6 KHz.

First Order High Pass Butterworth filter

- High pass filters are often formed simply by interchanging the frequency-determining resistors and capacitors in low pass filters.
- That is, a first order high pass filter is formed from a first order low pass type by interchanging components R & C.
- Figure 8.6 shows a first order high pass Butter worth filter with a low cut off frequency of fL. This is the frequency at which the magnitude of the gain is 0.707 times its pass band value.

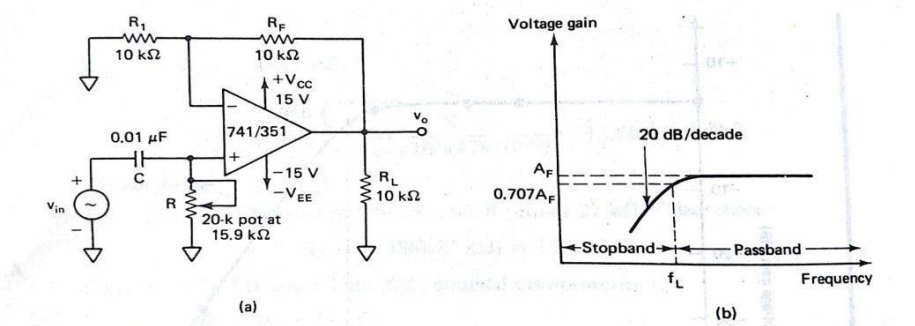


Figure 8–6 (a) First-order high-pass Butterworth filter. (b) Its frequency response.

- Obviously all frequencies higher than fL are pass band frequencies, with the highest frequency determined by the closed loop band width of the op-amp.
- For the first order high pass filter of Figure 8.6a, the output voltage is

$$V_o = (1+(R_f/R_1))\ (j2\Pi fRC/(1+j2\Pi fRC))\ V_{in}$$

$$V_o/V_{in} = A_f[j(f/f_L)/(1+j(f/f_L))$$

where $A_f = 1+(R_f/R_1)$, & $f_L = 1/2\Pi RC$

Hence the magnitude of the voltage gain is

$$|V_o/V_{in}| = A_f\ (f/f_L)/\sqrt{(1+(f/f_L)^2)}$$

- Since the high pass filters are formed from low pass filters simply by interchanging Rs and Cs, the design and frequency scaling procedures of the low pass filters are also applicable to high pass filters.

Wave form Generators

There are different types of wave form generators which are given below.

1 Square wave generator

2 Triangular wave generator

3 Saw tooth wave generator

Square wave Generator (Astable Multivibrator)

- A simple op-amp square wave generator is shown in Figure 5.10a.

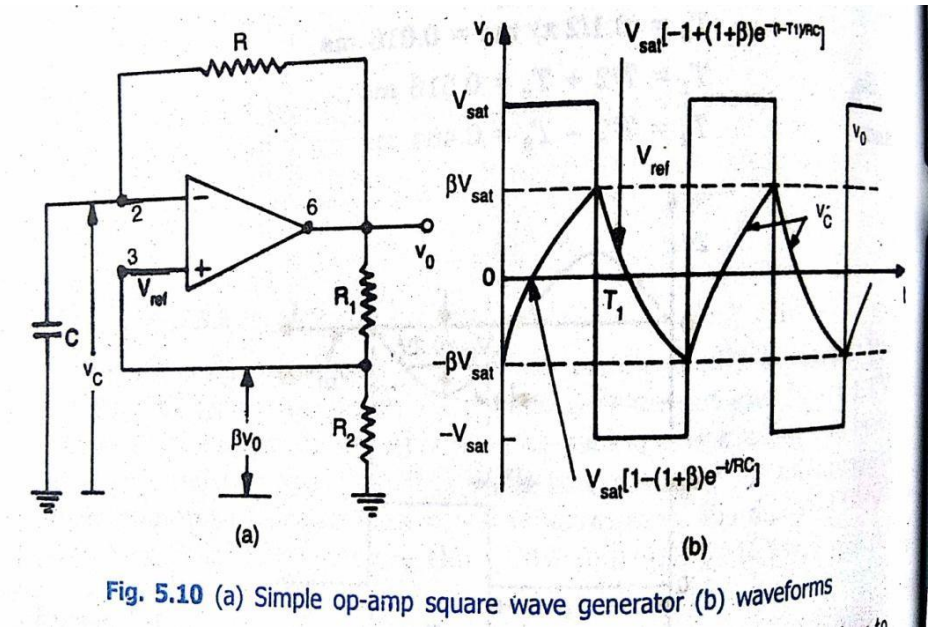


Fig. 5.10 (a) Simple op-amp square wave generator (b) waveforms

- It is also called a Free running oscillator.
- The principle of generation of square wave output is to force an op-amp to operate in saturation region.
- In Figure 5.10(a), fraction β = R2/(R1+R2) of the output is fed back to the +ve input terminal. Thus the reference voltage Vref is βVo and may take values as +βVsat or –βVsat.
- The output is also fed back to the –ve input terminal after integrating by means of a low pass RC combination.

- Whenever input at the –ve input terminal just exceeds Vref, switching takes place resulting in a square wave output.
- In Astable multivibrator, both the states are quasi stable.

Frequency Derivation

- The frequency is determined by the time it takes the capacitor to charge from –βVsat to + βVsat and vice versa.
- The voltage across the capacitor as a function of time is given by

  $Vc(t) = Vf + (Vi – Vf)\ e^{-t/RC}$

  where, the final value, $Vf = +Vsat$

  and the initial value, $Vi = –\beta Vsat$

  Therefore $Vc(t) = +Vsat + (–\beta Vsat – Vsat)\ e^{-t/RC}$

  $Vc(t) = Vsat – Vsat(1+\beta)\ e^{-t/RC}$

  At t = T1, voltage across the capacitor reaches βVsat and switching takes place.
- Therefore

  $Vc(T1) = \beta Vsat = Vsat – Vsat(1+ \beta)\ e^{-T1/RC}$

  After algebraic manipulation, we get

  $T1 = RC \ln (1+ \beta)/(1- \beta)$

This gives only one half of the period.

Therefore the total time period, $T = 2*T1 = 2RC \ln (1+ \beta)/(1- \beta)$ and the output waveform is symmetrical.

If R1 = R2, then β = 0.5 and $T = 2RC \ln 3$ and

for R1=1.16 R2, it can be seen that

$T = 2RC$ or $fo = 1/2RC$

Triangle Wave Generators

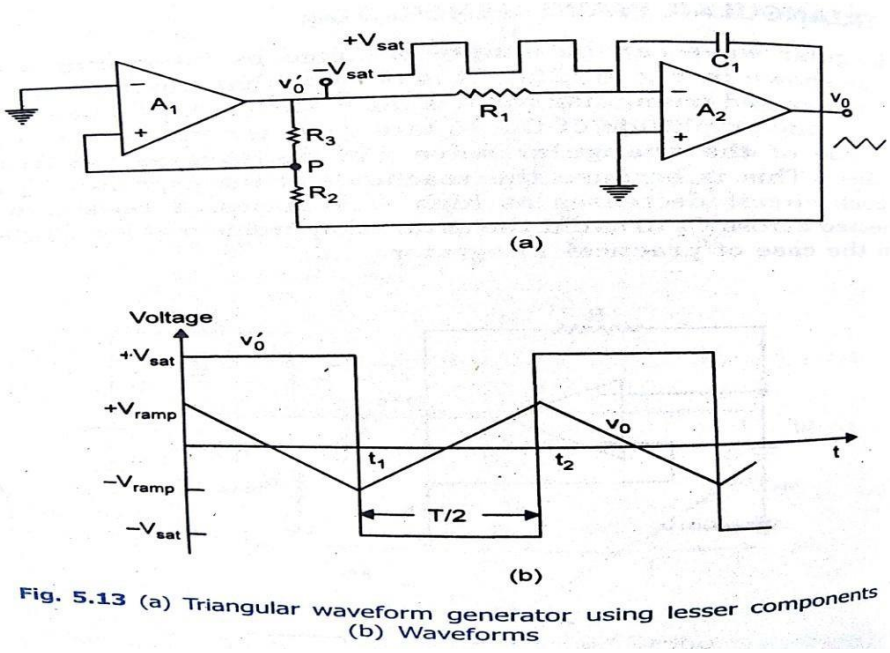


Fig. 5.13 (a) Triangular waveform generator using lesser components (b) Waveforms

- It basically consists of a two level comparator followed by an integrator.
- The output of the comparator A1 is a square wave of amplitude + or – Vsat and is applied to the –ve input terminal of the integrator A2 producing a triangular wave. This triangular wave is fed back as input to the comparator A1 through a voltage divider R2R3.
- Initially, let us consider that the output of the comparator A1 is at +Vsat. The output of the integrator A2 will be a –ve going ramp as shown in figure 5.13b. This one end of the voltage divider R2R3 is at a voltage +Vsat and the other at the –ve going ramp of A2.
- At a time t=t1, when the –ve going ramp attains a value of –Vramp, the effective voltage at point p becomes slightly less than 0 volts. This switches the output of A1, from positive saturation level to negative saturation level – Vsat.
- During the time when the output of A1 is at -Vsat, the output of A2 increases in the positive direction.
- And at the instant t=t2, the voltage at point p becomes just above 0 volts, thereby switching the output of A1 from –Vsat to +Vsat. The cycle repeats and generates a triangular waveform.

- It can be seen that the frequency of the square wave and triangular wave will be the same.
- However, the amplitude of the triangular wave depends upon the RC value of the integrator A2 and output voltage level of A1.

Derivation of Frequency of Triangular Waveform

- The effective voltage at point p during the time when output of A1 is at +Vsat level is given by

$-V_{ramp}+(R2/(R2+R3))\ [+V_{sat} – (-V_{ramp})]$ -- Eq(1)

At t=t1, the voltage at point p becomes approximately equal to zero. Therefore from Eq(1), we get $-V_{ramp} = (-R2/R3)\ (+V_{sat})$

Similarly at t=t2, when the output of A1 switches from –Vsat to +Vsat

$V_{ramp} = (-R2/R3)\ (-V_{sat}) = (R2/R3)\ V_{sat}$

Therefore peak to peak amplitude of the triangular wave is

$V_{o(pp)} = +V_{ramp} – (-V_{ramp})$

$V_{o(pp)} = 2\ V_{ramp} = 2\ (R2/R3)\ V_{sat}$ ----- Eq(2)

The output switches from –Vramp to +Vramp in half the time period T/2.

Putting the values in the basic integrator equation $V_o = -(1/RC) \int V_i\, dt$, we get

$V_{o(pp)}=-(1/R1C1)\ 0\int^{T/2} (-V_{sat})dt =(V_{sat}/R1C1)\ (T/2)$

Therefore $T=2\ R1C1\ V_{o(pp)}/V_{sat}$

Putting the value of $V_{o(pp)}$ from Eq(2), we get

$$T = 4R1\ C1\ R2/R3$$

Hence the frequency of oscillation fo is

$$f_o = 1/T = R3/4\ R1\ C1\ R2$$

Sawtooth Wave Generator

- The difference between the triangular and sawtooth waveforms is that

rise time and fall time are equal – Triangular

rise time and fall time are unequal – Sawtooth

- The triangular wave generator can be converted into a sawtooth wave generator by injecting a variable DC voltage into the non-inverting terminal of the integrator A2.

- This can be accomplished by using the potentiometer and connecting it to the +Vcc and -Vee as shown in Figure 8-24(a)

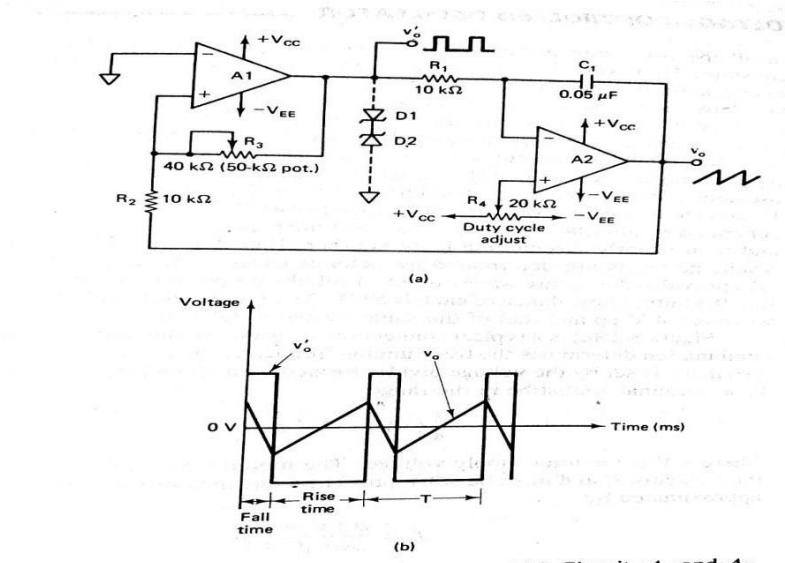


Figure 8–24 Sawtooth wave generator. (a) Circuit. A_1 and A_2 dual op-amp: 1458/353. D_1 and D_2: IN4735 with $V_Z = 6.2$ V. (b) Output waveform when noninverting input of A_2 is at some negative dc level.

- Depending on the R4 setting, a certain DC level is inserted in the output of A2.

- Now suppose that the output of A1 is a square wave and the potentiometer R4 is adjusted for a certain DC level.

- This means that the output of A2 will be a triangular wave, riding on some DC level that is a function of the R4 setting.

- The duty cycle of the square wave will be determined by the polarity and amplitude of this DC level.

- A duty cycle less than 50% will then cause the output of A2 to be a sawtooth.

- With the wiper at the center of R4, the output of A2 is a triangular wave. For any other position of R4 wiper, the output is a sawtooth waveform.
- R4 wiper is towards **–Vee**,the **rise time is more**
- R4 wiper is towards **+Vcc**,the **fall time is more**

Introduction to IC 555 Timer

- The 555 timer is a highly stable device for generating accurate time delay or oscillation.
- Signetics corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8 pin circular type, To-99 can or 8-pin mini DIP or as 14–pin DIP.
- A single 555 timer can provide time delay ranging from µsec to hours.
- The 555 timer can be used with supply voltage in the range of +5 Volts to +18 volts and can drive load upto 200mA.
- It is compatible with both TTL and CMOS logics.

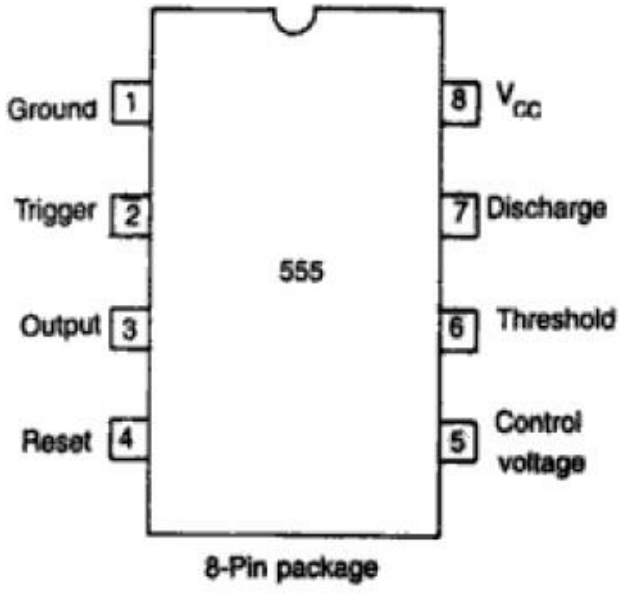


Fig. 8.1 Pin diagram

- Because of wide range of supply voltage, the 555 timer is versatile & easy to use in various applications.
- Various applications include oscillators, pulse generator, ramp & square wave generator, mono shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

Functional Diagram of 555 Timer

- Figure 8.2 gives the functional diagram for 555 IC timer.

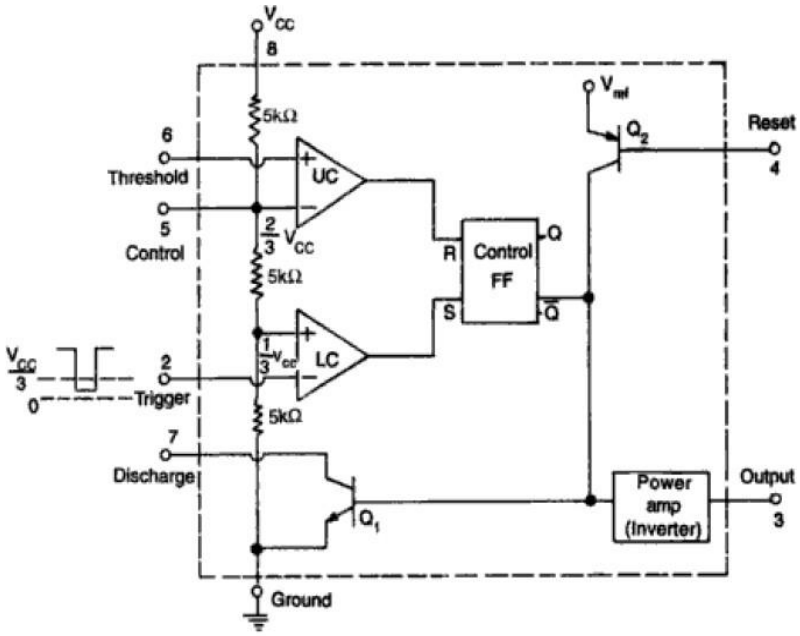


Fig. 8.2 Functional diagram of 555 timer

- Referring to Figure 8.2, 3 5KΩ internal resistors act as voltage divider, providing bias voltage of 2/3 Vcc to the upper comparator (UC), and 1/3 Vcc to the lower comparator (LC) where Vcc is the supply voltage.
- In the stand by(stable) state, the output Q of control filp-flop(FF) is high.
- This makes the output LOW because of power amplifier which behaves like inverter.
- A –ve going trigger pulse is applied to pin 2 and should have its DC level greater than the threshold level of the lower comparator (that is Vcc/3).

- At the –ve going edge of the trigger, as the trigger passes through Vcc/3, the output of the lower comparator goes HIGH and sets the FF.
- During the positive excursion, when the threshold voltage at pin 6 passes through 2/3 Vcc, the output of the upper comparator goes HIGH and resets the FF(Q=0, Q=1).
- The reset input (pin 4) provide a mechanism to reset the FF in a manner which over rides the effect of any instruction coming to FF from lower comparator.
- When this reset is not used, it is returned to Vcc

Monostable Operation

- Figure 8.3 shows a 555 timer connected for mono stable operation and its functional diagram is shown in Figure 8.4

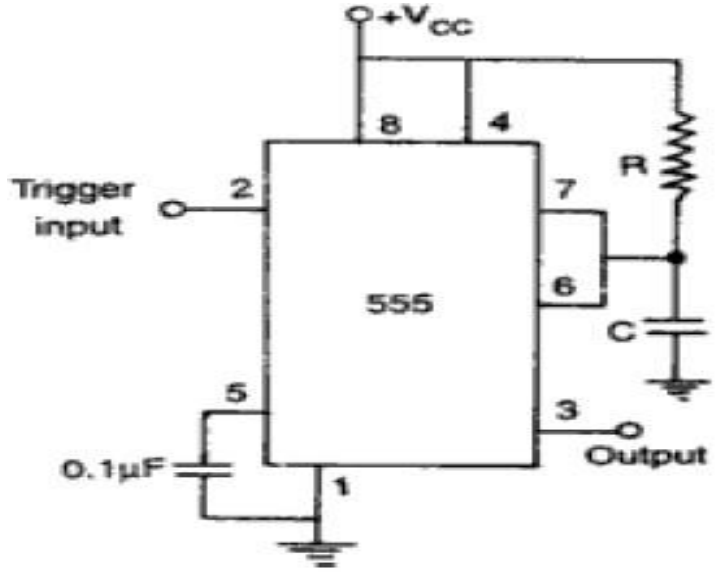


Fig. 8.3 Monostable multivibrator

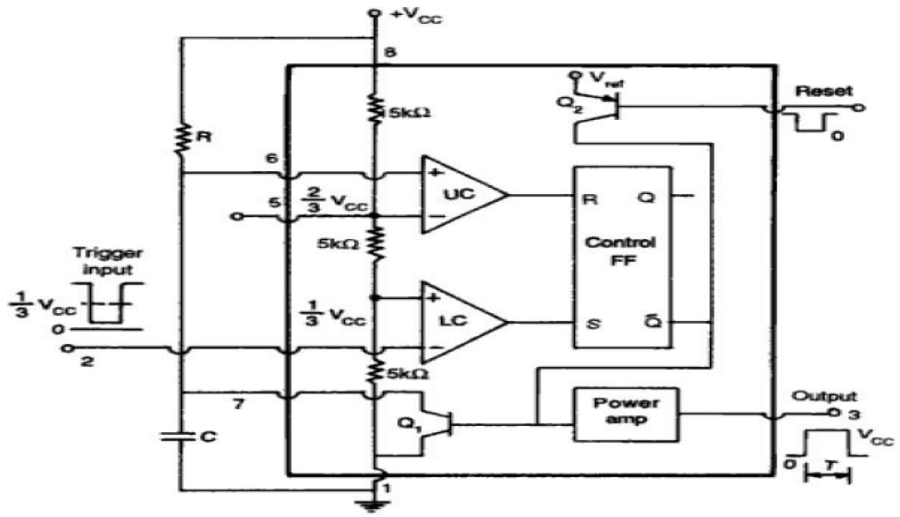


Fig. 8.4 Timer in monostable operation with functional diagram

- In the stand by state, FF holds transistor Q1 on, thus clamping the external timing capacitor C to ground. The output remains at ground potential ie low.
- As the trigger passes through Vcc/3, the FF is set ie Q = 0. This makes the transistor Q1 off and the short circuit across the timing capacitor C is released. As Q is low, output goes HIGH (= Vcc).
- Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC as in Figure 8.5 b.

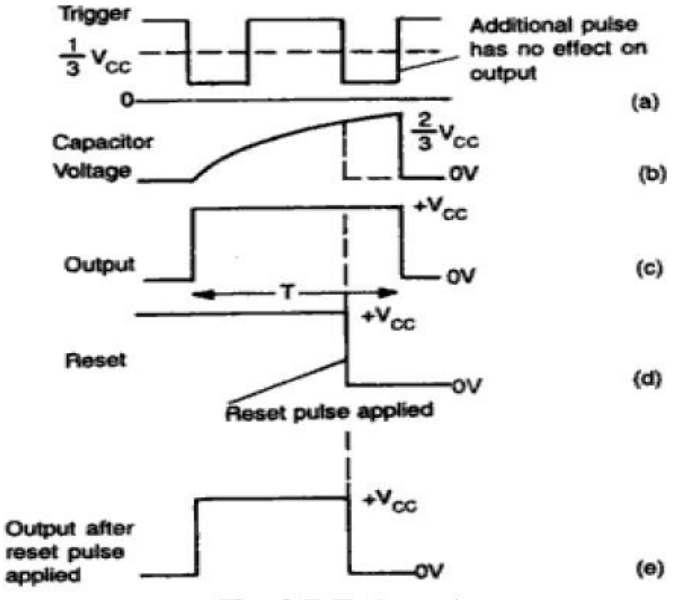


Fig. 8.5 Timing pulses

- After a time period T the capacitor voltage is just greater than 2/3 Vcc and the upper comparator resets the FF, that is, R =1, S=0. This makes Q = 1, transistor Q1 goes on (ie saturates), thereby discharging the capacitor C rapidly to ground potential. The output returns to the ground potential as shown in Figure 8.5c.
- The voltage across the capacitor as in Figure 8.5b is given by $V_c = V_{cc}(1- e^{-t/RC})$

  At t= T, Vc= 2/3 Vcc

  Therefore $2/3\ V_{cc} = V_{cc}(1- e^{-T/RC})$

  $e^{-T/RC} = 1 - 2/3 \Rightarrow e^{T/RC} = 3$

  $T/RC = \ln 3 \rightarrow T = 1.1\ RC$ ---------Eq(1)
- It is evident from Eq(1) that the timing interval is independent of the supply voltage. It may also be noted that once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state.

  However, if a negative going reset pulse as in Figure 8.5 d is applied to the reset terminal during the timing cycle, transistor Q2 goes off, Q1 becomes on and the external timing capacitor C is immediately discharged. The output now will be as in Figure 8.5 e.

Applications in Monostable Mode

- Some applications of monostable multivibrator are
  - Missing pulse detector
  - Linear ramp generator

Missing Pulse Detector:

- Missing pulse detector circuit using 555 timer is shown in Figure 8.8.

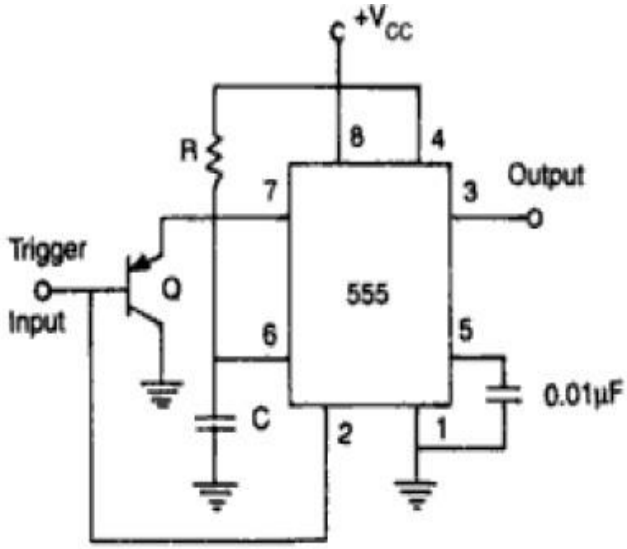


Fig. 8.8 A missing pulse detector monostable circuit

- Whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~0.7V). The output of the timer goes HIGH.
- So long the trigger pulse train keeps coming at pin 2, the output remains HIGH.
- However, if a pulse misses, the trigger input is high and transistor Q is cutoff. The 555 timer enters into normal state of monostable operation. The output goes LOW after time T of the mono-shot.
- Thus this type of circuit can be used to detect missing heart beat.

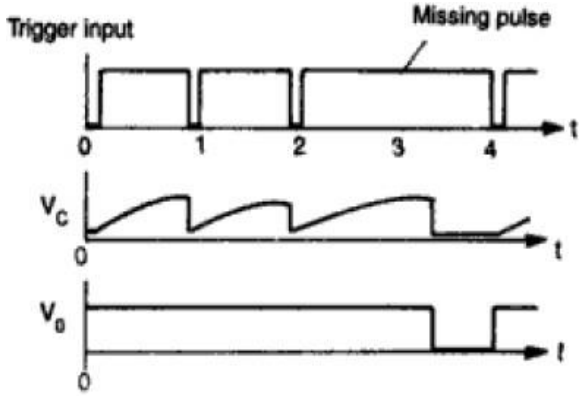


Fig. 8.9 Output of missing pulse detector

Astable Operation

- The device is connected for Astable operation as shown in Figure 8.15.

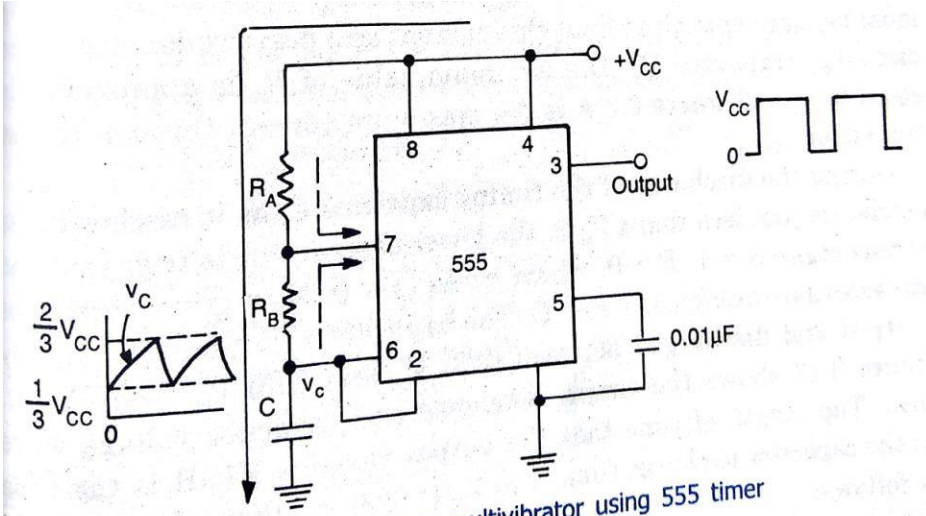


Fig. 8.15 Astable multivibrator using 555 timer

- For better understanding the complete diagram of Astable multivibrator with detailed internal diagram of 555 is shown in Figure 8.16.

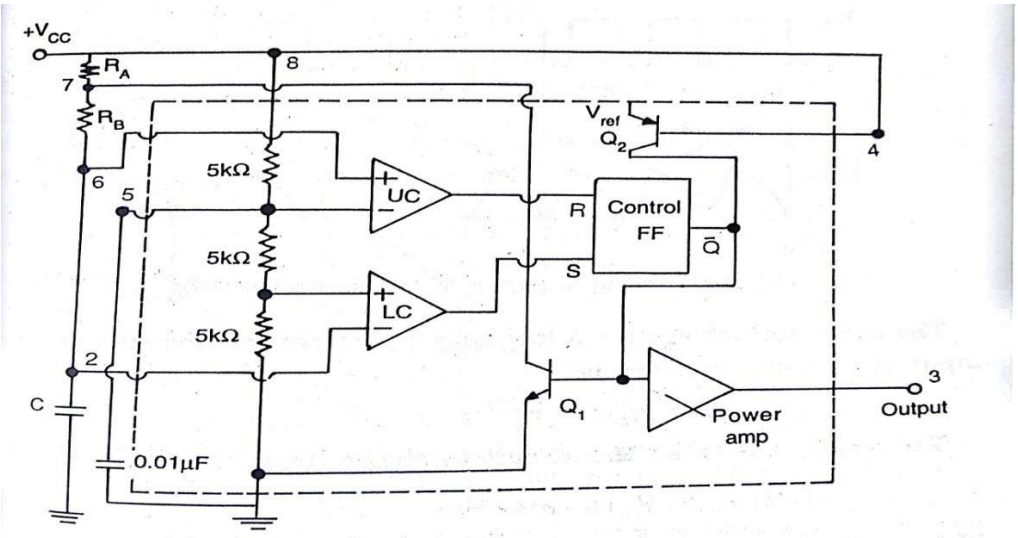


Fig. 8.16 Functional diagram of astable multivibrator using 555 timer

- Comparing with the monostable operation, the timing resistor is now split into two sections Ra and Rb. Pin 7 of discharging transistor Q1 is connected to the junction of Ra and Rb.

- When the power supply Vcc is connected, the external timing capacitor C charges towards Vcc with a time constant (Ra+Rb)C. During this time, output(pin 3) is HIGH (equals Vcc) as RESET R=0, SET S=1 and this combination makes Q=0 which has unclamped the timing capacitor C.

- When the capacitor voltage equals 2/3 Vcc the upper comparator triggers the control FF so that Q=1. This, in turn, makes the transistor Q1 on and capacitor C starts discharging towards ground through Rb and transistor Q1 with a time constant Rb C.

- Current also flows into transistor Q1 through Ra.

- Resistors Ra and Rb must be large enough to limit this current and prevent damage to the discharge transistor Q1.

- The minimum value of Ra is approximately equal to Vcc/0.2 where 0.2 A is the maximum current through the ON transistor Q1.

- During the discharge of the timing capacitor C, as it reaches Vcc/3, the lower comparator is triggered and at this stage S=1, R=0, which turns Q=0. Now Q=0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between 2/3 Vcc and 1/3 Vcc respectively.

- Figure 8.17 shows the timing sequence and capacitor voltage waveform.

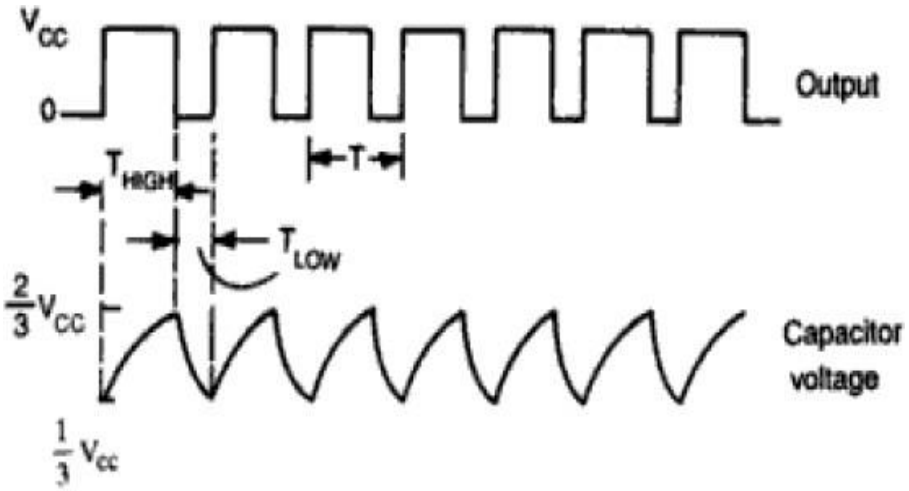


Fig. 8.17 Timing sequence of astable multivibrator

- The length of Time that the output remains HIGH is the time for the capacitor to charge from 1/3 Vcc to 2/3 Vcc. It may be calculated as follows.
- The capacitor voltage for a low pass RC circuit subjected to a step input of Vcc volts is given by Vc = Vcc (1- e^(-t/RC))
- The time t1 taken by the circuit to charge from 0 to 2/3 Vcc is

  2/3 Vcc = Vcc(1 – e^(-t1/RC)) ➔ t1= 1.09 RC

  And the time t2 to charge from 0 to 1/3 Vcc is

  1/3 Vcc = Vcc (1- e^(-t2/RC)) ➔ t2 = 0.405 RC

  So the time to charge from 1/3 Vcc to 2/3 Vcc

  tHIGH = t1 –t2 = 1.09 RC – 0.405 RC = 0.69 RC

  So, for the given circuit, tHIGH = 0.69 (Ra+Rb) C

  The output is low while the capacitor discharges from 2/3 Vcc to 1/3 Vcc and the voltage across the capacitor is given by

  1/3 Vcc =2/3 Vcc e^(-t/RC)

  Solving, we get t =0.69 RC

  So for the given circuit, tLOW = 0.69 Rb C

  Notice that both Ra & Rb are in the charge path, but only Rb is in the discharge path.

  Therefore, Total time T= tHIGH + tLOW

  ➔ T = 0.69(Ra + 2Rb) C

  So f =1/T = 1.45/((Ra + 2Rb) C)
- The Duty cycle D of a circuit is defined as the ratio of ON time to the total time period

  T = tON + tOFF.

  In this circuit, when the transistor Q1 is ON, the output goes LOW. Hence

  D % = (tLOW / T) * 100

  = Rb/(Ra + 2Rb) *100

With the circuit configuration of Fig 8.15 it is not possible to have a duty cycle more than 50% since tHIGH = 0.69 (Ra+Rb) C will always be greater than tLOW = 0.69 Rb C

- In order to obtain a symmetrical square wave ie D =50%, the resistance Ra must be reduced to zero.
- However, now Pin 7 is connected directly to Vcc and extra current will flow through Q1 when it is ON. This may damage Q1 and hence the timer
- An alternate circuit which will allow duty cycle to be set at practically any level is shown in Figure 8.19.

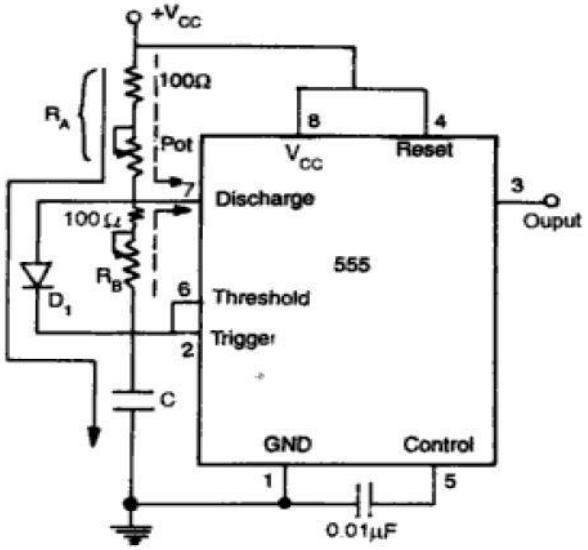


Fig. 8.19 Adjustable duty cycle rectangular wave generator

- During the charging portion of the cycle, diode D1 is forward biased effectively short circuiting Rb so that tHIGH = 0.69 Ra C
- However, during the discharging portion of the cycle, transistor Q1 becomes ON, thereby grounding pin 7 and hence the diode D1 is reverse biased. So tLOW = 0.69 Rb C

Therefore T= tHIGH + tLOW = 0.69(Ra+Rb)C

➔ f = 1/T = 1.45 /(Ra+Rb)C

And Duty cycle, D = Rb /(Ra+Rb)

- Resistors Ra and Rb could be made variable to allow adjustment of frequency.

- However, a series resistor of at least 100Ω should be added to each Ra and Rb. This will limit peak current to the discharge transistor Q1 when the variable resistors are at minimum value.
- And, if Ra is made equal to Rb, then 50% duty cycle is achieved.

Example: Refer Figure 8.15. For Ra = 6.8 KΩ, Rb = 3.3 KΩ and C=0.1 µF, calculate (a) tHIGH (b) tLOW (c) free running frequency (d) duty cycle D.

Solution:

a) tHIGH = 0.69(Ra+Rb) C

= 0.69 (6.8 KΩ + 3.3 KΩ) 0.1 µF

= 0.7 ms

b) tLOW = 0.69 Rb C

= 0.69 (3.3KΩ) 0.1 µF

= 0.23 ms

c) f = 1.45/((Ra +2Rb) C)

= 1.45/((6.8 KΩ + 2(3.3 KΩ)) (0.1 µF))

= 1.07 KHz

d) Duty Cycle D = tLOW / T = Rb/(Ra + 2Rb)

= 3.3 KΩ /(6.8 KΩ + 2 (3.3 KΩ))

= 0.25 = 25%

Applications in Astable Mode

- A couple of applications in Astable mode are
  - Pulse position modulator
  - FSK Generator

Pulse Position Modulator:

- The Pulse Position Modulator can be constructed by applying a modulating signal to pin5 of a 555 timer connected for Astable operation as shown in Figure 8.22.

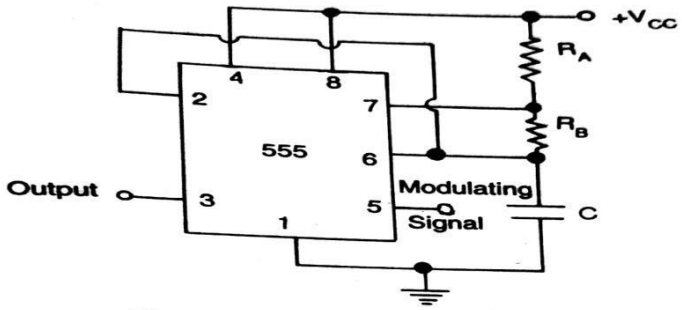


Fig. 8.22 Pulse position modulator

Fig. 8.23 Pulse position modulator output

- The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.
- Figure 8.23 shows the output waveform generated for a triangle wave modulation signal. It may be noted from the output waveform that the frequency is varying leading to pulse position modulation.

Phase Locked Loops: Introduction

- Although the evolution of the phase-locked loop began in the early 1930's, its cost outweighed it's advantages at first.
- With the rapid development of integrated circuit technology, however, the phase locked loop has emerged as one of the fundamental building blocks in electronics technology.
- The phase-locked loop principle has been used in applications such as FM stereo decoders, motor speed controls, tracking filters, frequency synthesized transmitters and

receivers, FM demodulators, FSK decoders, and a generation of local oscillator frequencies and in TV and FM tuners.

Block Schematic and Operation Principle

- Figure 10.25 shows the phase-Locked loop (PLL) in its basic form.

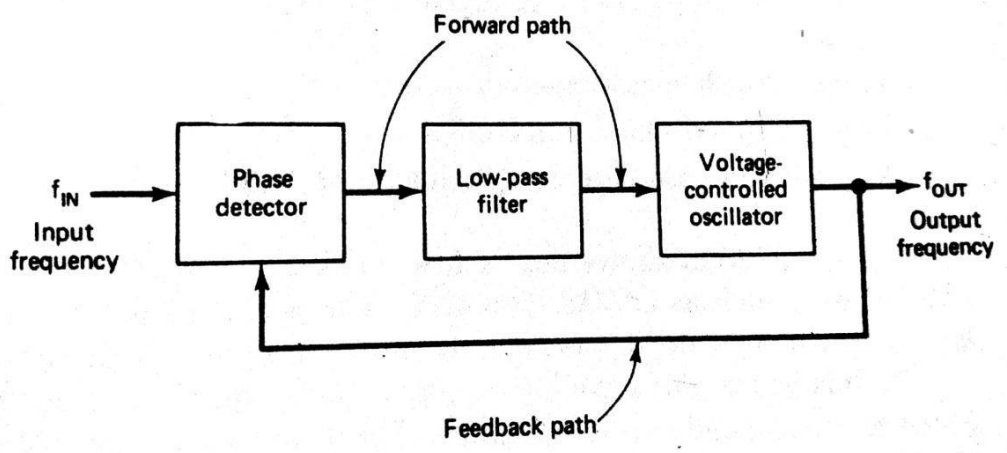


Figure 10–25 Block diagram of a phase-locked loop.

- As illustrated in this figure, the phase-locked loop consists of (1) a phase detector (2) a low-pass filter (3) a voltage controlled oscillator.
- The phase detector or comparator compares the input frequency fIN with the feed-back frequency fOUT. The output of the phase detector is proportional to the phase difference between fIN and fOUT. The output voltage of a phase detector is a DCvoltage and therefore is often referred to as the error voltage.
- The output of the phase detector is then applied to the low pass filter, which removes the high frequency noise and produces a DC level. This DC level, in turn, is the input to the voltage controlled oscillator(VCO).
- The output frequency of the VCO is directly proportional to the input DC level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies.
- In short, the phase locked loop goes through three states: free-running, capture and phase lock.

- Before the input is applied, the phase locked loop is in the free-running state.
- Once the input frequency is applied, the VCO frequency starts to change and the phase locked loop is said to be in the capture mode.
- The VCO frequency continues to change until it equals the input frequency, and the phase-locked loop is then in the phase locked state. When phase locked, the loop tracks any change in the input frequency through its repetitive action.

Phase Detector

- The phase detector compares the input frequency and the VCO frequency and generates a DC voltage that is proportional to the phase difference between the two frequencies.
- Depending on the analog or digital phase detector used, the PLL is either called an analog or digital type respectively.
- A double balanced mixer is a classic example of an analog phase detector. On the other hand examples of digital phase detectors are these:

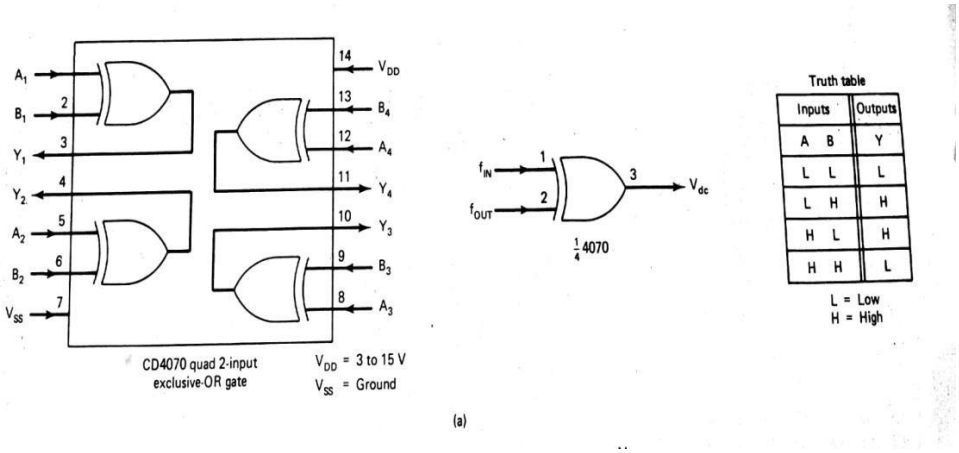
1 Exclusive OR phase detector

2 Edge triggered phase detector

3 Monolithic phase detector

Exclusive OR Phase Detector:

- Figure 10.26a shows the exclusive OR phase detector that uses an exclusive OR gate such as CMOS type 4070.



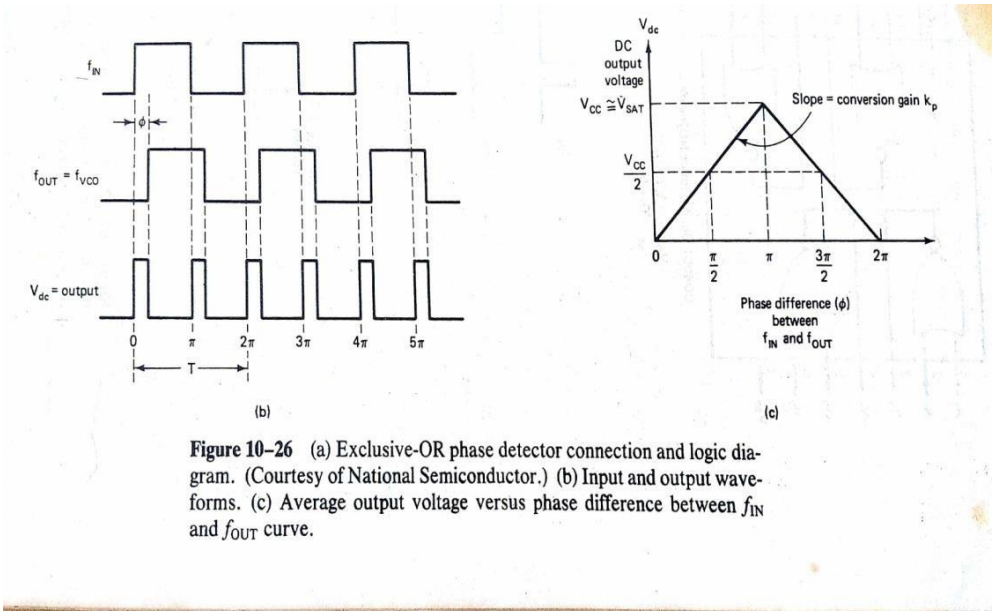


Figure 10–26 (a) Exclusive-OR phase detector connection and logic diagram. (Courtesy of National Semiconductor.) (b) Input and output waveforms. (c) Average output voltage versus phase difference between f_{IN} and f_{OUT} curve.

- The output of the exclusive OR gate is high only when fIN or fOUT is high, as shown in figure 10.26b.
- In this figure, fIN is leading fOUT by ϕ degrees

ie the phase difference between fIN and fOUT is ϕ degrees.

- The DC output voltage of the exclusive OR phase detector is a function of the phase difference between its two inputs.
- Figure 10.26 c shows DC output voltage as a function of the phase difference between fIN and fOUT. This graph indicates that the maximum DC output voltage occurs when the phase difference is Π radians or 180 degrees.
- The slope of the curve between 0 and Π radians is the conversion gain Kp of the phase detector.

For example, if the exclusive OR gate uses a supply voltage Vcc = 5 V, the conversion gain Kp is

$$K_p = 5V/\Pi = 1.59 \text{ V/Radians}$$

- The exclusive OR type of phase detector is generally used if fIN and fOUT are square waves.
- The edge triggered phase detector, on the other hand, is preferred if the fIN and fOUT are pulse waveforms with less than 50% duty cycles.

- These both types of phase detectors are sensitive to harmonics of the input signal and changes in duty cycles of fIN and fOUT. In such cases Monolithic phase detector is used

Low Pass Filter

- The second block shown in the PLL block diagram of figure 10.25 is a low-pass filter.
- The function of the low-pass filter is to remove the high frequency components in the output of the phase detector and to remove high frequency noise.
- More important, the low-pass filter controls the dynamic characteristics of the phase-locked loop. These characteristics include capture and lock ranges, band width, and transient response.
- The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency fIN. An equivalent term for lock range is the tracking range.
- On the other hand, the capture range is the frequency range in which the PLL acquires phase lock. Obviously the capture range is always smaller than the lock range.
- As the filter bandwidth is reduced, it's response time increases. However, reduced band width reduces the capture range of PLL.
- Nevertheless, reduced bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes the noise
- The loop filter used in the PLL may be one of the three types shown in figure 10.29.

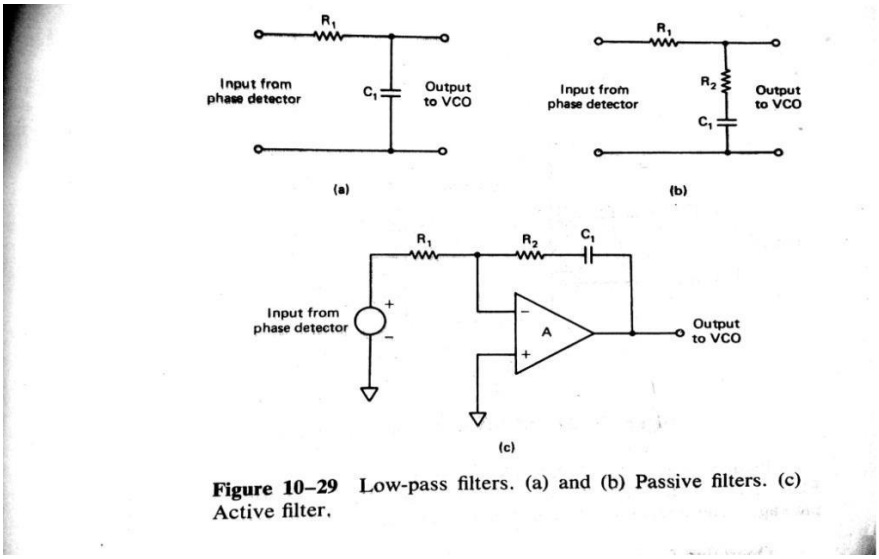


Figure 10–29 Low-pass filters. (a) and (b) Passive filters. (c) Active filter.

- With the passive filters of Figure 10.29a and b, an amplifier is generally used for gain. On the other hand, the active filter of Figure 10.29c includes the gain.

Voltage Controlled Oscillator

- A third section of the PLL is the voltage controlled oscillator.
- The VCO generates an output frequency that is directly proportional to it's input voltage. The block diagram of the VCO is shown in Figure 10.30.

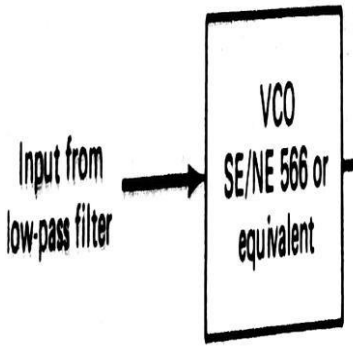


Figure 10-30 VCO block diagram.

565 PLL

- Figure 10.32 shows the block diagram and connection diagram of the 565 PLL. The device is available as a 14 pin DIP package and as 10 pin metal can package.

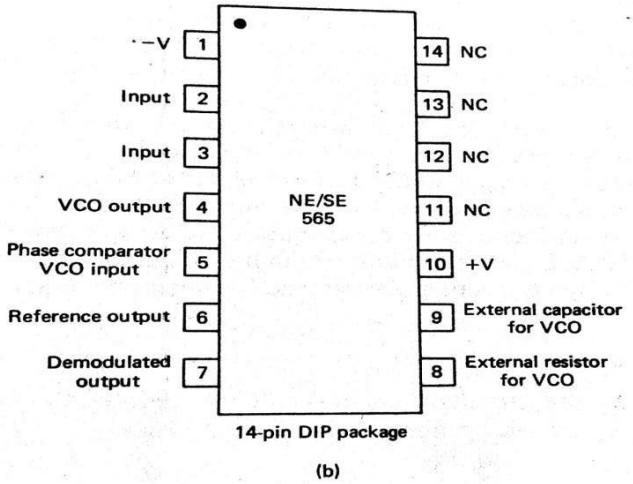
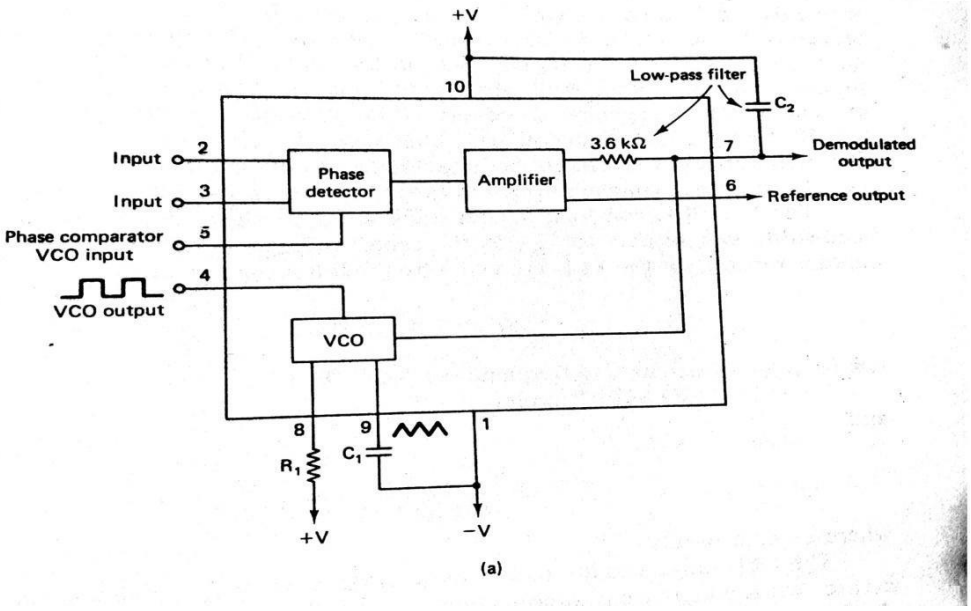


Figure 10–32 (a) NE/SE565 PLL block diagram. (b) Connection diagram. (Courtesy of Signetics Corporation.)



- The central frequency of the PLL is determined by the free running frequency of the VCO, which is given by the equation

  fOUT = 1.2/(4 R1 C1) Hz

  where R1 and C1 are external resistor and capacitor connected to pins 8 & 9 respectively.

- The VCO free running frequency fOUT is adjusted externally with R1 and C1 to be at the center of the input frequency range.
- Although C1 can be any value, R1 must have a value between 2 KΩ and 20 KΩ
- A capacitor C2 connected between pin 7 and positive supply (pin 10) forms a first order low-pass filter with an internal resistance of 3.6 KΩ.
- The filter capacitor C2 should be large enough to eliminate variations in the demodulated output voltage at Pin 7 in order to stabilize the VCO frequency.
- The 565 PLL can lock to and track an input signal over typically + or – 60% bandwidth with respect to fOUT as the center frequency.
- The lock range fL and capture range fC of the PLL are given by the following equations:

  fL = + or – 8 fOUT/ V Hz

  Where fOUT=free running frequency of VCO (Hz)

  V = v – (-v) volts

  and fC = + or – [fL/((2π) (3.6 * 10^3) C2)]^(1/2)

  Where C2 is in Farads.
- The lock range usually increases with an increase in input voltage but decreases with an increase in supply voltages.
- Pins 2 & 3 are the input terminals and an input signal can be direct-coupled, provided that there is no DC voltage difference between the pins and DC resistances seen from pins 2 & 3 are equal.
- A short between pins 4 & 5 connects the VCO output (fOUT) to the phase comparator and enables the comparator to compare fOUT with the input signal fIN.

Applications of PLL

Frequency Multiplication:

- Figure 9.12 gives the block diagram of a frequency multiplier using PLL.

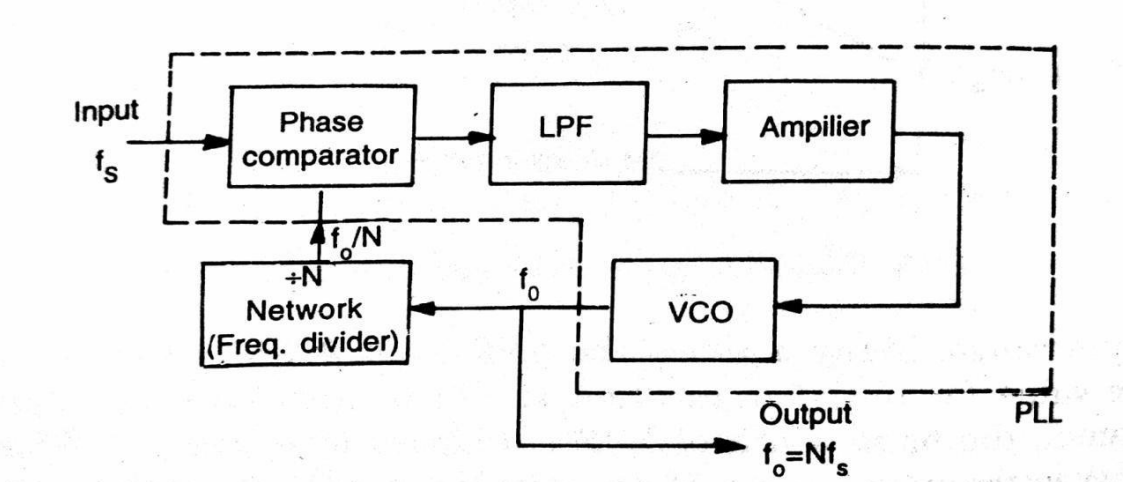


Fig. 9.12 Frequency multiplier using IC PLL

- A divide by N network is inserted between the VCO output and the phase comparator input.
- In the locked state, the VCO output frequency fo is given by

  fo = Nfs

- The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

End of Unit II

Unit III

Data Converters

Introduction

- Most of the real world physical quantities such as voltage, current, temperature, pressure and time etc are available in analog form.
- Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store, or transmit the analog signal with out introducing considerable error because of superimposition of noise as in the case of amplitude modulation.
- Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise.
- The operation of any digital communication system is based upon Analog to Digital (A/D) and Digital to Analog (D/A) conversion.
- Figure 10.1, highlights a typical application with in which A/D and D/A conversion is used.

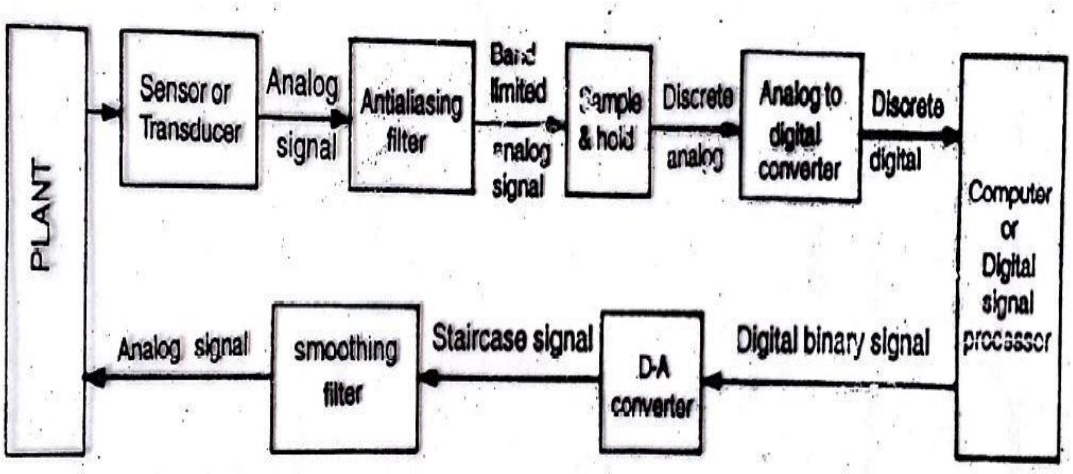


Fig. 10.1 Circuit showing application of A/D and D/A converter

- The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal.
- The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit.
- The ADC output is a sequence in binary digit. The micro-computer or Digital signal processor performs the numerical calculations of the desired control algorithm.
- The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal.
- The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit.
- The ADC output is a sequence in binary digit. The micro-computer or Digital signal processor performs the numerical calculations of the desired control algorithm.
- The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC.
- The output of a D/A converter is commonly a staircase. This staircase like output is passed through a smoothing filter to reduce the effect of quantization noise.

Applications of A/D and D/A conversion

- The scheme given in Figure 10.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multi meter, direct digital control, digital signal processing, microprocessor based instrumentation.

Basic DAC techniques

- The schematic of a DAC is shown in Figure 10.2.

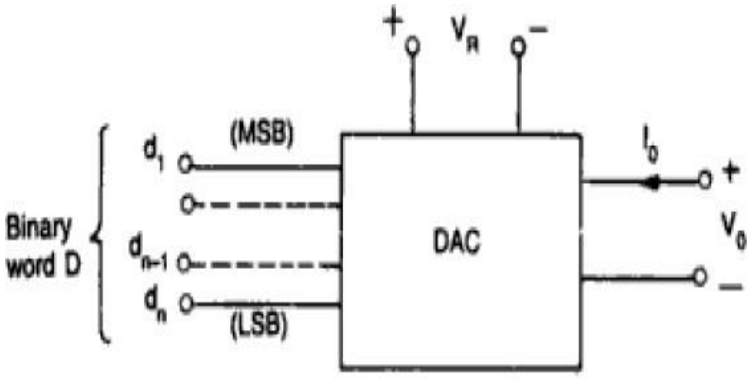


Fig. 10.2 Schematic of a DAC

- The input is an n-bit binary word D and is combined with a reference voltage vR to give an analog output signal.
- The output of a DAC can be either a voltage or current.
- For a voltage output DAC, the D/A converter is mathematically described as

Vo=K Vfs(d1 2^-1 + d2 2^-2 + d3 2^-3+ ----- +dn 2^-n) --- (1)

Where Vo = output voltage, Vfs=full scale output voltage

K = scaling factor usually adjusted to unity

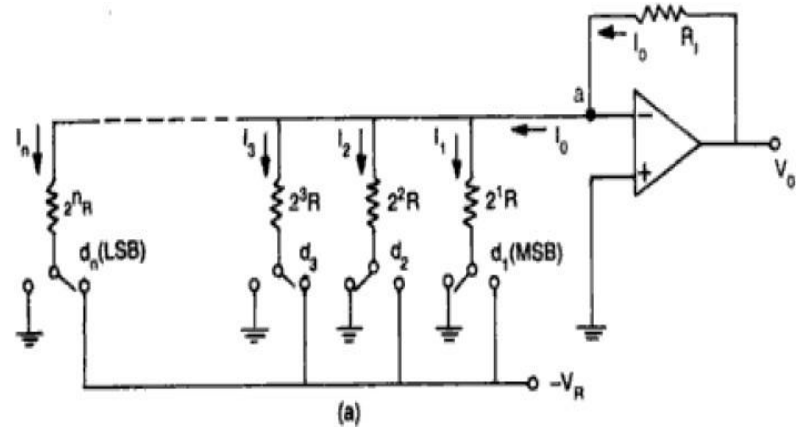
d1 d2 d3-------- dn = n-bit binary fractional word

d1 = MSB with weight of Vfs/2, dn =LSB with a weight of Vfs/2^n

- There are various ways to implement eq(1). Here we shall discuss the following resistive techniques only
    - Weighted resistor DAC
    - R-2R Ladder DAC
    - Inverted R-2R Ladder DAC

Weighted Resistor DAC:

- One of the simplest circuits shown in Figure 10.3a uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches d1, d2, d3, -----dn, controlled by Binary input word.



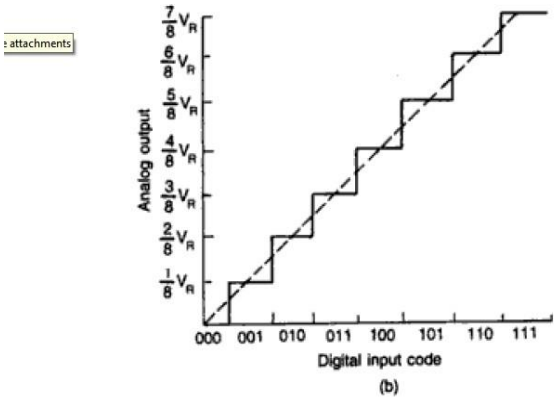


Fig. 10.3 (a) A simple weighted resistor DAC (b) Transfer characteristics of a 3-bit DAC

- These switches are single pole double throw (SPDT) type.
- If the Binary input to a particular switch is 1, it connects the resistance to the reference voltage (-Vr). And if the input bit is zero, the switch connects the resistor to ground.
- From Figure 10.3a, the output current Io for an ideal op-amp can be written as

Io = I1 +I2 + ---------- + In

= (Vr/(2R)) d1 + (Vr/(2^2 R)) d2 + -----+(Vr/(2^n R)) dn

= Vr/R (d1 2^-1 + d2 2^-2 + --------- + dn 2^-n)

The output voltage

Vo=Io Rf=Vr Rf/R (d1 2^-1 + d2 2^-2 + ---- + dn 2^-n) – (2)

- Comparing eq(1) with eq(2), we get

if Rf = R, then K=1, and Vfs = Vr

- The circuit shown in Figure 10.3a uses a –ve reference voltage. The analog output voltage is therefore +ve staircase as shown in Figure 10.3b for a 3-bit weighted resistor DAC.
- It may be noted that
    - Although the op-amp in Figure 10.3a is connected in inverting mode, it can also be connected in non-inverting mode.
    - The op-amp is simply working as a current-to-voltage converter.
    - The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches , the reference voltage should be +5V and the output will be –ve.

Problems with Weighted Resistor DAC

- The accuracy and stability of a DAC depends up on the accuracy of the resistors and tracking of each other with temperature.
- There are, however, a number of problems associated with this type of DAC.
- One of the disadvantages of Binary weighted resistor type DAC is the wide range of resistor values required.
- It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bits increases, the range of resistance value increases.
- For 8-bit DAC, the resistors required are 2^1 R, 2^2 R, ------ , 2^8 R. The largest resistor is 128 times the smallest one for only 8-bit DAC.
- For a 12-bit DAC, the largest resistance required is 5.12 MΩ if the smallest is 2.5KΩ.
- The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy.
- The choice of smallest resistor value as 2.5 KΩ is reasonable, otherwise loading effect will be there.
- The difficult of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8 bits.

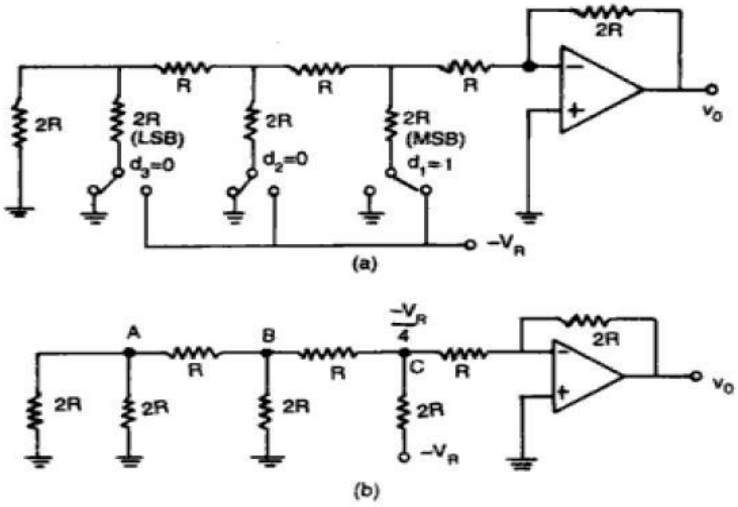
R-2R Ladder DAC:

- Wide range of resistors are required in Binary Weighted Resistor type DAC. This can be avoided by using R-2R Ladder type DAC where only two values of resistors are required.
- It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 KΩ to 10KΩ.
- For simplicity, consider a 3-bit DAC as shown in Figure 10.5a, where the switch position d1 d2 d3 corresponds to the Binary word 100.
- The circuit can be simplified to the equation form of Figure 10.5b and finally to Figure 10.5c.
- Then, voltage at node C can be easily calculated by the set procedure of network analysis as

  -Vr ((2/3) R) / (2R + (2/3)R) = -Vr/4

- The output voltage

Vo= -2R/R(-Vr/4) = Vr/2 = Vfs/2



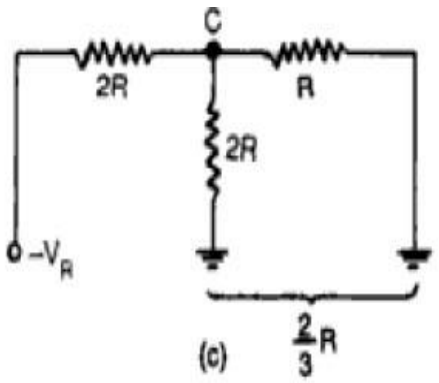


Fig. 10.5 (a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

A/D Converters

- The block schematic of ADC shown in Figure 10.9 provides the function just opposite to that of a DAC.

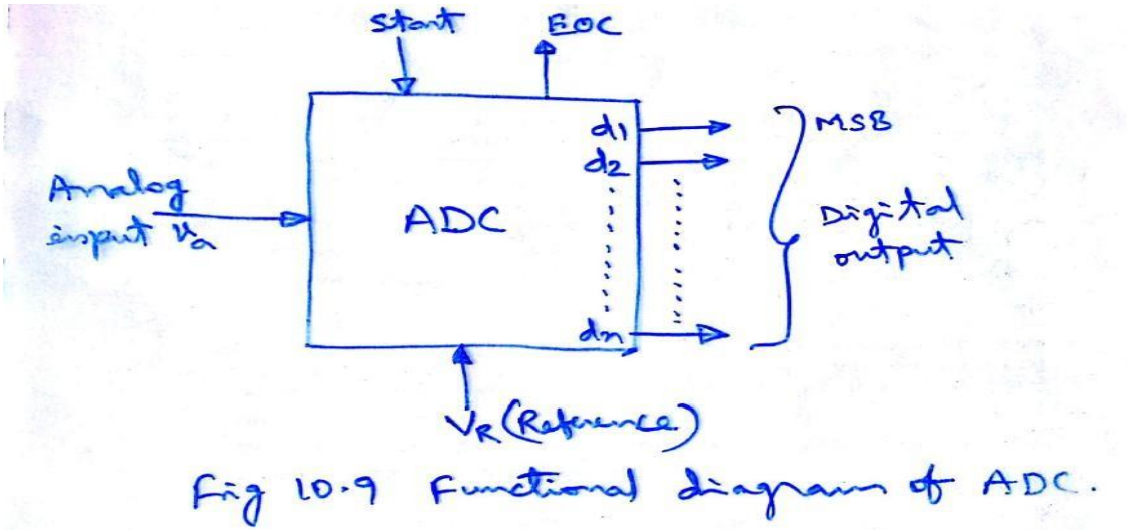


Fig 10.9 Functional diagram of ADC.

- It accepts an analog input voltage Va and produces an output binary word d1d2 ------- dn of functional value D, so that

D = d1 2^-1 + d2 2^-2 +----------+ dn 2^-n

where d1 is the MSB and dn is the LSB.

- An ADC usually has two additional control lines: the START input to tell the ADC when to start the conversion and EOC (end of conversion) output to announce when the conversion is complete.
- Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.
- ADCs are classified broadly into two groups according to their conversion technique
    - Direct type ADCs
    - Integrating type ADCs
- Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes
    - Flash (comparator) type converter
    - Counter type converter
    - Tracking or servo conveter
    - Successive approximation type converter
- Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:
    - Charge balancing ADC
    - Dual slope ADC

Successive Approximation Converter

- The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods.
- For example, an 8-bit converter would require eight clock pulses to obtain a digital output. Figure 10.13 shows an 8-bit converter.

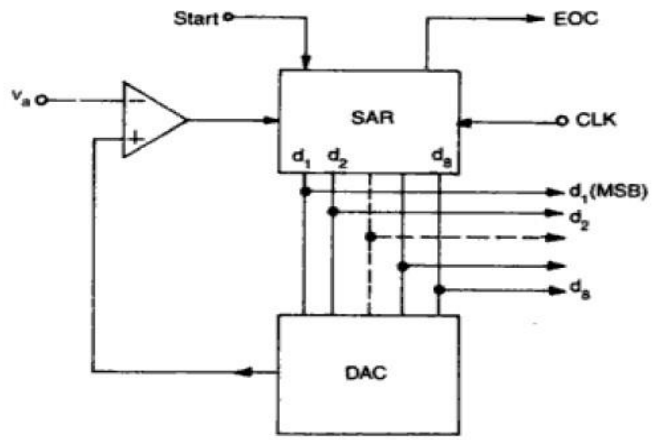


Fig. 10.13 Functional diagram of the successive approximation ADC

- The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error.

Circuit Operation:

- With the arrival of the START command the SAR sets the MSB d1=1, with all other bits to zero so that the trial code is 10000000.
- The output Vd of the DAC is now compared with analog input Va.
- If Va is greater than the DAC output Vd, then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.
- However, if Va is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to zero and go on to the next lower significant bit.
- This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested.
- Whenever the DAC output crosses Va, the comparator changes state and this can be taken as the end of conversion (EOC) command.
- Figure 10.14a shows a typical conversion sequence and Figure 10.14b shows the associated waveforms.

Correct digital representation	*Successive approximation register output V_d at different stages in the conversion*	*Comparator output*
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 10.14 (a) Successive approximation conversion sequence for a typical analog input

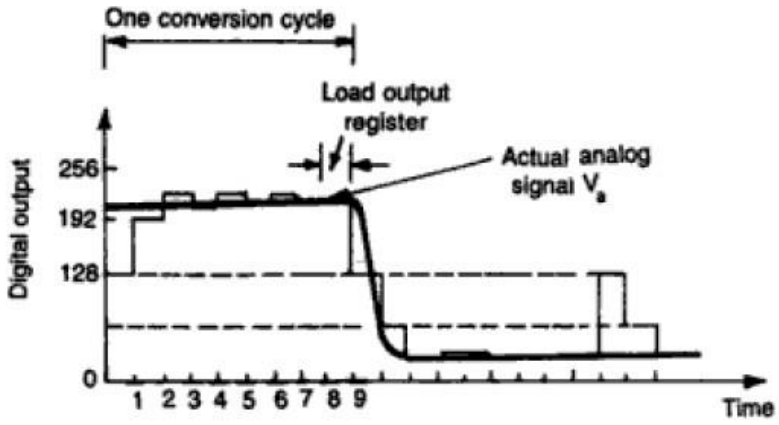
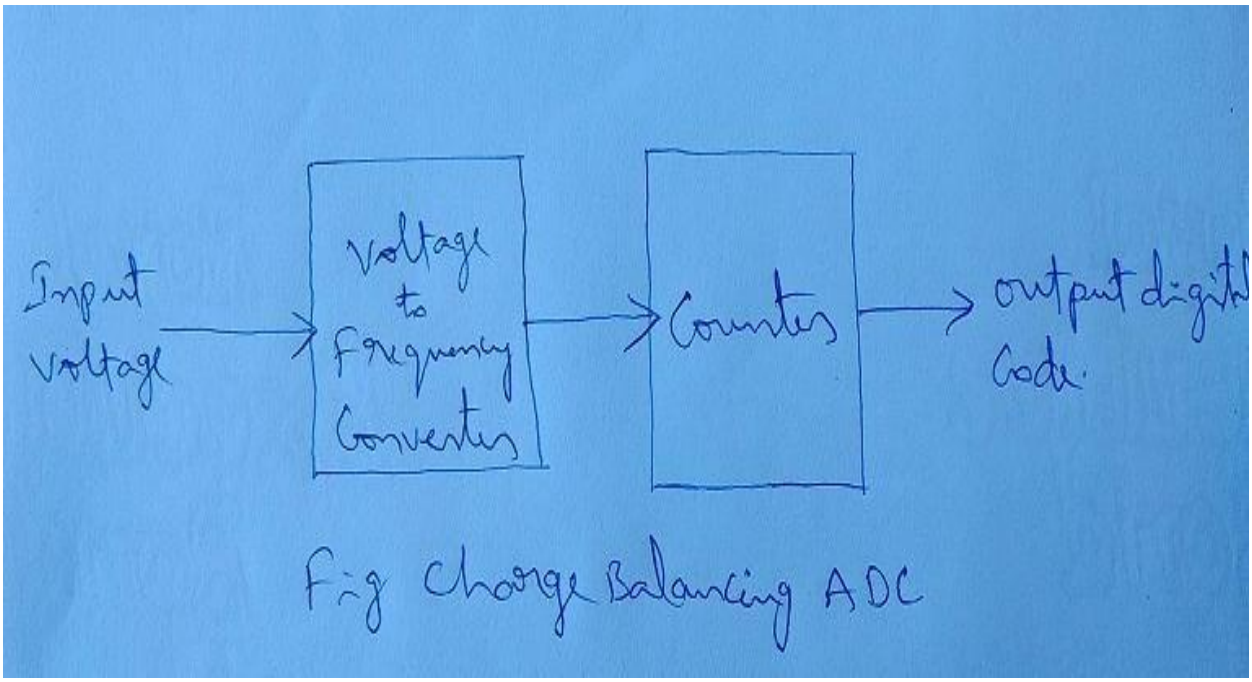


Fig. 10.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

- It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage.
- It requires 8 pulses to establish the accurate output regardless of the value of the analog input.
- However, one additional clock pulse is used to load the output register and reinitialize the circuit.
- The AD7592 (Analog Devices Co.), a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.

Charge Balancing ADC

- The figure showing this type of conversion is shown below.



- The principle of charge balancing ADC is to first convert the input signal to a frequency using a voltage to frequency converter.
- This frequency is then measured by a counter and converted to an output code proportional to the analog input.
- The main advantage of these converters is that it is possible to transmit frequency even in noisy environment or in isolated form.
- However the limitation of the circuit is that the output of V/F converter depends upon an RC product whose value cannot be easily maintained with temperature and time.
- The drawback of the charge balancing ADC is eliminated by the Dual slope conversion.

DAC/ADC Specifications

- Both D/A and A/D converters are available with wide range of specifications.

- The various important specifications of converters generally specified by the manufacturers are analyzed
- The specifications are Resolution, Linearity, Accuracy, Monotonicity, settling time and stability.

Resolution:

- The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter.
- For example, an 8-bit D/A converter has 2^8 -1 =255 equal intervals. Hence the smallest change in output voltage is 1/255 of the full scale output range. In short, the resolution is the value of the LSB.

  Resolution (in volts) = Vfs/((2^n) – 1)

Linearity:

- The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics.
- In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear.

Accuracy:

- Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.
- Relative accuracy is the maximum deviation after gain and offset errors have been removed.

Monotonicity:

- A monotonic DAC is the one whose analog output increases for an increase in digital input.
- A monotonic characteristic is essential in control applications, otherwise oscillations can result.

Settling time:

- The most important dynamic parameter is the settling time.
- It represents the time it takes for the output to settle with in a specified band + or – ½ LSB of its final value following a code change at the input (usually a full scale change).
- Settling time ranges from 100 ns to 10 μs depending on word length and type of circuit used.

Stability:

- The performance of converter changes with temperature, age and power supply variations.
- So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

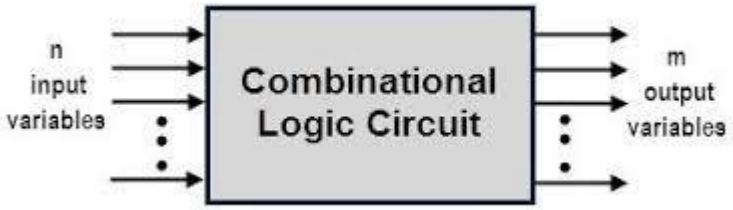
End of Unit III

Unit 4

COMBINATIONAL INTEGRATED CIRCUITS

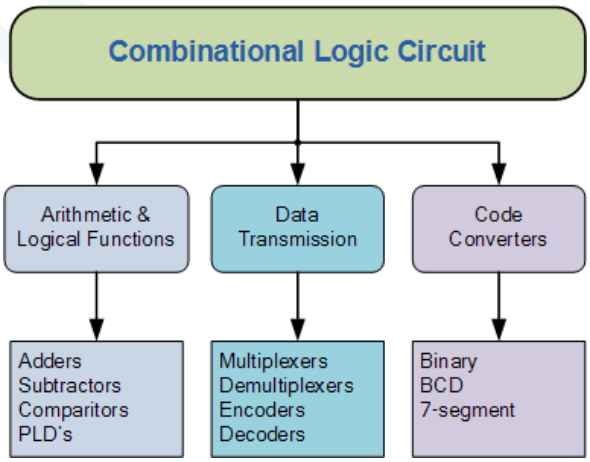
Combinational Logic Circuits:

- The logic level at the output depends on the combination of logic levels present at the inputs.
- A combinational circuit has no memory, so its output depends only on the current value of its inputs.
- For *n* input variables, there are 2^n possible binary input combinations.
- For each binary combination of the input variables, there is one possible output



- Combinational Logic Circuits are made up from basic logic NAND, NOR or NOT gates that are "combined" or connected together to produce more complicated switching circuits. These logic gates are the building blocks of combinational logic circuits.
- Combinational logic circuits can be very simple or very complicated and any combinational circuit can be implemented with only NAND and NOR gates as these are classed as "universal" gates

Classification of Combinational Logic:

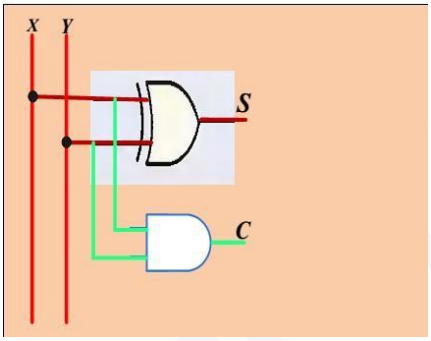


The combinational logic circuits can be classified into various types based on the purpose of usage, such as arithmetic & logical functions, data transmission, and code converters. To solve the arithmetic and logical functions we generally use adders, subtractors, and comparators which are generally realized by combining various logic gates called as combinational logic circuits. Similarly, for data transmission, we use multiplexers, demultiplexers, encoders, and decoders which are also realized using combinational logic. The code converters such as binary, BCD, and 7-segment are designed using various logic circuits.

Half Adder: It is a combinational circuit that performs the addition of two bits, this circuit needs two binary inputs and two binary outputs.

Inputs		Outputs	
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Truth table



Where S is the sum and C is the carry.

$$\begin{cases} S = X \oplus Y \\ C = XY \end{cases}$$ 2 (Using XOR and AND Gates)

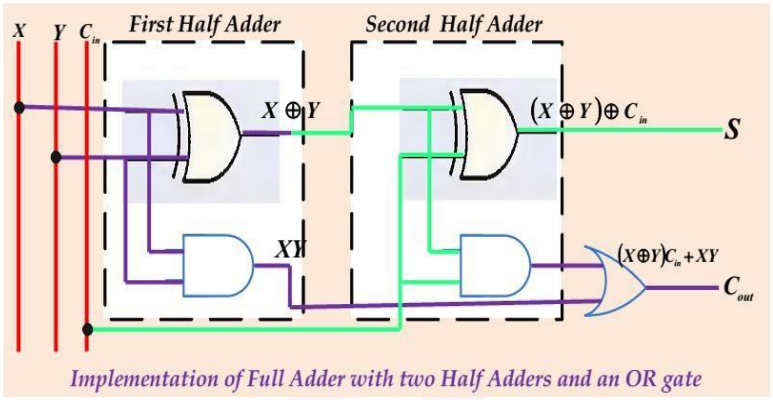
- The implementation of half adder using exclusive–OR and an AND gates is used to show that two half adders can be used to construct a full adder.
- The inputs to the XOR gate are also the inputs to the AND gate.

Full Adder: Full Adder is a combinational circuit that performs the addition of three bits (two significant bits and previous carry).

- It consists of three inputs and two outputs, two inputs are the bits to be added, the third input represents the carry form the previous position.
- The full adder is usually a component in a cascade of adders, which add 8, 16, etc, binary numbers.
- The output is equal to1 when only one input = 1 or when all three inputs are equal to 1
- The output has a carry 1 if two or three inputs are equal to 1.

Inputs			Outputs	
X	Y	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table for the full adder



Implementation of Full Adder with two Half Adders and an OR gate

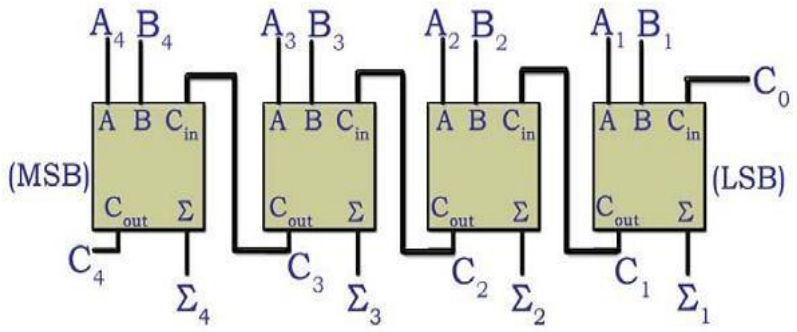
$$\begin{cases} S = C_{in} \oplus (X \oplus Y) \\ C_{out} = C_{in} \cdot (X \oplus Y) + XY \end{cases}$$

Parallel binary adder:

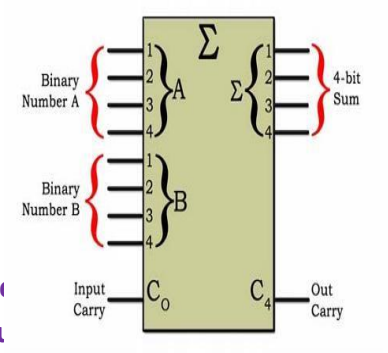
- Parallel Adder is a digital circuit that produces the arithmetic sum of 2 binary numbers.
- The Parallel binary adder is a combinational circuit consists of various full adders in parallel structure so that when more than 1-bit numbers are to be added, then there can be full adder for every column for the addition.
- The number of full adders in a parallel binary adder depends on the number of bits present in the number for the addition.
- If 4-bits numbers are to be added, then there will be 4-full adder in the parallel binary adder.

4-Bit parallel Binary adder:

- A group of four bits is called a nibble. A basic 4-bit parallel adder is implemented with four full-adder stages as shown in Figure.
- The LSBs (A1and B1) in each number being added go into the right-most full-adder: the higher-order bits are applied as shown to the successively higher-order adders, with the MSBs (A4and B4) in each number being applied to the left-most full-adder. The carry output of each adder is connected to the carry input of the next higher-order adder as indicated. These are called internal carries.



4-bit parallel binary adder logic symbol & Truth Table:



C_{n-1}	A_n	B_n	$\sum_n$	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

For exampl **m and output ca**
two 4-bit nu **B4B3B2Bl= 1100**

n = 1: $A_1 = 0$, $B_1 = 0$, and $C_{n-1} = 0$. From the first row of the table,

$\sum_1 = \mathbf{0}$ and $C_1 = 0$

For n = 2: $A_2 = 0$, $B_2 = 0$, and $C_{n-1} = 0$. From the 1st row of the table,

$\sum_1 = \mathbf{0}$ and $C_2 = 0$

For n = 3: $A_3 = 1$, $B_3 = 1$, and $C_{n-1} = 0$. From the 4th row of the table,

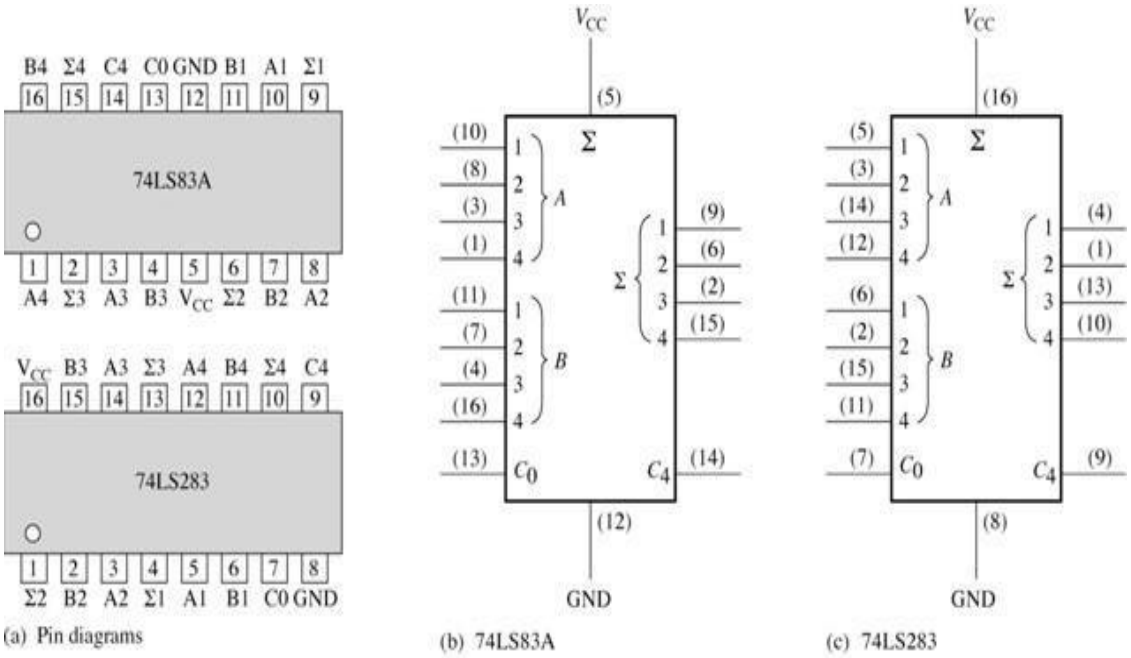
$\sum_1 = \mathbf{0}$ and $C_3 = 1$

For n = 4: $A_4 = 1$, $B_4 = 1$, and $C_{n-1} = 1$. From the last row of the table,

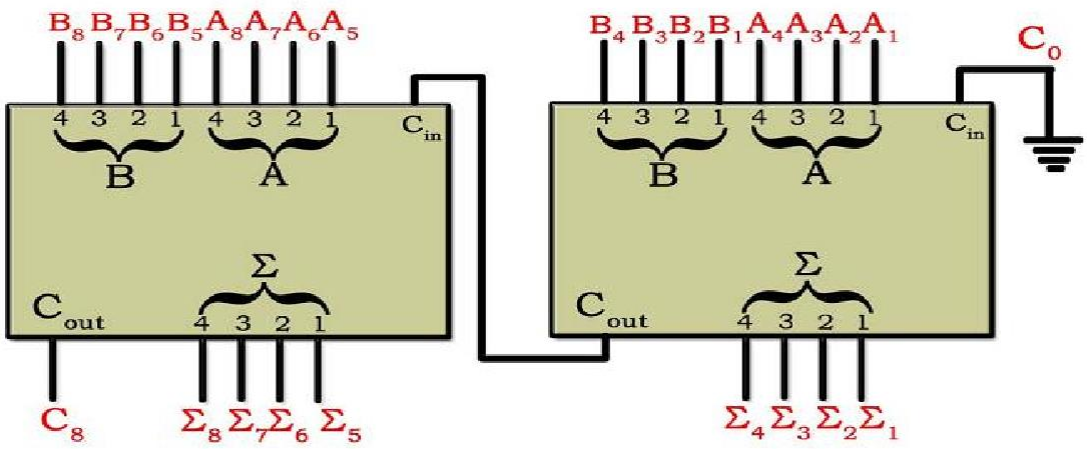
$\sum_1 = \mathbf{1}$ and $C_4 = \mathbf{1}$

So C_4 becomes the output carry and the sum of two numbers 1100 and 1100 is **11000**.

4- bit parallel adders: The most common is a 4-bit parallel adder IC (74LS83/74283) that contains four inter connected full-adders and the look-ahead carry circuitry needed for high-speed operation. The 7483 and 74283 are a TTL medium scale integrated (MSI) circuit with same pin configuration



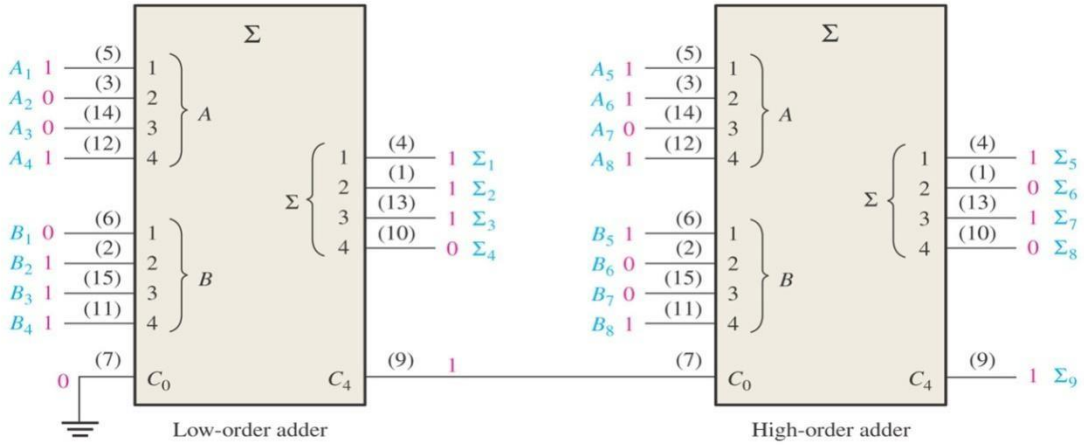
Adder expansion/8-Bit Adder: Two or more parallel-adder blocks can be connected (cascaded) to accommodate the addition of larger binary numbers.



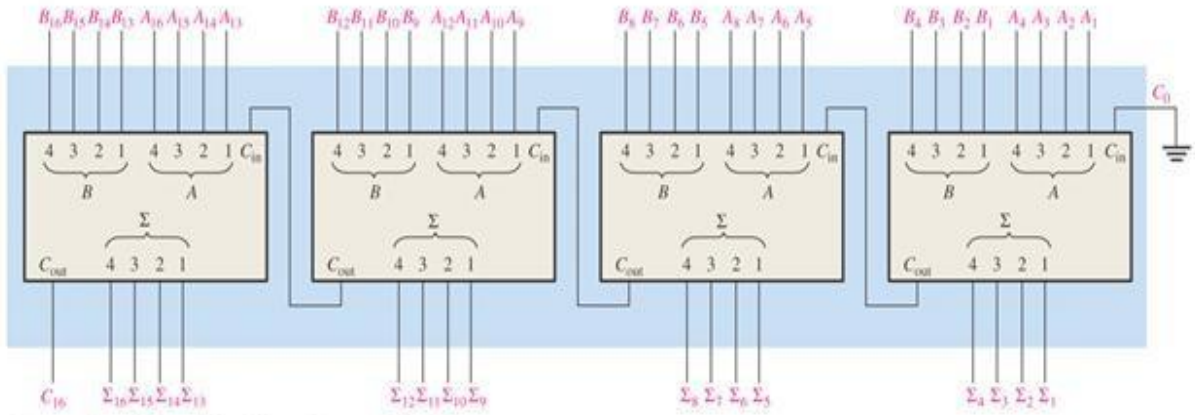
- The 4-bit parallel adder can be expanded to handle the addition of two 8-bit numbers by using two 4-bit adders.
- The carry input of the low-order adder (C0) is connected to ground because there is no carry into the least significant bit position, and the carry output of the low-order adder is connected to the carry input of the high-order adder, as shown in the above figure.
- This process is known as cascading.

- The low-order adder is the one that adds the lower or less significant four bits in the numbers, and the high-order adder is the one that adds the higher or more significant four bits in the 8-bit numbers

Two 74LS283 adders connected as an 8-bit parallel adder (pin numbers are in parentheses).
The following two 8-bit numbers are added.
$A_8A_7A_6A_5A_4A_3A_2A_1 = 10111001$ and $B_8B_7B_6B_5B_4B_3B_2B_1 = 10011110$

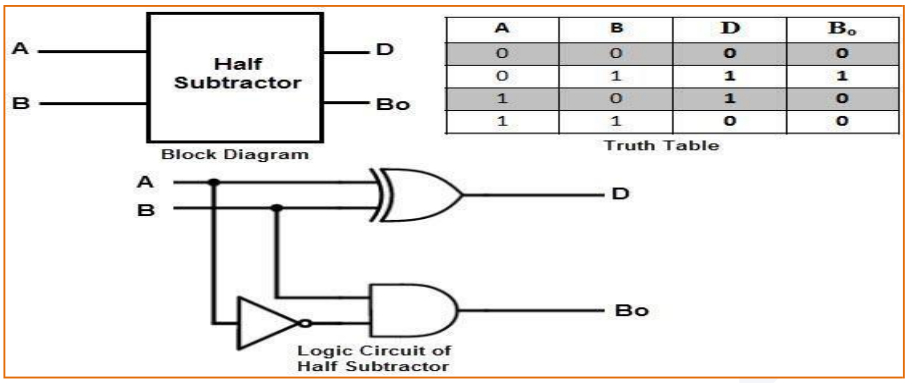


- **Similarly, four 4-bit adders can be cascaded to handle two 16-bit numbers.**



(b) Cascading of four 4-bit adders to form a 16-bit adder

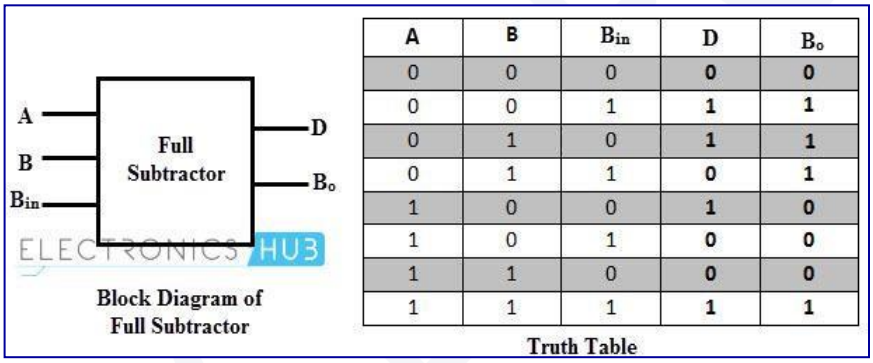
Half Subtractors : Half subtractor is a combinational circuit with two inputs and two outputs (difference and borrow). It produces the difference between the two binary bits at the input and also produces an output (Borrow) to indicate if a 1 has been borrowed.



A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

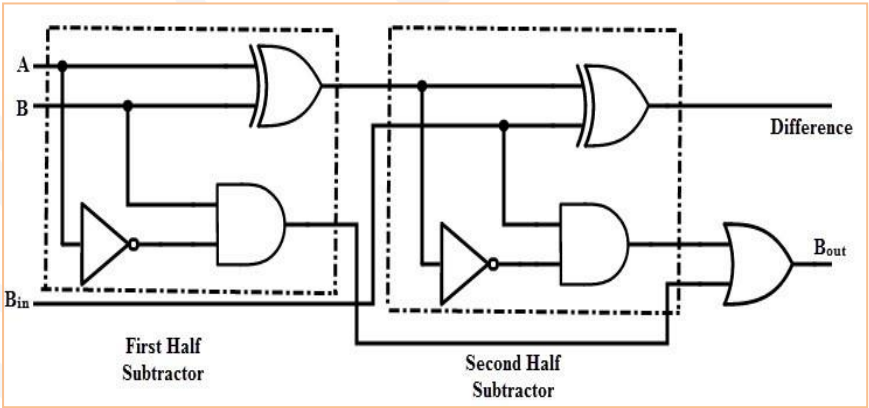
Truth Table

Full Subtractors : The disadvantage of a half subtractor is overcome by full subtractor. The full subtractor is a combinational circuit with three inputs A,B,C and two output D and C'. A is the 'minuend', B is 'subtrahend', C is the 'borrow' produced by the previous stage, D is the difference output and C' is the borrow output.



A	B	B_{in}	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

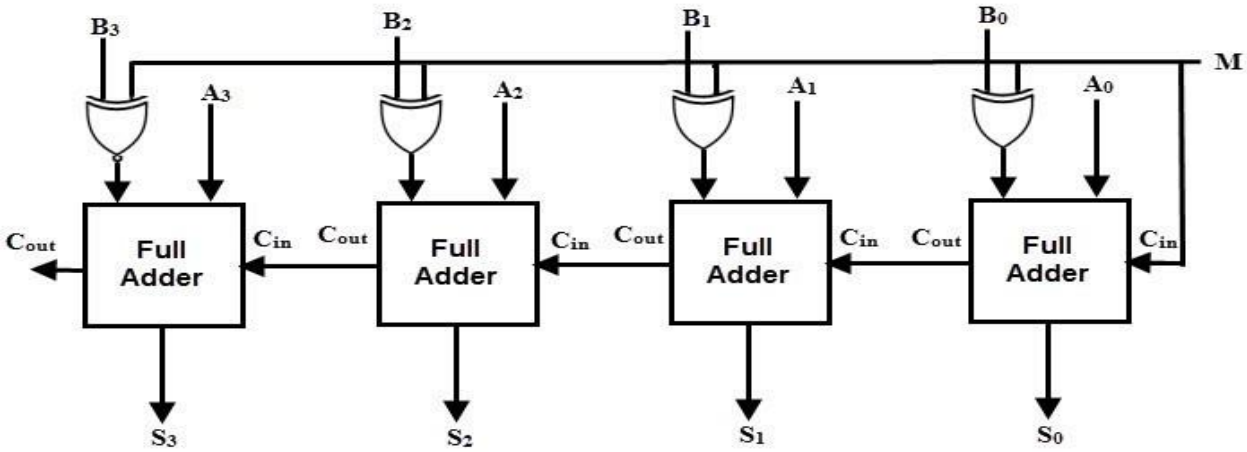
Truth Table



To perform the subtraction , we can use the 2's complements, so the subtraction can be converted to addition.

2's complement can be obtained by talking the 1's complement and adding 1 to the LSB bit. 1) 1's complement can be implemented with inventors. 2) 1 can be added to the sum through the input carry.

4-Bit Parallel Adder / Subtractor: 4-Bit Parallel Adder / Subtractor circuit can be constructed by using Full Adders and EX-OR gates as shown in the figure.



- The logic circuit has an additional input called the control input M, which determines the addition or subtraction.
- When M= 1, the circuit is a subtractor and when M=0, the circuit becomes adder.
- The Ex-OR gate consists of two inputs to which one is connected to the B and other to input M.
- When M = 0, B Ex-OR of 0 produce B. Then full adders add the B with A with carry input zero and hence an addition operation is performed.
- When M = 1, B Ex-OR of 0 produce B complement and also carry input is 1. Hence the complemented B inputs are added to A and 1 is added through the input carry, nothing but a 2's complement operation. Therefore, the subtraction operation is performed.

Magnitude Comparator: Magnitude comparator is a combinational circuit that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number.

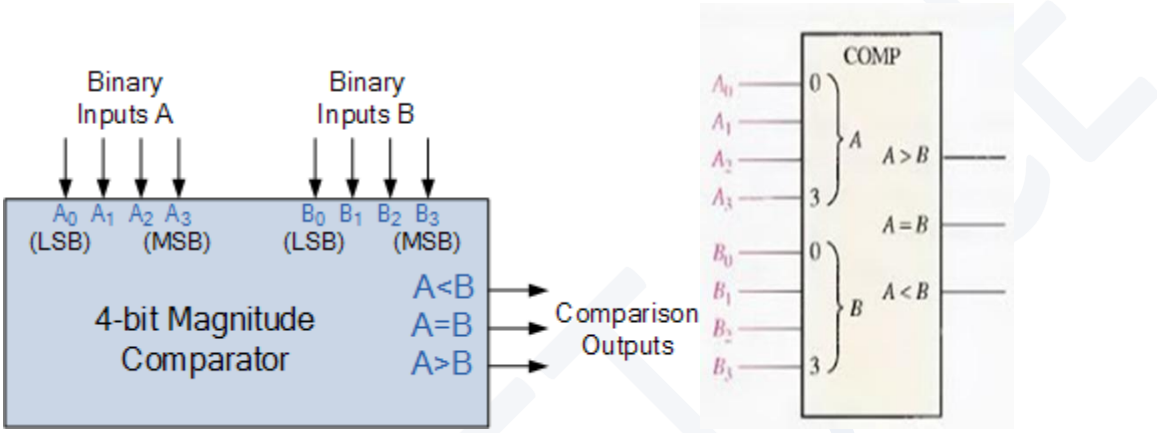
- The comparison of two numbers is an operation that determines if one number is greater than, less than, or equal to the other number.
- The outcome of the comparison is specified my three binary variables that indicate whether A>B, A=B, or A<B.

Truth table for a comparator:

A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1

1	0	1	0	0
1	1	0	1	0

4-bit Comparator: **T**wo 4-bit words ("nibbles") are compared to each other to produce the relevant output with one word connected to inputs A and the other to be compared against connected to input B as shown below.

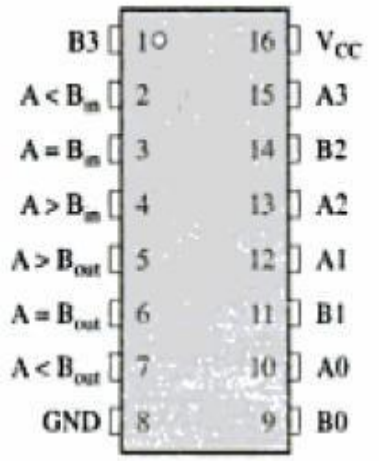


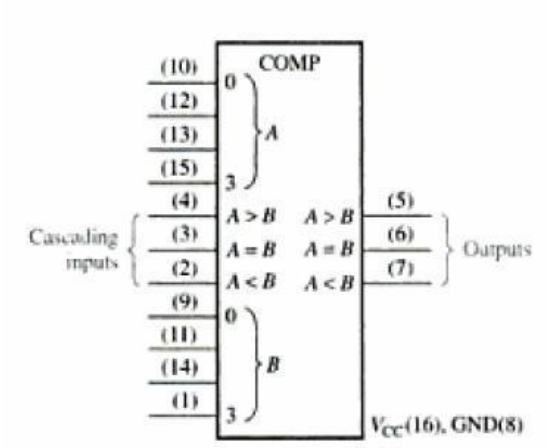
Logic symbol of 4-bit comparator

- To determine an inequality of binary numbers A and B, first examine the highest- order bit in each number.
- The following conditions are possible:
  If A3=1 and B3=0, then A>B.
  If A3 = 0 and B3 =1 then A<B.
  If A3 =B3 , examine the next lower bit position for an inequality. These three operations are valid for each bit position in the numbers.
- The general procedure used in a comparator is to check for an inequality in a bit position, starting with the highest-order bits (MSBs).
- Highest order indication must take precedence.

Some commercially available digital comparators such as the TTL 74HC85 is 4-bit magnitude comparator have additional input terminals that allow more individual comparators to be "cascaded" together to compare words larger than 4-bits with magnitude comparators of "n"-bits being produced. These cascading inputs are connected directly to the corresponding outputs of the previous comparator as shown to compare 8, 16 or even 32-bit words.

74HC85 is a 4-bit comparator: The pin diagram and logic diagram of 74HC85 is shown in the figure



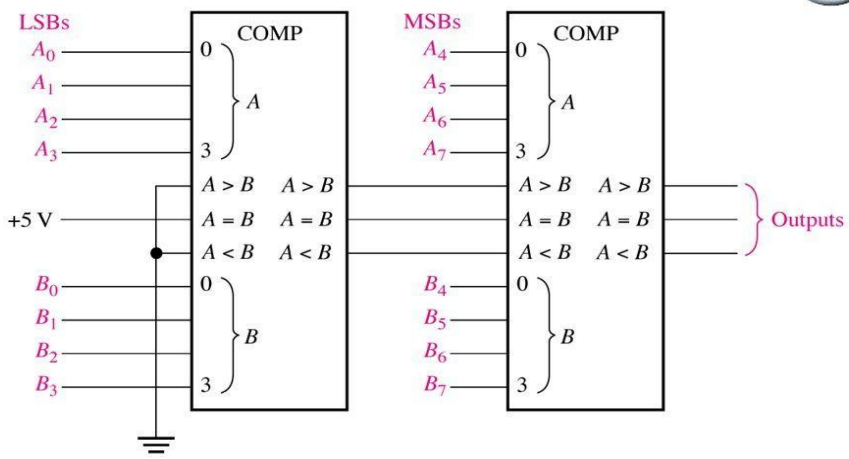


Comparator expansion/8-bit comparator:

- The above device has got 3 cascading inputs, A < B, A = B, A > B. These inputs allow several comparators to be cascaded for comparison of any number of bits greater than four.
- To expand the comparator, the A < B, A = B and A > B outputs of the lower order comparator are connected to the corresponding cascading inputs
  of the next higher-order comparator.
- The lowest order comparator must have a HIGH on the A = B input and LOWs on the A < B and A > B inputs

Two 74HC85s are required to compare two 8-bit numbers. They are connected as shown in the figure in a cascaded arrangement.

An 8-bit magnitude comparator using two 4-bit comparators.

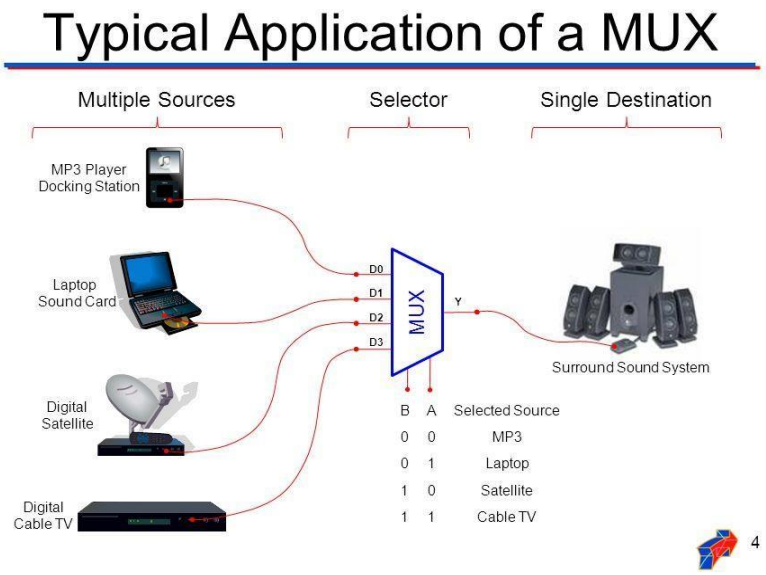


8 bit comparator truth table:

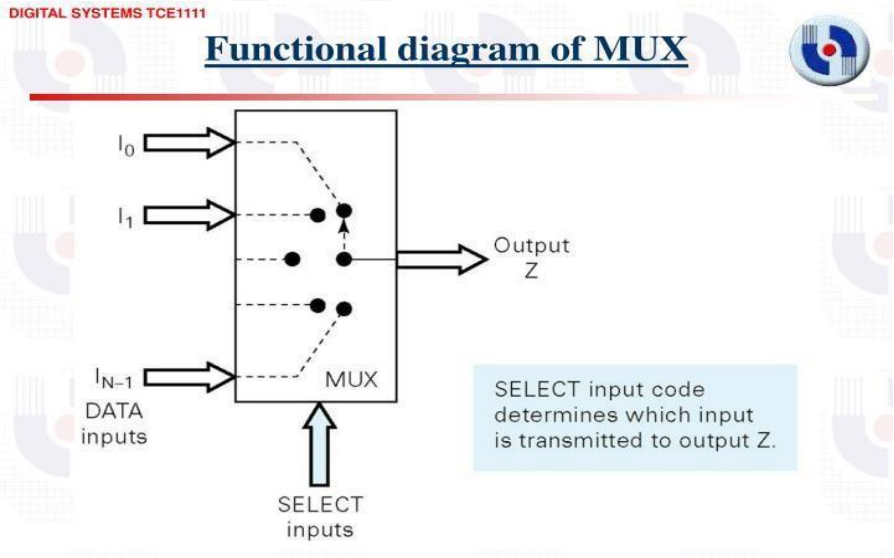
Inputs		Outputs		
A	B	A<B	A=B	A>B
00001100	00001100	0	1	0
00001010	00010001	1	0	0
00001111	00000101	0	0	1
00011000	00011000	0	1	0

Multiplexer (Data Selectors):

- A multiplxer(MUX) is a CLC that allows digital information(data) from several sources to be routed onto a single line for transmission over that line to a common destination.
- The basic multiplxer has several data-input lines and a single output line.
- It also has **data-select inputs**, which permit digital data on **any one of the inputs to be switched to the single output line**

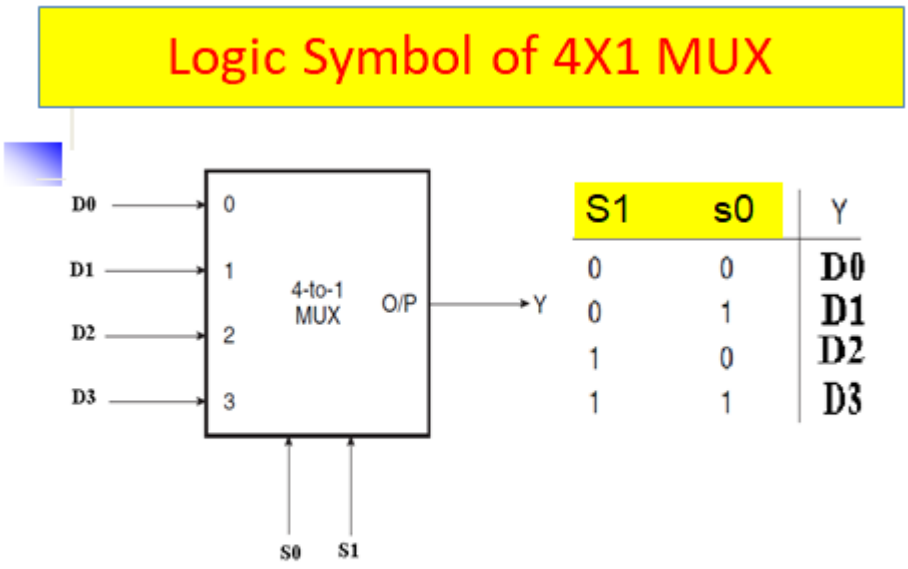


Multiplexers operate like very fast acting multiple position rotary switches connecting or controlling multiple input lines called “channels” one at a time to the output.

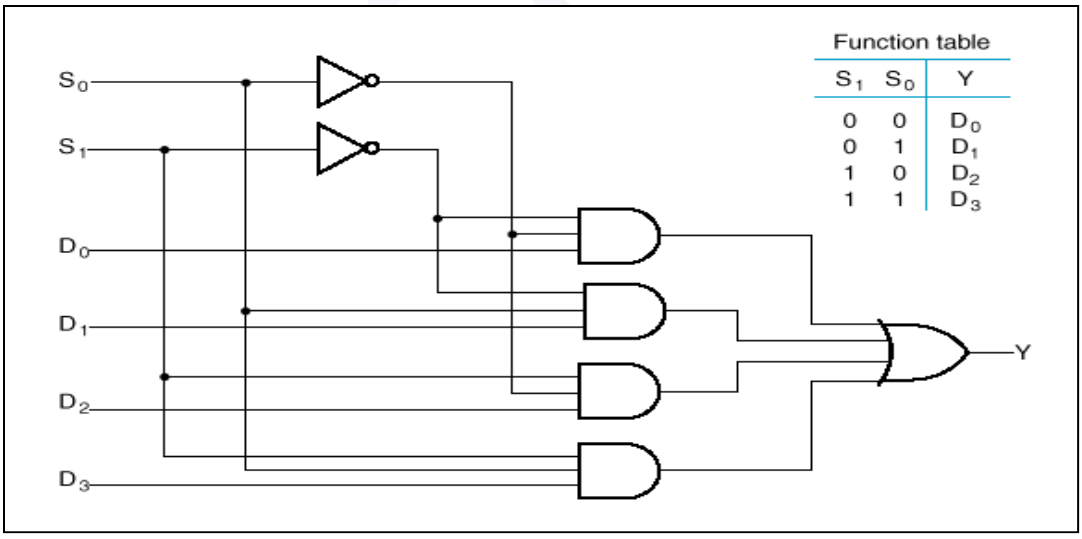


Multiplexing is the generic term used to describe the operation of sending one or more analogue or digital signals

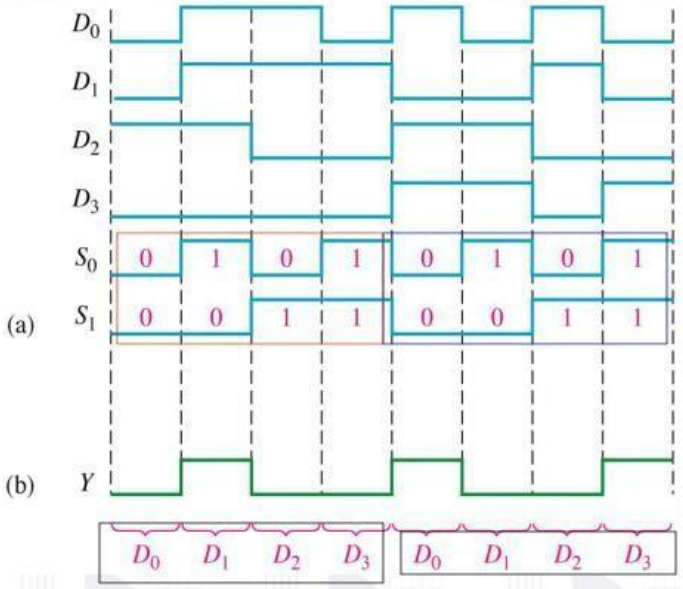
over a common transmission line at different times or speeds and as such, the device we use to do just that is called a **Multiplexer**.



Logic diagram of 4X1 MUX:



Output Waveforms in relation with the Data-Input and Data-Select waveforms - 4-input MUX

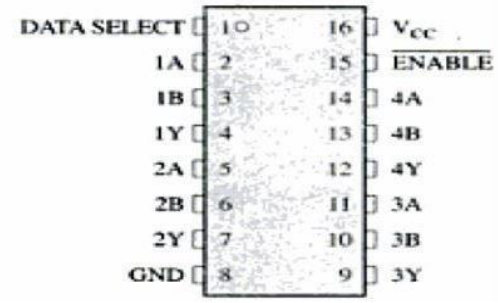


The binary state of the data-select inputs during each interval determines which data input is selected. Here the data-select inputs go through a repetitive binary sequence 00,01,10,11,00, and so on. The resulting output waveform is shown.

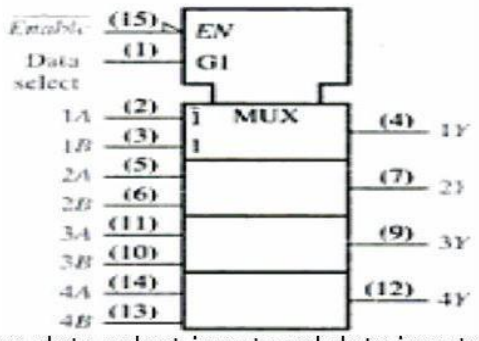
Quad 2-input Multiplexer-IC 74HC157

- It contains 4-separate 2-input multiplexers.
- All the multiplexers share common data select line and a common Enable.
- $\overline{Enable}$ =LOW, allows selected input data to pass through to the output.
- $\overline{Enable}$ =HIGH, prevents data from going through to the output (disables the multiplexer).

Pin Diagram



Logic Diagram



- G1=indicates AND relationship between data select input and data inputs.
- When data slect=HIGH, B inputs of the multiplexer are selected.
- When data slect=LOW, A inputs of the multiplexer are selected

74LS151 8X1 Multiplexer :

- The 74LS151 has eight data inputs (D0 – D7) and, therefore, three data select or address input lines (S0 – S2)
- Three bits are required to select any one of the eight data inputs.
- A LOW on the Enable input allows the selected input data to pass through to the output.
- Notice that the data output and its complement both are available.

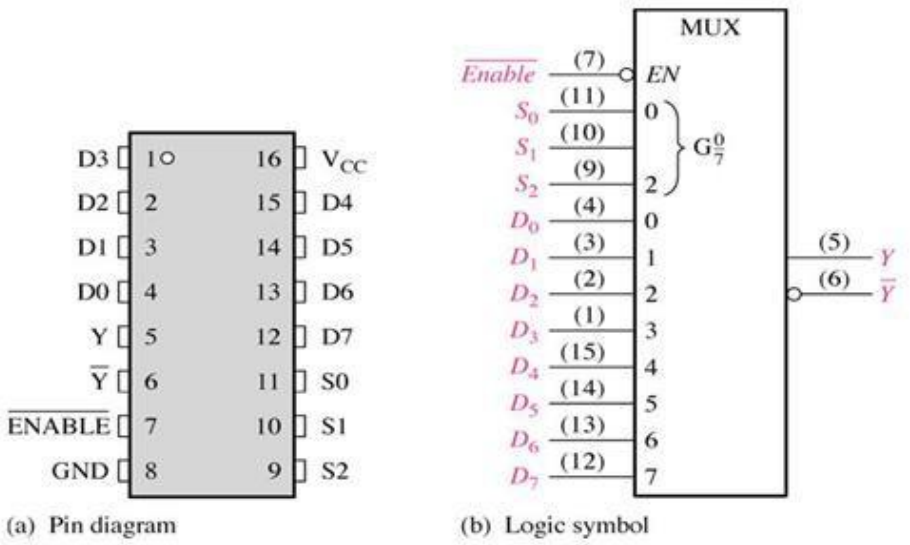


Figure Pin diagram and logic symbol for the 74LS151 8-input data selector/multiplexer.

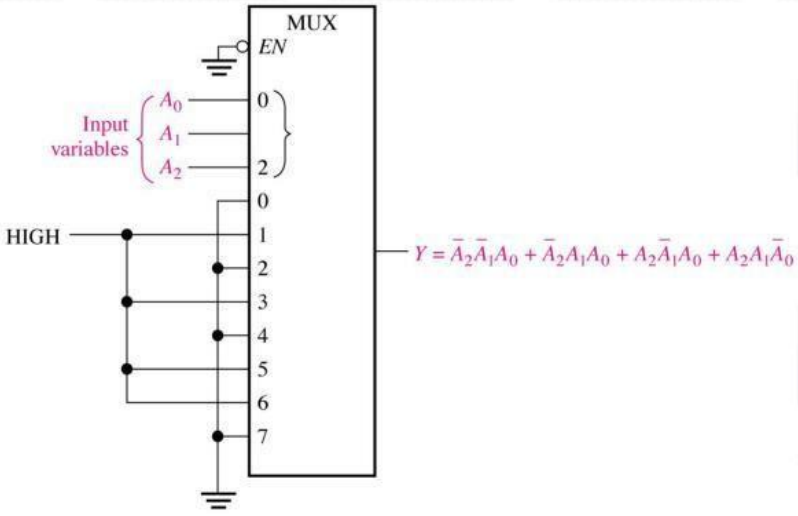
LOGIC FUNCTION GENERATION USING MUX

Exercise 1:

Implement the logic circuit function specified in the table given below by using 74LS151 8-input data selector/multiplexer.

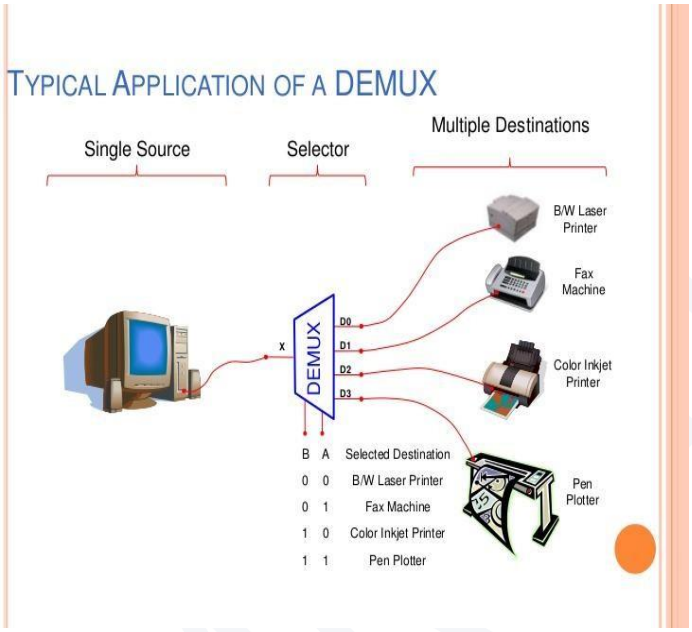
Input			Output	
A2	A1	A0	Y	
0	0	0	0	0
0	0	1	1	1
0	1	0	0	2
0	1	1	1	3
1	0	0	0	4
1	0	1	1	5
1	1	0	1	6
1	1	1	0	7

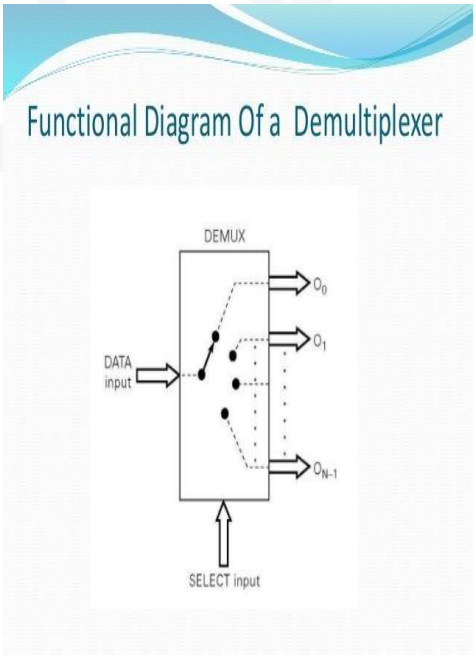
Solution :



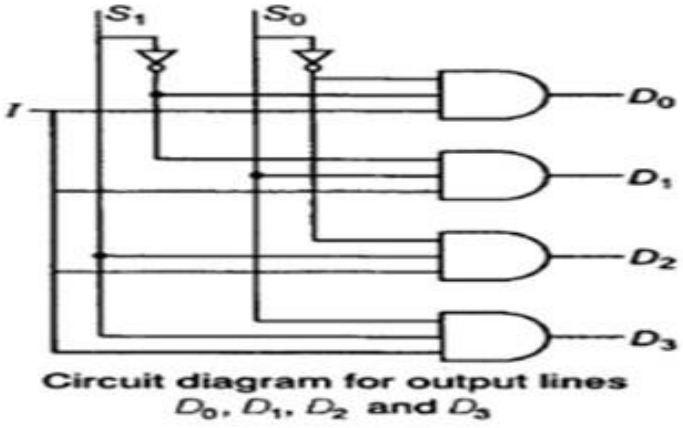
Demultiplexer(DEMUX) :

- A demultiplexer (DEMUX) basically reverses the multiplexing function.
- A demultiplexer (or demux) is a device that takes a single input line and routes it to one of several digital output lines.
- A demultiplexer of 2^n outputs has n select lines, which are used to select which output line to send the input.
- A demultiplexer is also called a data distributor.





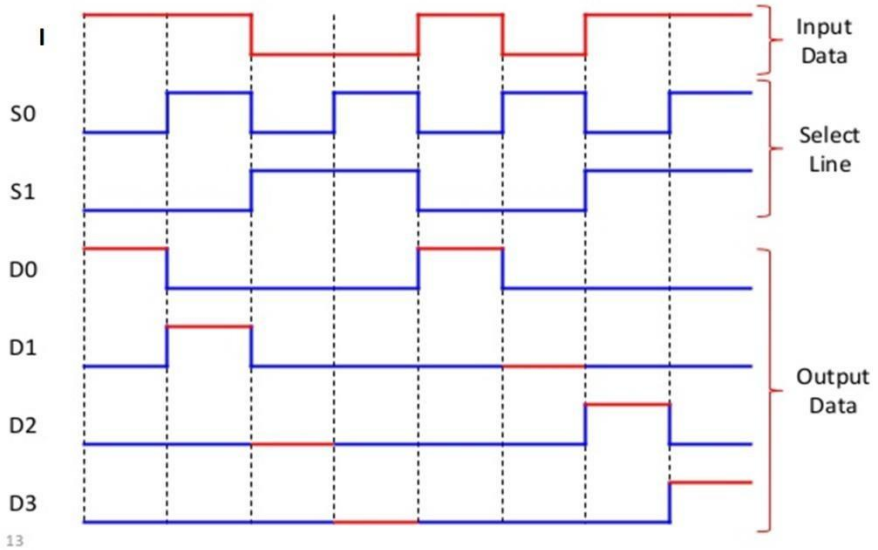
Logic Diagram of 1X4 DEMUX



Circuit diagram for output lines D_0, D_1, D_2 and D_3

Input	Select Lines	Output Lines
I	S_1 S_0	D_0 D_1 D_2 D_3
I	0 0	1 0 0 0
I	0 1	0 1 0 0
I	1 0	0 0 1 0
I	1 1	0 0 0 1

1-to-4 De-Multiplexer Waveforms



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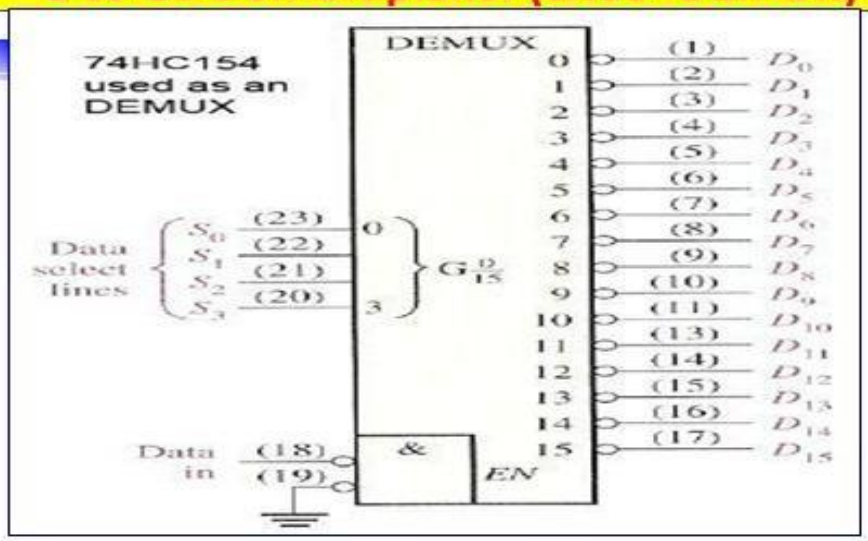
74HC154
1-to-16 Demultiplexer (1X16 DEMUX)



Decoders: **Decoder** is a combinational **logic** circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs.

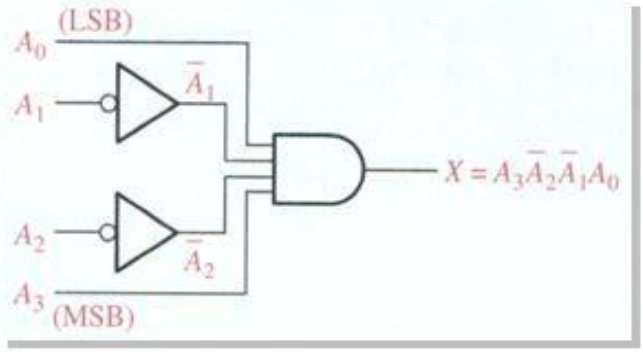
- The basic function of a decoder is to detect the presence of a specified combination of bits (code) on its inputs and to indicate the presence of that code by a specified output level.
- In its general form, a decoder has n input lines to handle n bits and from one to 2^n output lines to indicate the presence of one or more n-bit combinations.

The Basic Binary Decoder :

- Suppose, you need to determine when a binary 1001 occurs on the inputs of a digital circuit.
- An AND gate can be used as the basic decoding element because it produces a HIGH output only when all of its inputs are HIGH.
- Therefore, you must make sure that all of the inputs to the AND gate are HIGH when the Binary number 1001 occurs.

- **Binary decoder output is 1 only when:**

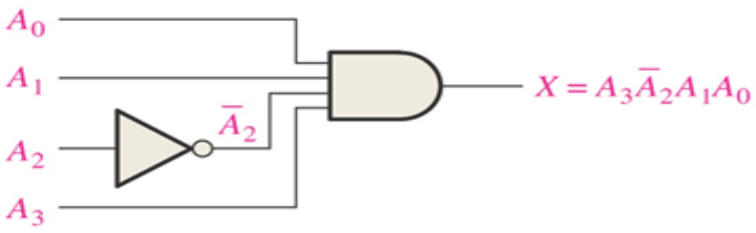
$A_0 = 1$
$A_2 = 0$
$A_3 = 0$
$A_4 = 1$



- **The logic equation for the decoder is developed as illustrated in the Figure.**
- The output is 0 except when A0=1, A1=0, A2=0, and A3=1 are applied to the input.

This is only one of an infinite number of examples

- Determine the logic required to decode the binary number 1011 by producing a HIGH level on the output. LSB = A_0 (right most)
- $A_0 = 1, A_1 = 1, A_2 = 0, A_3 = 1$
- $X = A_3\bar{A}_2A_1A_0$



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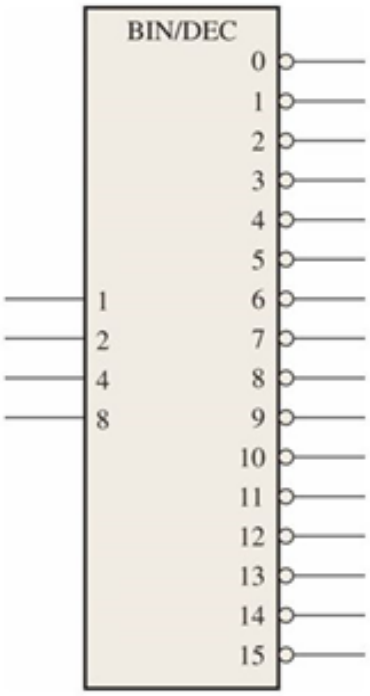
4-Bit Decoder:

- In order to decode all possible combinations of four bits, sixteen decoding gates are required (2^4 = 16)
- This type of decoder is commonly called either a 4-line-to-16-line decoder because there are four inputs and sixteen outputs or a 1-of-16-decoder because for any given code on the inputs, one of the sixteen outputs is activated.

Truth Table of 4-line-to-16-line decoder: **A list of sixteen binary codes and their corresponding decoding functions is given in Table.**

BINARY INPUTS				DECODING	OUTPUTS														
A_3	A_2	A_1	A_0	FUNCTION	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	$\bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	$\bar{A}_3\bar{A}_2\bar{A}_1A_0$	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	$\bar{A}_3\bar{A}_2A_1\bar{A}_0$	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	$\bar{A}_3\bar{A}_2A_1A_0$	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	$\bar{A}_3A_2\bar{A}_1\bar{A}_0$	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	1	0	1	$\bar{A}_3A_2\bar{A}_1A_0$	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	0	$\bar{A}_3A_2A_1\bar{A}_0$	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	1	1	1	$\bar{A}_3A_2A_1A_0$	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	0	0	0	$A_3\bar{A}_2\bar{A}_1\bar{A}_0$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	1	$A_3\bar{A}_2\bar{A}_1A_0$	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
1	0	1	0	$A_3\bar{A}_2A_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	1	1	$A_3\bar{A}_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1	1	0	0	$A_3A_2\bar{A}_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	1	$A_3A_2\bar{A}_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	0	$A_3A_2A_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	$A_3A_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Logic symbol of 4-line-to-16-line decoder



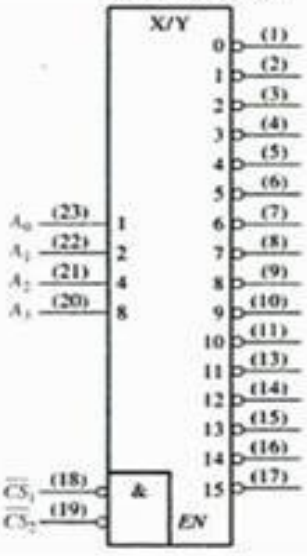
- The logic symbol of 4-line-to-16-line decoder with active low outputs
- The BIN/DEC label indicates that the binary input makes the corresponding decimal output active low

$A_3A_2A_1A_0$ Output
0 1 1 0 6 is low, all other outputs are high

74HC154
4-line-to-16-line decoder

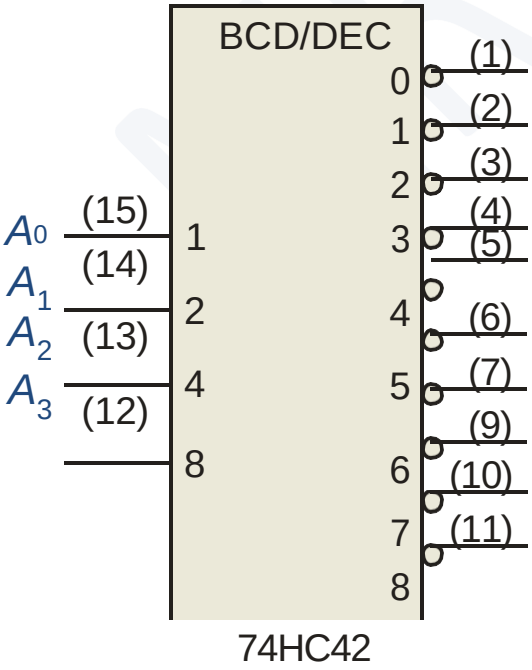
Pin Diagram

Logic Diagram



- EN(enable input): It is implemented with a NOR gate used as a negative-AND.
- If $\overline{CS1}$ *and* $\overline{CS2}$=LOW, makes EN=HIGH and the enable gate output is connected to input of each NAND gate in decoder, so it must be HIGH for the NAND gates to be enabled.
- IF EN=not activated by a LOW on both inputs, then all sixteen decoder output (Y) will be HIGH regardless of the states of four input variables A0, A1, A2 and A3

BCD-to-Decimal Decoder: BCD-to-decimal decoders accept a binary coded decimal input and activate one of ten possible decimal digit indications.

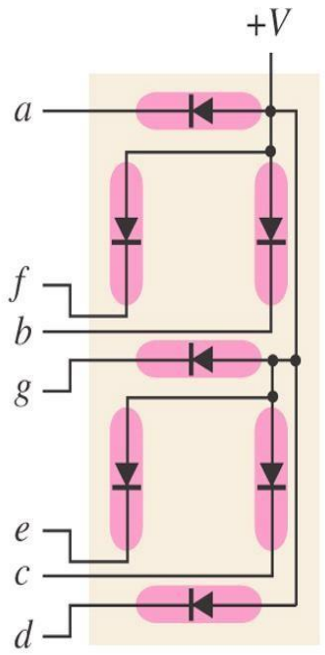


DECIMAL DIGIT	BCD CODE A_3	A_2	A_1	A_0	DECODING FUNCTION
0	0	0	0	0	$\overline{A}_3\overline{A}_2\overline{A}_1\overline{A}_0$
1	0	0	0	1	$\overline{A}_3\overline{A}_2\overline{A}_1A_0$
2	0	0	1	0	$\overline{A}_3\overline{A}_2A_1\overline{A}_0$
3	0	0	1	1	$\overline{A}_3\overline{A}_2A_1A_0$
4	0	1	0	0	$\overline{A}_3A_2\overline{A}_1\overline{A}_0$
5	0	1	0	1	$\overline{A}_3A_2\overline{A}_1A_0$
6	0	1	1	0	$\overline{A}_3A_2A_1\overline{A}_0$
7	0	1	1	1	$\overline{A}_3A_2A_1A_0$
8	1	0	0	0	$A_3\overline{A}_2\overline{A}_1\overline{A}_0$
9	1	0	0	1	$A_3\overline{A}_2\overline{A}_1A_0$

BCD-to-7-segement decoder: **BCD to Seven Segment decoder** is a combinational logic circuit that accepts a decimal digit in **BCD** (input) and generates appropriate outputs for the 7-**segments** to **display** the input decimal digit.

Truth Table:

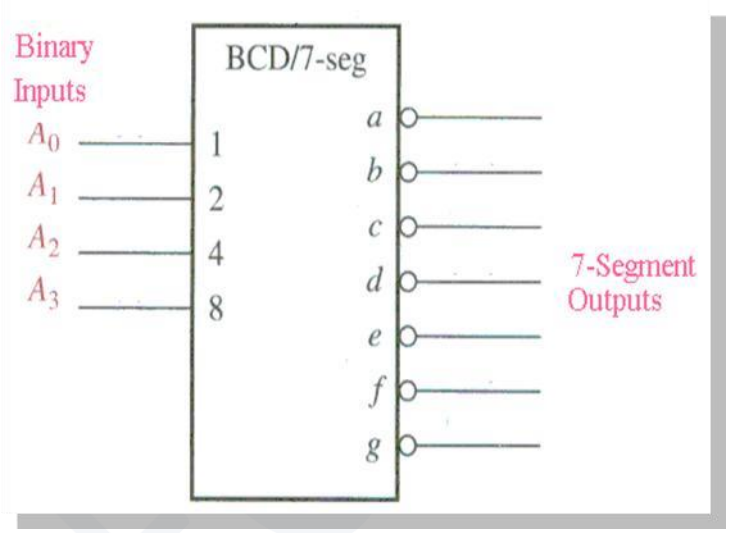
DECIMAL DIGIT	INPUTS				SEGMENT OUTPUTS						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	1	0	1	0	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X
12	1	1	0	0	X	X	X	X	X	X	X
13	1	1	0	1	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	X	X
15	1	1	1	1	X	X	X	X	X	X	X



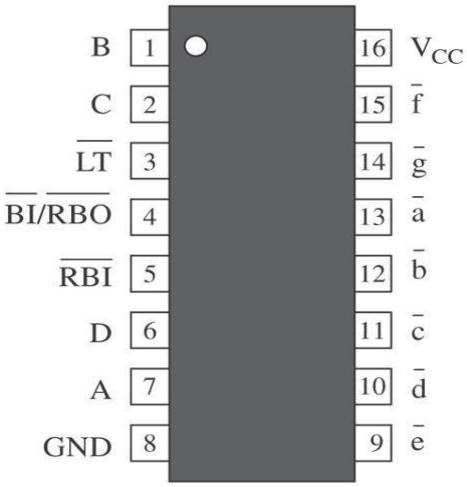
Common-anode

Common Anode has all anodes of LEDs tied to +V

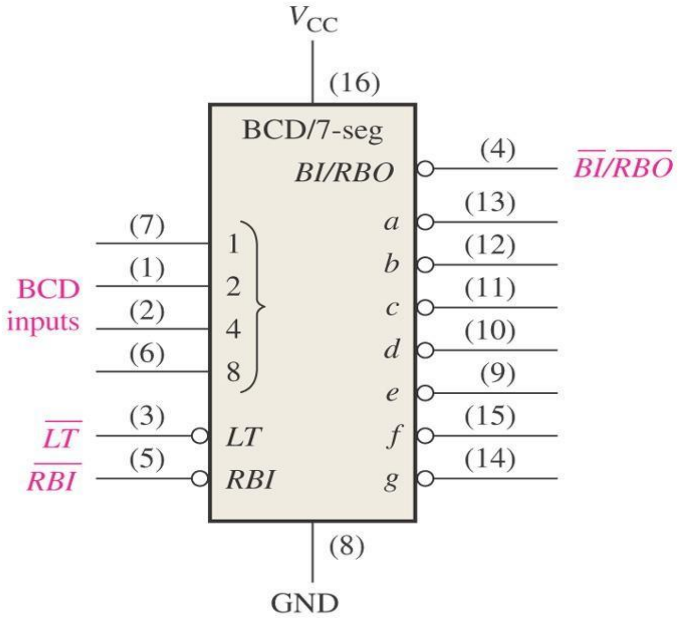
Logic diagram of BCD-to-7-Segment Decoder:



74LS47 BCD-to-7-segment



(a) Pin diagram



(b) Logic symbol

decoder:

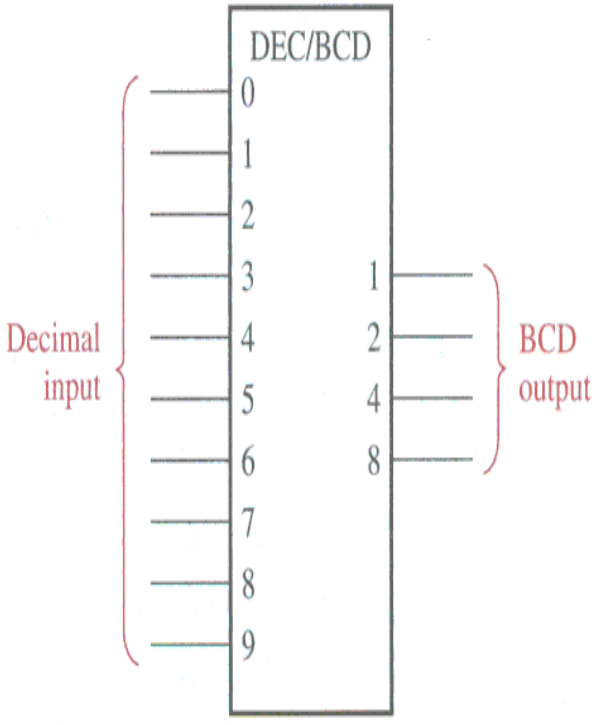
$\overline{LT}$ = Lamp Test - when LOW and BI/RBO is HI then all LEDs are ON
$\overline{BI}$ = Blanking Input
$\overline{RBI}$ = Ripple Blanking Input
RBO = Ripple Blanking Output

- BCD Inputs (D-A)
- 7-segment Outputs (*a* -*g*)

Encoders:

- An encoder is a combinational logic circuit that essentially performs a “reverse” decoder function.
- An encoder is a device or a combinational circuit that converts information from one format or code to another.
- Digital Encoder are more commonly called a Binary Encoder takes all its data inputs one at a time and then converts them into a single encoded output.
- An "n-bit" binary encoder has 2^n input lines and n-bit output lines
- An encoder accepts an active level on one of its inputs representing a digit, such as a decimal or octal digit, and converts it to a coded output such as BCD or binary.
- Encoders can also be devised to encode various symbols and alphabetic characters.
- The process of converting from familiar symbols or numbers to a coded format is called encoding

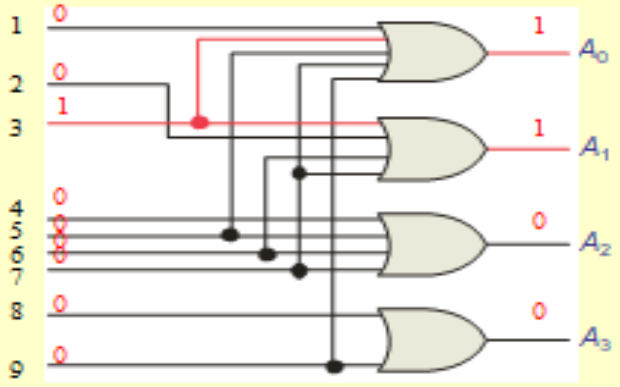
Decimal-to-BCD encoder (10 inputs, 4 outputs) : This type of encoder has ten inputs – one for each decimal digit and four outputs corresponding to the BCD code, as shown in figure. This is a 10-line-to-4-line encoder.



DECIMAL DIGIT	BCD CODE A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Example:

- **Show how the decimal-to-BCD encoder converts the decimal number 3 into a BCD 0011.**

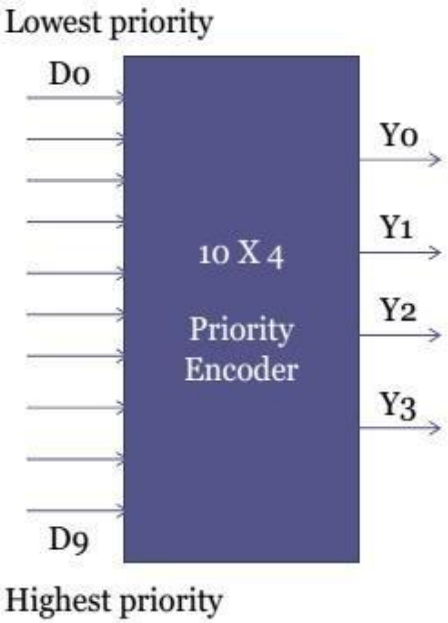


Priority Encoder:

- A priority encoder is a special type of encoder whose output corresponds to the currently active input which has the highest priority.
- So when an input with a higher priority is present, all other inputs with a lower priority will be ignored.
- They are two types
  (a) 10-to-4 bit priority encoder
  (b) 8-to-3 bit priority encoder

(a) 10-to-4 bit priority encoder: The priority function means that the encoder will produce a BCD output corresponding to the highest order decimal digit input that is active and will ignore any other lower-order active inputs.

10 to 4 priority encoder

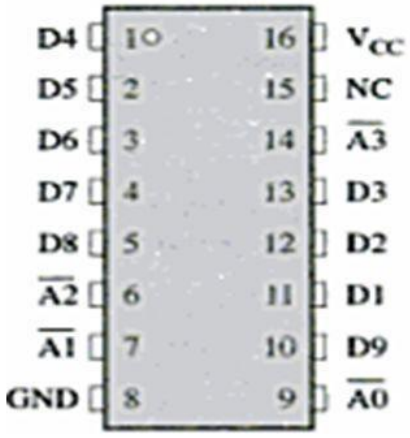


Input										Output			
D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0	1

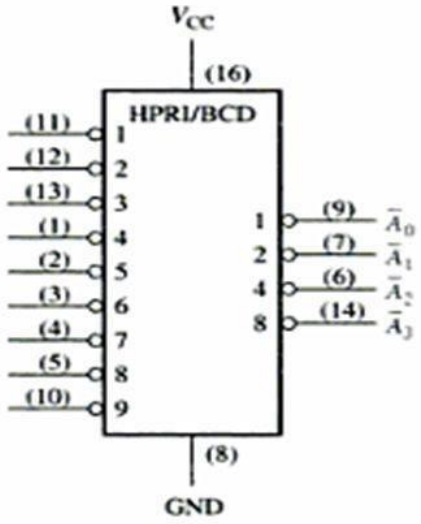
74HC147- priority encoder

- It is also called as 10-line-to-4-line encoder.
- 74HC147 is a priority encoder with active-low inputs (0) for decimal digits 1 to 9 and active-low BCD outputs.

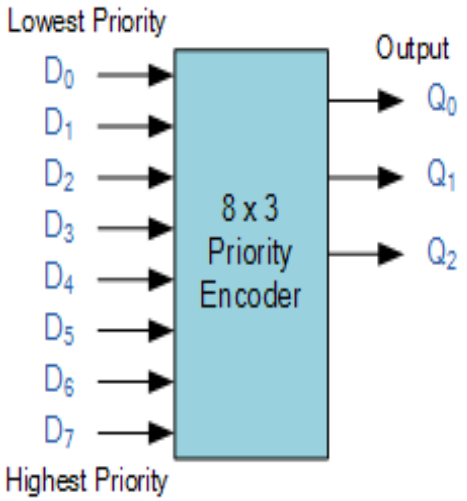
Pin Diagram-74147



Logic Diagram-74147



(b) 8-to-3 bit priority encoder:

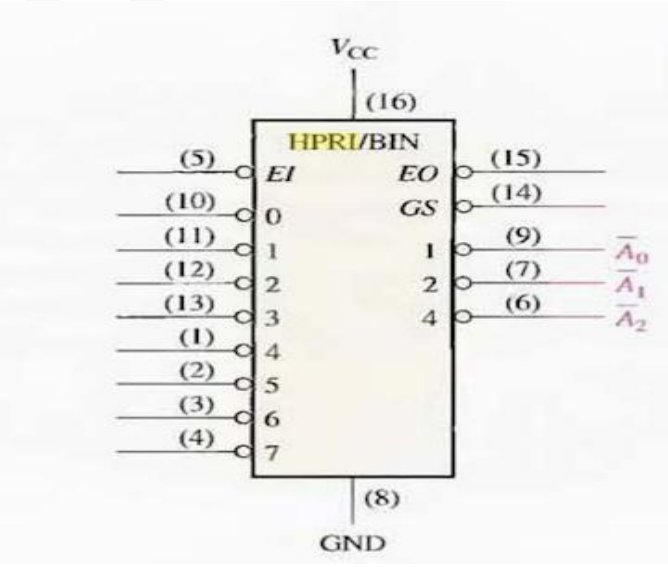


Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

X = dont care

74LS148 is 8-line-to-3-line encoder: It is priority encoder has eight active-LOW inputs and three active-LOW binary outputs. This is used to convert octal inputs to a 3-bit binary code.

To enable the device ,the EI (Enable input) must be low .It also has EO (Enable Output) and GS output for expansion purpose.



Code Converters:

- Binary-Gray and Gray-Binary conversion
- BCD-to-binary conversion

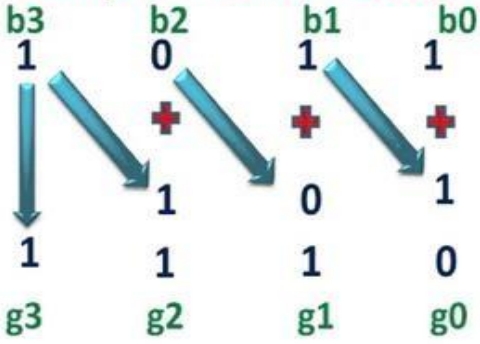
The Gray Code:

- The gray code is unweighted code and no specific weights assigned to the bit positions.
- The important feature of the Gray code is that it exhibits only a single bit change from one code word to the next in sequence.
- This property is an important one in many applications, such as shaft position encoders, where error susceptibility increases with the number of bit changes between adjacent numbers in a sequence.

Decimal Number	4 bit Binary Number ABCD	4 bit Gray Code $G_1G_2G_3G_4$
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0
8	1 0 0 0	1 1 0 0
9	1 0 0 1	1 1 0 1
10	1 0 1 0	1 1 1 1
11	1 0 1 1	1 1 1 0
12	1 1 0 0	1 0 1 0
13	1 1 0 1	1 0 1 1
14	1 1 1 0	1 0 0 1
15	1 1 1 1	1 0 0 0

Binary to Gray Code Conversion: The MSB in the Gray code is the same as the corresponding MSB in the Binary number 2. Going from left to right, add each adjacent pair of binary code bits to get the next Gray code bit. Discard carries

Example = convert 1011 binary to gray



A ⊕ B

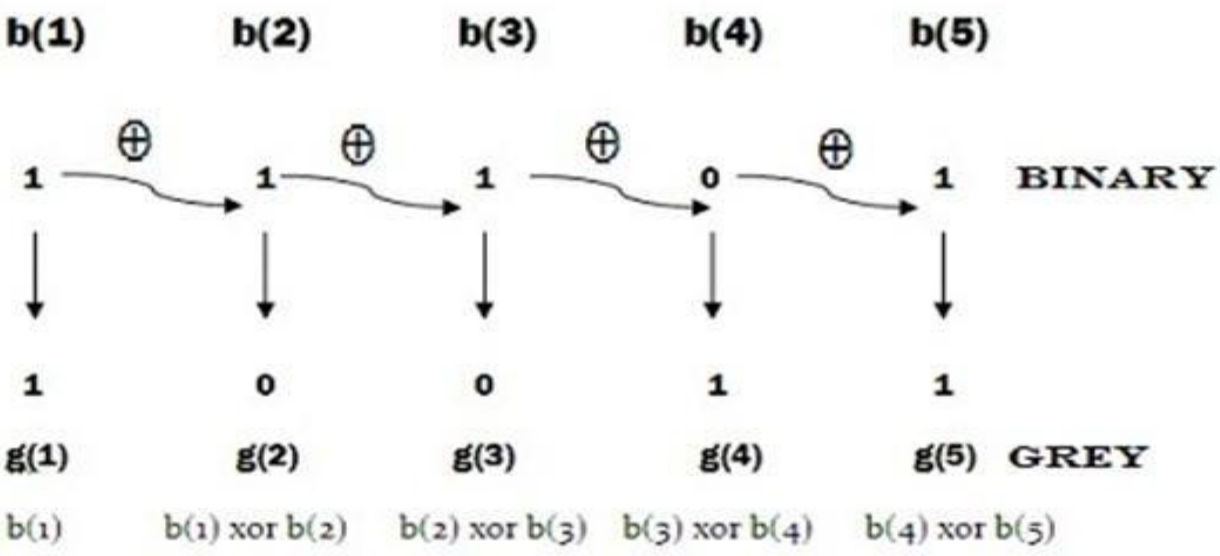
A	B	Y=AB'+A'B
0	0	0
0	1	1
1	0	1
1	1	0

MSB write as it is

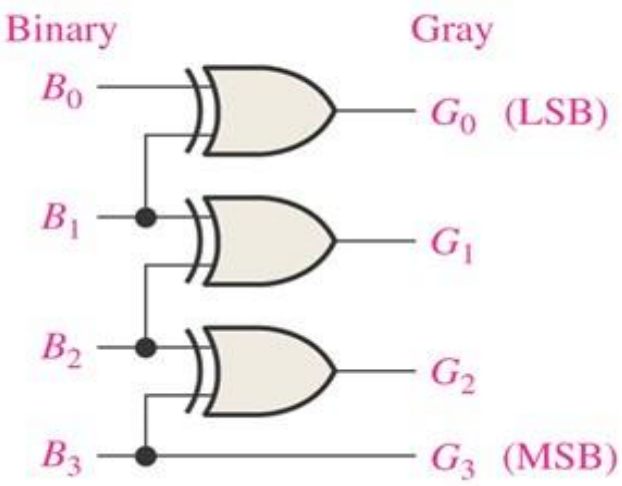
Add MSB in next bit neglect carry if produce

We can represent it as X-OR (odd 1's detector)

Convert the binary 11101_2 to its equivalent Grey code



Four-bit binary-to-Gray conversion logic.



Convert 1 1 0 0 to Gray

1 0 1 0

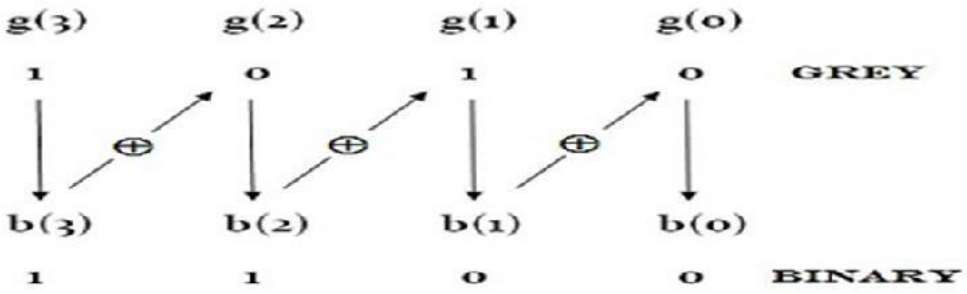
XOR

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

Gray-Binary code conversion:

- The MSB in the Binary code is the same as the corresponding bit in the Gray code
- Add each Binary code bit generated to the Gray code bit in the next adjacent position. Discard carries.

Convert the Grey code 1010 to its equivalent Binary

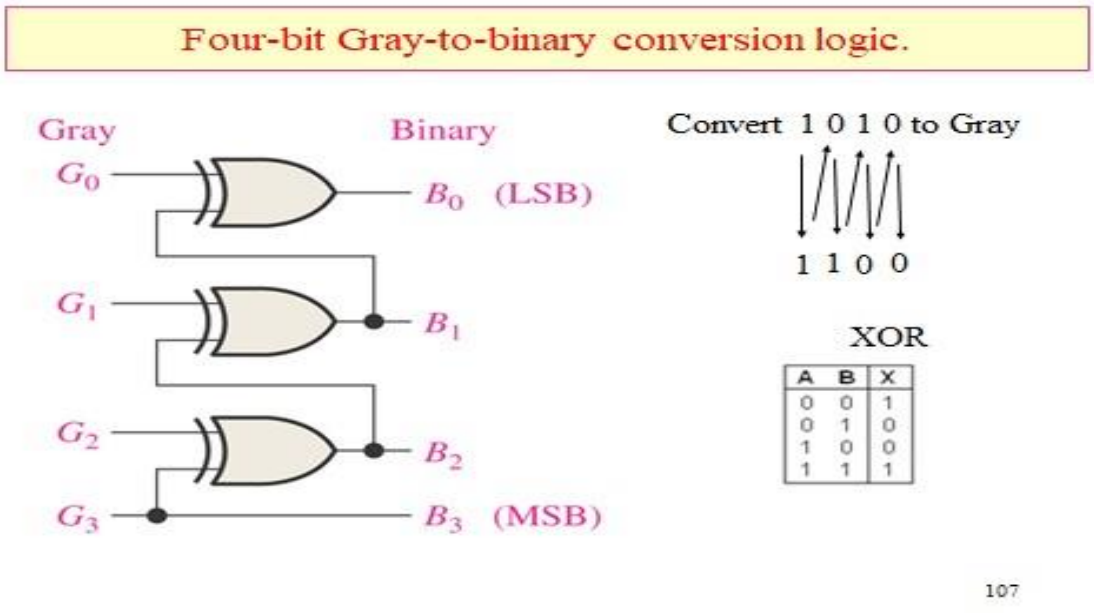


i.e $b(3) = g(3)$

$b(2) = b(3) \oplus g(2)$

$b(1) = b(2) \oplus g(1)$

$b(0) = b(1) \oplus g(0)$



BCD to Binary Conversion:

• One method of BCD-to-Binary code conversion uses adder circuits. The basic conversion process is as follows.

1. The value, or weight, of each bit in the BCD number is represented by a Binary number.
2. All of the Binary representations of the weights of bits that are 1s in the BCD number are added.
3. The result of this addition is the Binary equivalent of the BCD number.

• A more concise statement of this operation is

– The Binary numbers representing the weights of the BCD bits are summed to produce the total Binary number

Let's take a decimal number 87. This can be written as 8 71000 0111

The left most 4-bit group represents 80 and the right most 4-bit group represents 7

• That is, the left most group has a weight of 10,and the right most group has weight of 1.

• Within each group, the binary weight of each bit is as follows.

	Tens Digit				Units Digit			
Weight:	**80**	**40**	**20**	**10**	**8**	**4**	**2**	**1**
Bit designation:	**B3**	**B2**	**B1**	**B0**	**A3**	**A2**	**A1**	**A0**

• If the binary representations for the weights of all the 1s in the BCD number are added, the result is the Binary number that corresponds to the BCD number.

Example: Convert the BCD number 0001 0101 (decimal 15) and 1001 0110 (decimal 96) to Binary.

Solution: Write the Binary representations of the weights of all 1s appearing in the numbers, and then add them together

	80	40	20	10	8	4	2	1
Decimal 15	0	0	0	1	0	1	0	1
Decimal 96	1	0	0	1	0	1	1	0

Binary number for Decimal 15 is 00000001 for 96 is 00000010

```
  00000100      00000100
  00001010      00001010
  --------      01010000
  00001111      ---------
  --------      01100000
                --------
```

Parity Generators/Checkers:

- Errors can occur as digital codes are being transferred from one point to another with in a digital system.
- The errors take the form of undesired changes in the bits that make up the coded information; that is, a 1 can change to a 0, or a 0 to a 1, because of component malfunctions or electrical noise.
- In most digital systems, the probability that even a single bit error will occur is very small, and the likelihood that more than one will occur is even smaller. Nevertheless, when an error occurs undetected, it can cause serious problems in a digital system.
- One method of error detections is to use parity.
- A parity bit is attached to a group of data in order to make the total number of 1s either even or odd.

Example The data is 1010011. Show the parity bit for the data with odd and even parity.

Solution data with odd parity = 11010011
data with even parity = 01010011

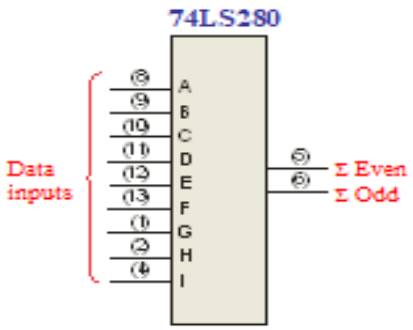
74LS280
9-bit Parity Generators/Checkers

- 74LS280 9-bit parity generator/checker (8 bits+1 parity bit)

- Checker:

# of 1s on inputs	Σ Even	Σ Odd
0,2,4,6,8	H	L
1,3,5,7,9	L	H

Generator: To generate even parity, the parity bit is taken from the odd parity output. To generate odd parity, the output is taken from the even parity output.



110

- This particular device can be used to check for odd or even parity on a 9-bit code (eight data bits and one parity bit) or it can be used to generate a parity bit for a binary code with up to nine bits.
- The inputs are A through I; when there is an even number of 1s on the inputs, the ΣEVEN output is HIGH and the ΣODD output is LOW.
- When this device is used as an even parity checker, the number of input bits should always be even; and when a parity error occurs, the ΣEVEN output goes LOW and the ΣODD output goes HIGH.
- When it is used as an odd parity checker, the number of input bits should always be odd; and when a parity error occurs, the ΣODD output goes LOW and the ΣEVEN output goes HIGH

Parity Generator:

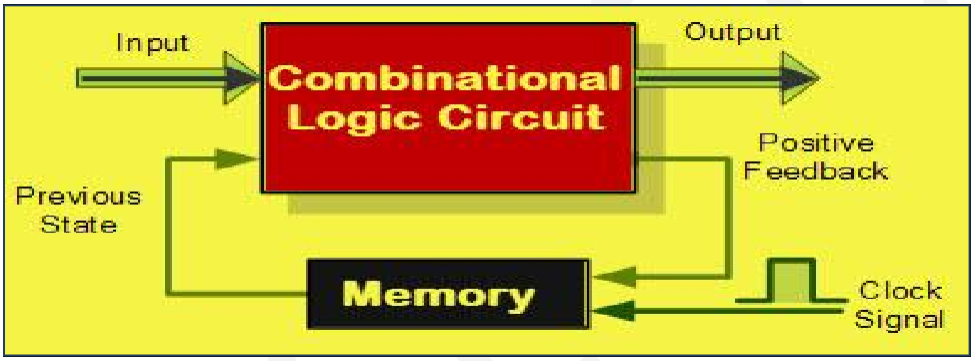
- If this device is used as an even parity generator, the parity bit is taken as the ΣODD output because this output is a 0 if there is an even number of input bits and it is a 1 if there is an odd number.
- When used as an odd parity generator, the parity bit is taken as the ΣEVEN output, because it is a 0 when the number of input bits is odd.

Unit 5

Sequential logic ICs and Memories

Sequential logic circuits:

- The main characteristic of combinational logic circuits is that their output values depend on their present input values.
- Sequential logic circuits differ from combinational logic circuits because they contain memory elements so that their output values depend on both present and past input values
- The circuit whose output at any instant depends not only on the input present but also on the past output a is known as sequential circuit



Sequential logic circuits vs combinational logic circuits:

Sr. No.	Parameter	Combinational circuits	Sequential circuits
1.	Output depend upon	Inputs present at that instant of time.	Present inputs and past inputs/outputs.
2.	Memory	Not necessary	Necessary
3.	Clock input	Not necessary	Necessary
4.	Examples	Adders, subtractors, code convertors	Flip flop, shift registers, counters

Latches and Flip Flops:

- Latches and flip flops are sequential circuit elements , whose output not only depends on the current inputs, but also depends on the previous input and outputs.
- The main difference between the latch and flip flop is that a flip flop has a clock signal, whereas a latch does not.

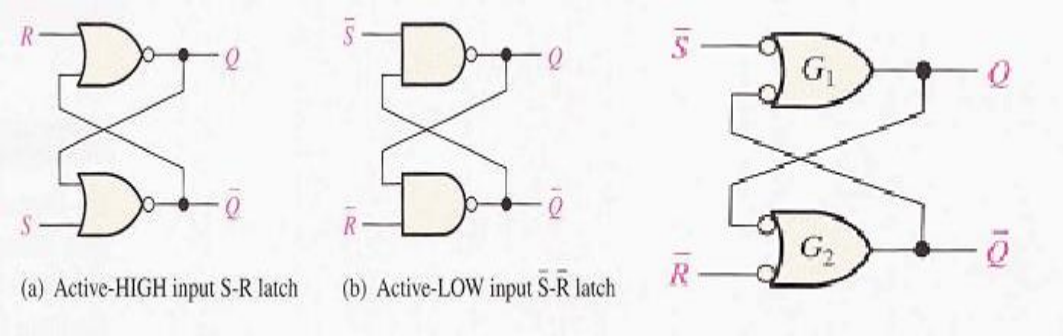
- Basically, there are four types of latches and flip flops: SR, D, JK and T.
- The major differences between these types of flip flops and latches are the number of i/ps they have and how they change the states.

Difference between Latch and Filp-Flop:

Latches	Flip Flops
Latches are building blocks of sequential circuits and these can be built from logic gates	Flip flops are also building blocks oof sequential circuits. But, these can be built from the latches.
Latch continuously checks its inputs and changes its output correspondingly.	Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal
The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on	Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register.
It is based on the enable function input	It works on the basis of clock pulses
It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.	It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.

The S-R Latch: The SR flip-flop, also known as a *SR Latch*, can be considered as one of the most basic sequential logic circuit possible. This simple flip-flop is basically a one-bit memory bistable device that has two inputs, one which will "SET" the device (meaning the output = "1"), and is labelled **S** and one which will "RESET" the device (meaning the output = "0"), labelled **R.**

The SR description stands for "Set-Reset". The reset input resets the flip-flop back to its original state with an output Q that will be either at a logic level "1" or logic "0" depending upon this set/reset condition.



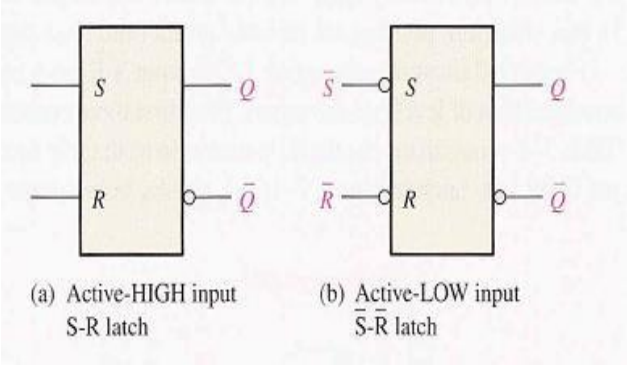
(a) Active-HIGH input S-R latch (b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

Truth table of Active HIGH input SR Latch

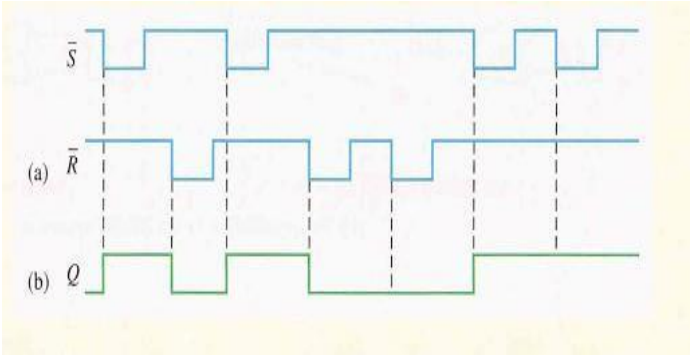
S	R	Q	State
0	0	Previous State	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Forbidden

Truth table of Active LOW input SR Latch

INPUTS $\bar{S}$	INPUTS $\bar{R}$	OUTPUTS Q	OUTPUTS $\bar{Q}$	COMMENTS
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition



(a) Active-HIGH input S-R latch (b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

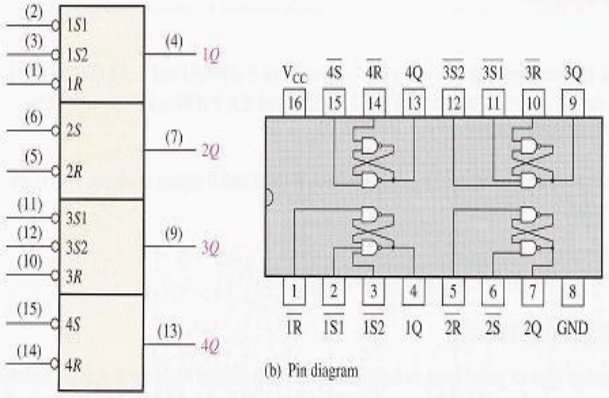


Logic Symbols of S-R Latch:

The 74LS279 SET-RESET LATCH: The 74LS279 is a Quad SR Bistable Latch IC.Each latch has two active low set inputs and an active high output.

THE 74LS279 SET-RESET LATCH

The 74LS279 is a quad $\overline{S}$-$\overline{R}$ latch represented by the logic diagram of Figure 7–7(a) and the pin diagram in part (b). Notice that two of the latches each have two $\overline{S}$ inputs.



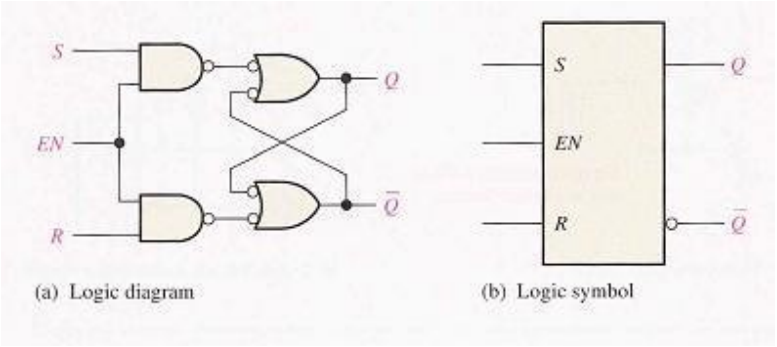
(a) Logic diagram

(b) Pin diagram

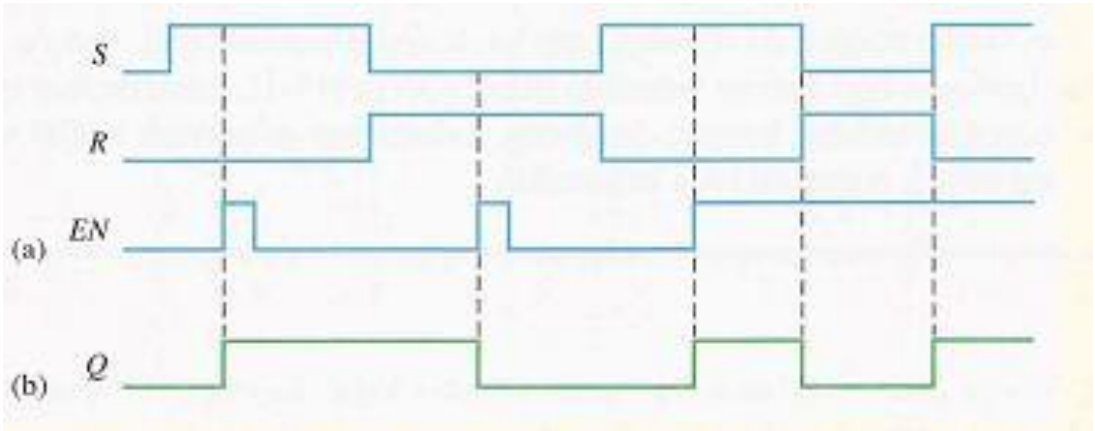
FIGURE 7–7

The 74LS279 quad $\overline{S}$-$\overline{R}$ latch.

The Gated S-R Latch: It is sometimes desirable in sequential logic circuits to have a bistable SR flip-flop that only changes state when certain conditions are met regardless of the condition of either the Set or the Reset inputs. By connecting a 2-input NAND gate in series with each input terminal of the SR Flip-flop a Gated SR Flip-flop can be created. This extra conditional input is called an "Enable" input and is given the prefix of "EN". The addition of this input means that the output at Q only changes state when it is HIGH and can therefore be used as a clock (CLK) input making it level-sensitive as shown.



(a) Logic diagram (b) Logic symbol



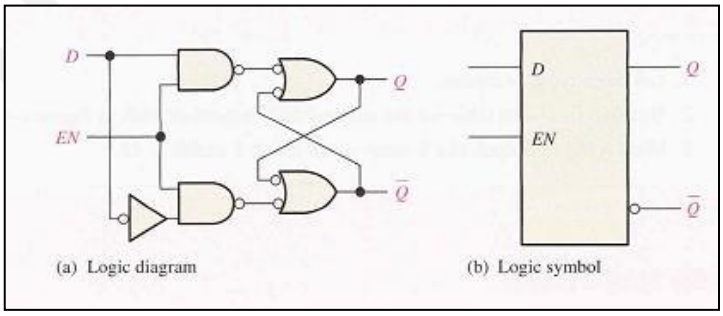
The Gated D Latch : The **D Flip Flop** is by far the most important of the clocked flip-flops as it ensures that ensures that inputs S and R are never equal to one at the same time.

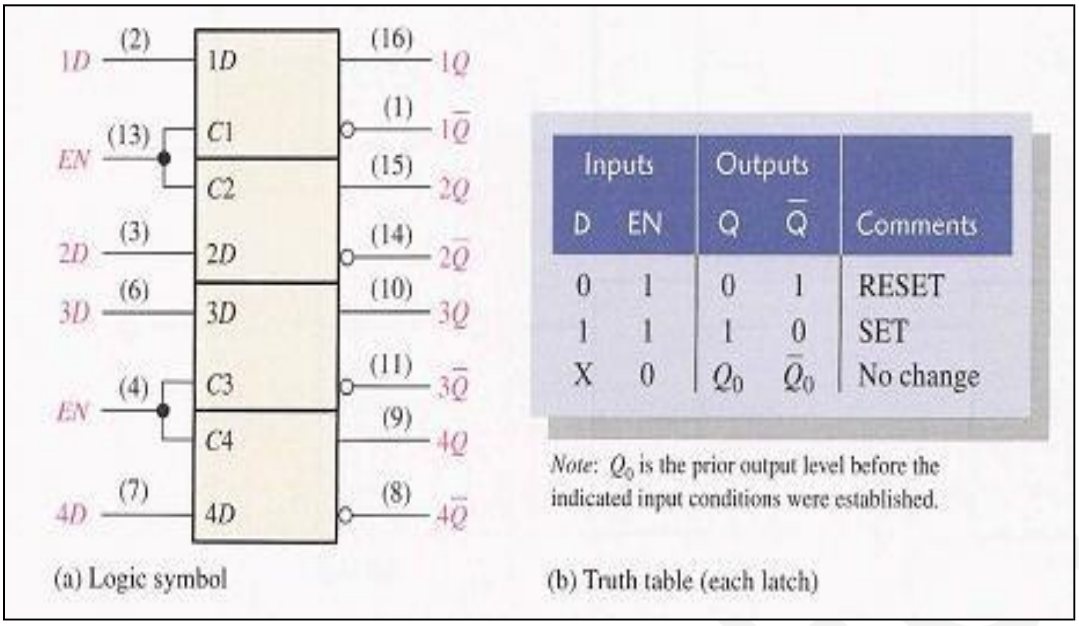
The D-type flip flop are constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (data) input.

Then this single data input, labelled "D" and is used in place of the "Set" signal, and the inverter is used to generate the complementary "Reset" input thereby making a level-sensitive D-type flip-flop from a level-sensitive SR-latch as now S = D and R = not D as shown.

Inputs		Outputs		Comments
E	D	Q_{n+1}	$\overline{Q}_{n+1}$	
1	0	0	1	Rset
1	1	1	0	Set

The 74LS75 Quad Gated D Latch: These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable is HIGH, and the Q output will follow the data input as long as the enable remains HIGH. When the enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go HIGH. These latches feature complementary Q and Q outputs from a 4-bit latch, and are available in 16-pin packages.



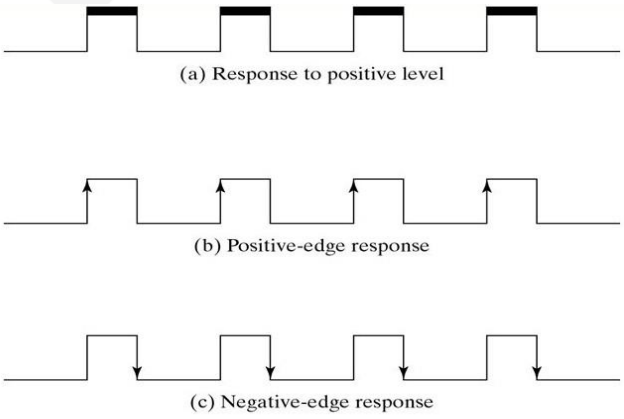


Inputs		Outputs		
D	EN	Q	$\bar{Q}$	Comments
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\bar{Q}_0$	No change

Note: Q_0 is the prior output level before the indicated input conditions were established.

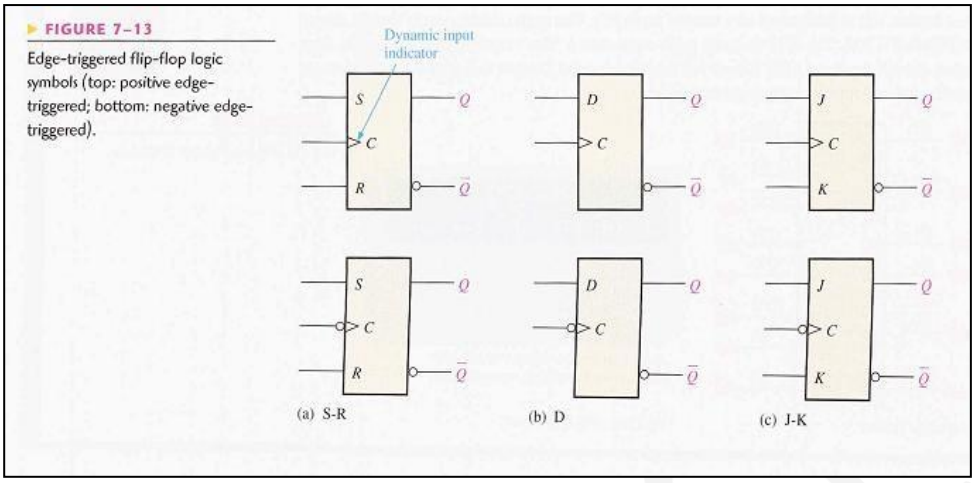
(b) Truth table (each latch)

Edge Triggered Flip-Flops:

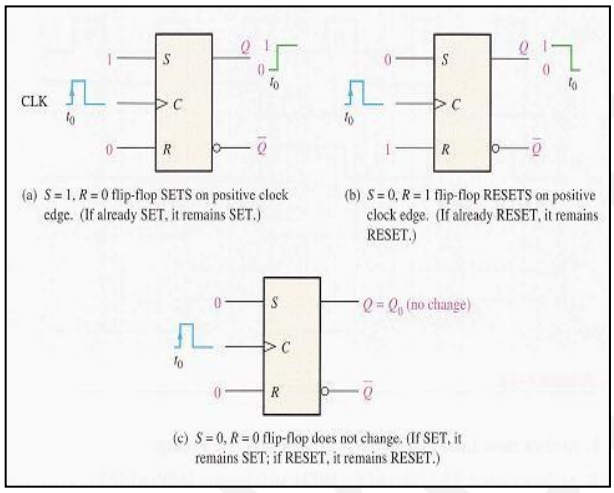


- Flip-flops are synchronous bi-stable devices, also known as bi-stable multivibrators.
- synchronous means the output changes state only at a specified point on the triggering input called the clock (CLK), which is designated as a control input C, ie changes in the output occur in synchronization with the clock
- An edge-triggered Flip-flop changes state either at the positive edge (raising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock.

Logic symbols of Edge Triggered Flip-Flops: Three types of edge-triggered Flip-flops symbols are shown in the figure. Although the S-R flip-flop is not available in IC form, it is the basis for the D and J-K flip-flops. Each type can be either positive edge triggered (no bubble at C input) or negative edge triggered (bubble at C input).The key to identifying an edge triggered flip-flop by it's logic symbol is the small triangle inside the block at the clock (C) input. This triangle is called the dynamic input indicator. The dynamic input indicator, > (Symbol), means the flip-flop changes the state only on the edge of a clock pulse.



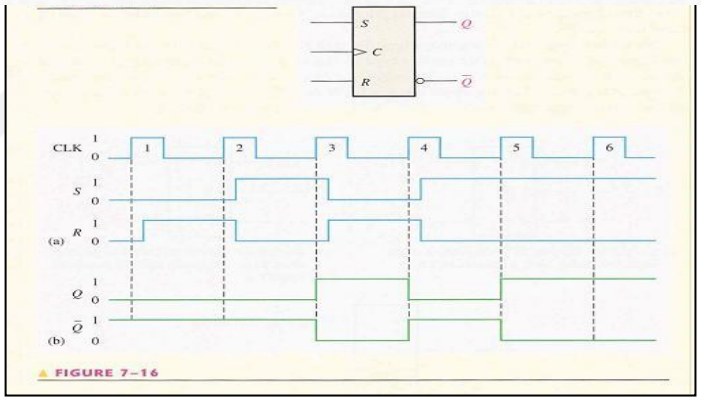
Edge Triggered S-R Flip-Flop :



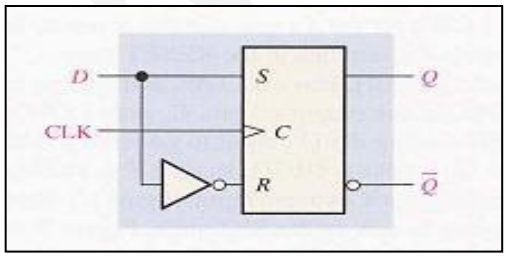
INPUTS S	R	CLK	OUTPUTS Q	$\overline{Q}$	COMMENTS
0	0	X	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

↑ = clock transition LOW to HIGH
X = irrelevant ("don't care")
Q_0 = output level prior to clock transition

The output waveforms of the flip flop in Figure for the S, R, and CLK inputs in the Figure.



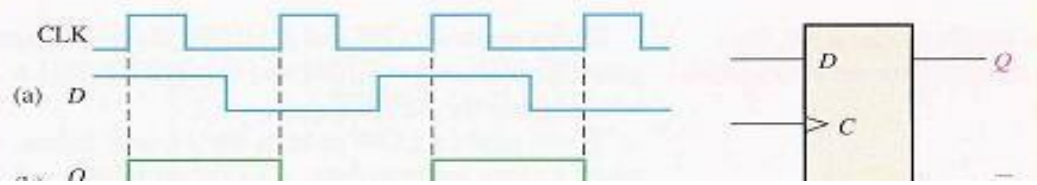
Edge Triggered D Flip-Flop:



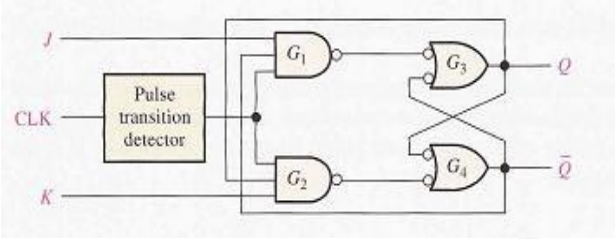
INPUTS D	CLK	OUTPUTS Q	$\overline{Q}$	COMMENTS
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock transition LOW to HIGH

Given the waveforms in Figure 7–21(a) for the *D* input and the clock, determine the *Q* output waveform if the flip-flop starts out RESET.



Edge Triggered J-K Flip-Flop :

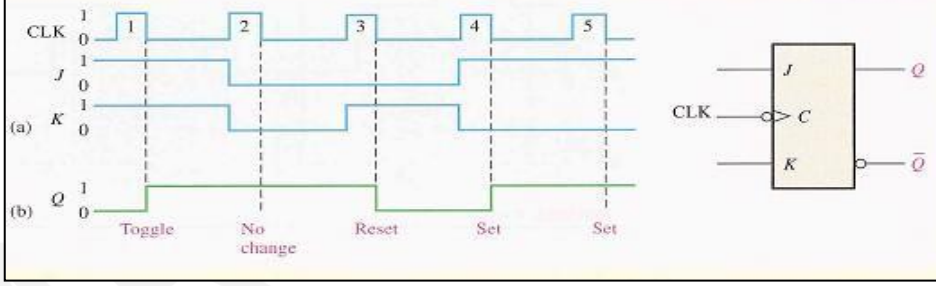


INPUTS J	INPUTS K	INPUTS CLK	OUTPUTS Q	OUTPUTS Q̄	COMMENTS
0	0	↑	Q_0	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle

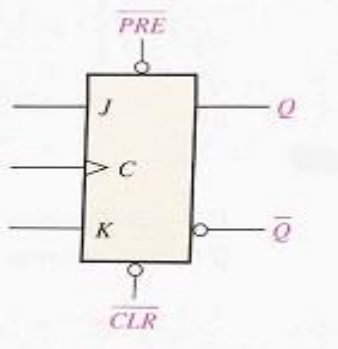
↑ = clock transition LOW to HIGH

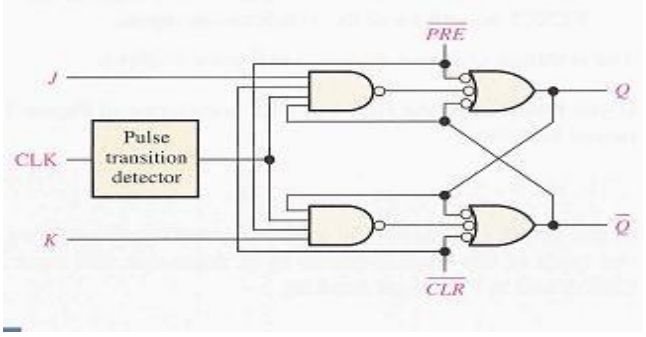
Q_0 = output level prior to clock transition

The waveforms in Figure 7–24(a) are applied to the *J*, *K*, and clock inputs as indicated. Determine the *Q* output, assuming that the flip-flop is initially RESET.

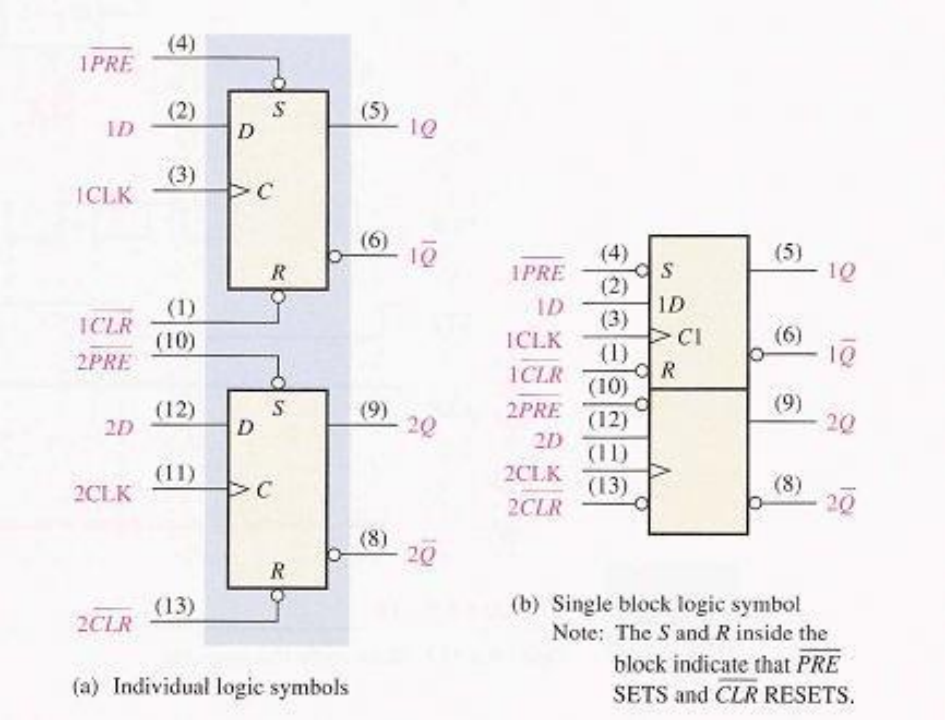


Asynchronous Preset and Clear Inputs: Asynchronous inputs on a flip-flop have control over the **outputs** (Q and not-Q) regardless of clock input status. These inputs are called the preset (**PRE**) and clear (CLR). The preset input drives the flip-flop to a set state while the clear input drives it to a reset state.





74AHC74 Dual D Flip-Flop: The 74AHC74 is a high-speed Si-gate CMOS device is pin compatiblewith Low-Power Schottky TTL (LSTTL). The 74AHC74 is a dual positive-edge triggered, D-type flip-flop with individual data inputs (D), clock inputs (CP), set inputs (SD) and reset inputs (RD). It also has complementary outputs (Q and Q).The set and reset are asynchronous active LOW inputs that operate independent of the clock input. Information on the data input istransferred to the Q output on the LOW to HIGH transition of the clock pulse. The data inputs must be stable one set-up time prior to the LOW to HIGH clock transition for predictable operation



The 74HC112 Dual JK Flip-flop: The 74HC112 is a dual negative-edge triggered JK flip-flop. It features individual J and K inputs, clock (nCP) set (nSD) and reset (nRD) inputs. It also has complementary nQ and nQoutputs. The set and reset are asynchronous active LOW inputs and operate independently of the clock input. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

Conversion of Flip-Flops : The conversion of one **flip flop** to another, a combinational circuit has to be designed first. If a JK Flip Flop is required, the inputs are given to the combinational circuit and the output of the combinational circuit is connected to the inputs of the actual flip flop. Thus, the output of the actual flip flop is the output of the required flip flop. In this post, the following flip flop conversions will be explained.

- **SR Flip Flop to JK Flip Flop**
- **JK Flip Flop to SR Flip Flop**
- **SR Flip Flop to D Flip Flop**
- **D Flip Flop to SR Flip Flop**
- **JK Flip Flop to T Flip Flop**
- **JK Flip Flop to D Flip Flop**
- **D Flip Flop to JK Flip Flop**

The following steps indicate the procedure to be followed to convert a flip-flop into another flip-flop.

Steps:

1. **Identify available and required flip-flops.**
2. **Make characteristics table for the required flip-flop.**
3. **Make excitation table for available flip-flop.**
4. **Write boolean expression for available flip-flop.**
5. **Draw the circuit.**

SR Flip Flop to JK Flip-Flop: J and K will be given as external inputs to S and R. As shown in the logic diagram below, S and R will be the outputs of the combinational circuit.

The truth tables for the flip flop conversion are given below. The present state is represented by Qp and Qp+1 is the next state to be obtained when the J and K inputs are applied.

For two inputs J and K, there will be eight possible combinations. For each combination of J, K and Qp, the corresponding Qp+1 states are found. Qp+1 simply suggests the future values to be obtained by the JK flip flop after the value of Qp. The table is then completed by writing the values of S and R required to get each Qp+1 from the corresponding Qp. That is, the values of S and R that are required to change the state of the flip flop from Qp to Qp+1 are written.

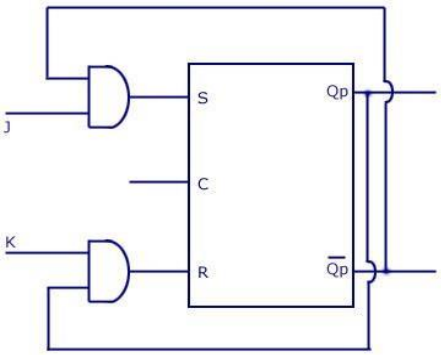
Available flip-flop = SR
Required flip-flop = JK

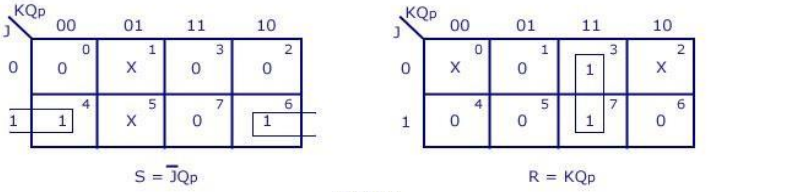
S-R Flip Flop to J-K Flip Flop

Conversion Table

J-K Inputs		Outputs		S-R Inputs	
J	K	Qp	Qp+1	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Logic Diagram





K-Map

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JK Flip Flop to SR Flip Flop: This will be the reverse process of the above explained conversion. S and R will be the external inputs to J and K. As shown in the logic diagram below, J and K will be the outputs of the combinational circuit. Thus, the values of J and K have to be obtained in terms of S, R and Qp. The logic diagram is shown below.

A conversion table is to be written using S, R, Qp, Qp+1, J and K. For two inputs, S and R, eight combinations are made. For each combination, the corresponding Qp+1 outputs are found out. The outputs for the combinations of S=1 and R=1 are not permitted for an SR flip flop. Thus the outputs are considered invalid and the J and K values are taken as “don’t cares”.

Available flip-flop = JK

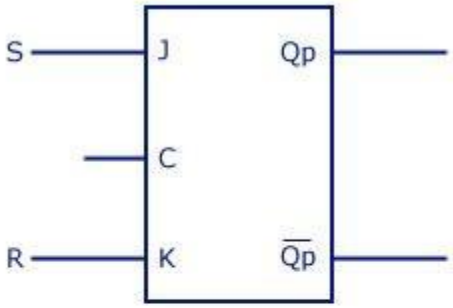
Required flip-flop = SR

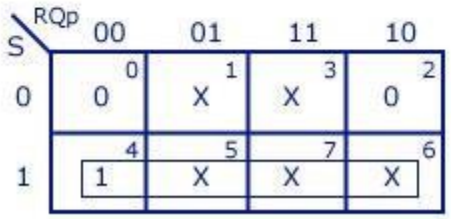
J-K Flip Flop to S-R Flip Flop

Conversion Table

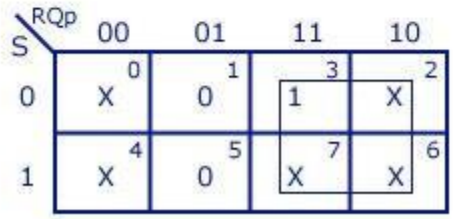
S-R Inputs		Outputs		J-K Inputs	
S	R	Qp	Qp+1	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	Invalid		Dont care	
1	1	Invalid		Dont care	

Logic Diagram





J=S



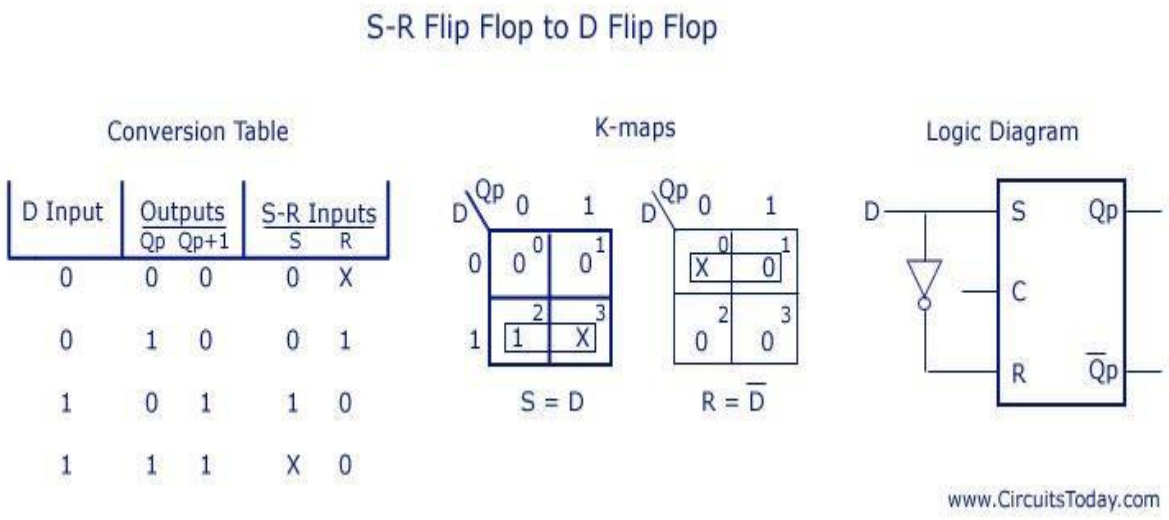
K=R

K-maps

SR Flip Flop to D Flip Flop: S and R are the actual inputs of the flip flop and D is the external input of the flip flop. The four combinations, the logic diagram, conversion table, and the K-map for S and R in terms of D and Qp are shown below.

Available flip-flop = SR

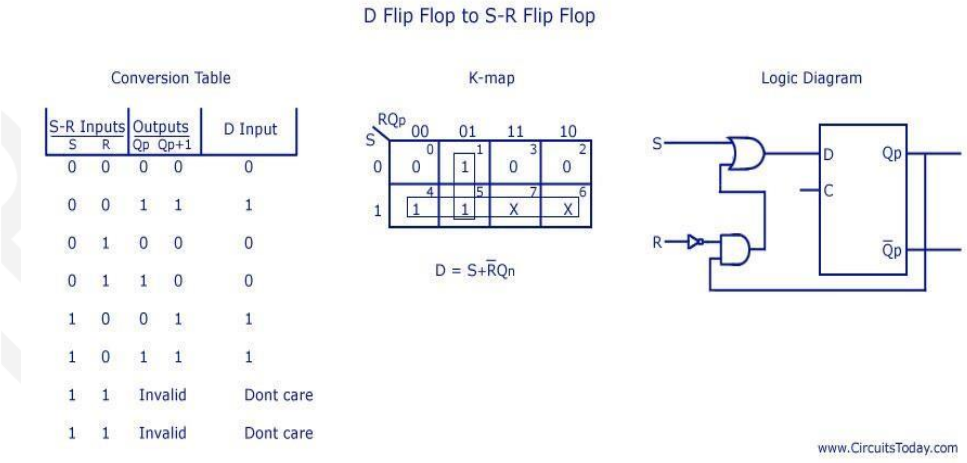
Required flip-flop = D



D Flip Flop to SR Flip Flop: D is the actual input of the flip flop and S and R are the external inputs. Eight possible combinations are achieved from the external inputs S, R and Qp. But, since the combination of S=1 and R=1 are invalid, the values of Qp+1 and D are considered as "don't cares". The logic diagram showing the conversion from D to SR, and the K-map for D in terms of S, R and Qp are shown below.

Available flip-flop = D

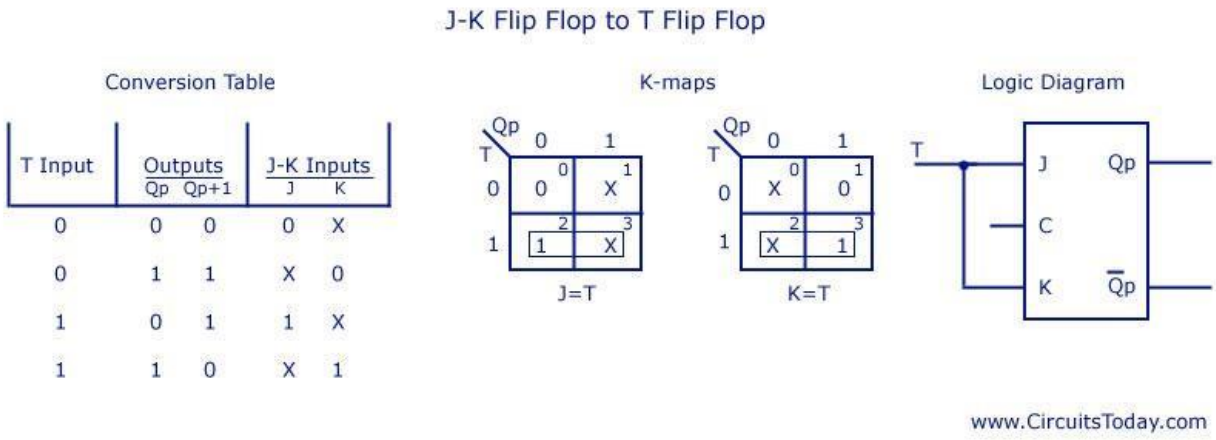
Required flip-flop = SR



JK Flip Flop to T Flip Flop: J and K are the actual inputs of the flip flop and T is taken as the external input for conversion. Four combinations are produced with T and Qp. J and K are expressed in terms of T and Qp. The conversion table, K-maps, and the logic diagram are given below.

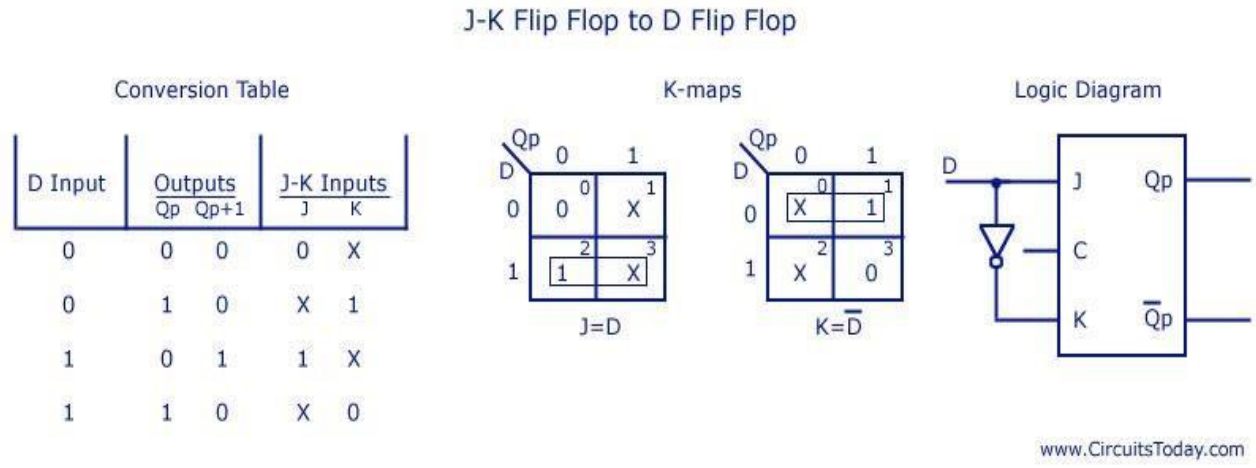
Available flip-flop = JK

Required flip-flop = T



JK Flip Flop to D Flip Flop : D is the external input and J and K are the actual inputs of the flip flop. D and Qp make four combinations. J and K are expressed in terms of D and Qp. The four combination conversion table, the K-maps for J and K in terms of D and Qp, and the logic diagram showing the conversion from JK to D are given below.

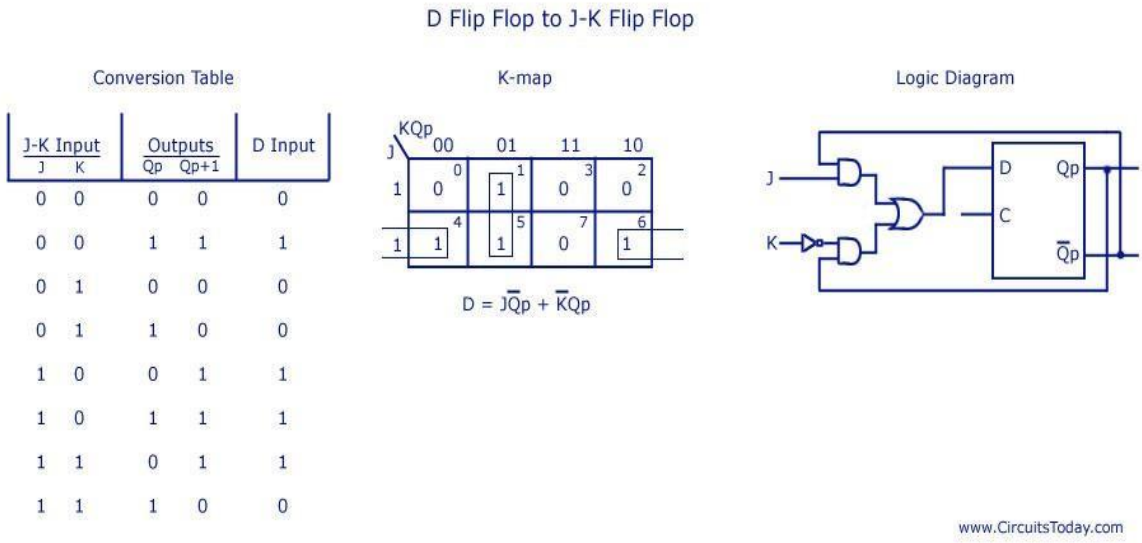
Available flip-flop = JK
Required flip-flop = D



D Flip Flop to JK Flip Flop: D is the actual input to the flip flop and J and K are the external inputs. J, K and Qp make eight possible combinations, as shown in the conversion table below. D is expressed in terms of J, K and Qp.

The conversion table, the K-map for D in terms of J, K and Qp and the logic diagram showing the conversion from D to JK are given in the figure below.

Available flip-flop = D
Required flip-flop = JK



Counters : Counter is a sequential circuit which is used for counting events/operations/pulses.

- Counter is the widest application of flip-flops.
- It is a group of flip-flops with a clock signal applied
- The number of flip-flops used and the way in which they are connected determine the number of states.

Counters are classified into two broad categories according to the way they are clocked;

1. **Asynchronous**
2. **Synchronous.**

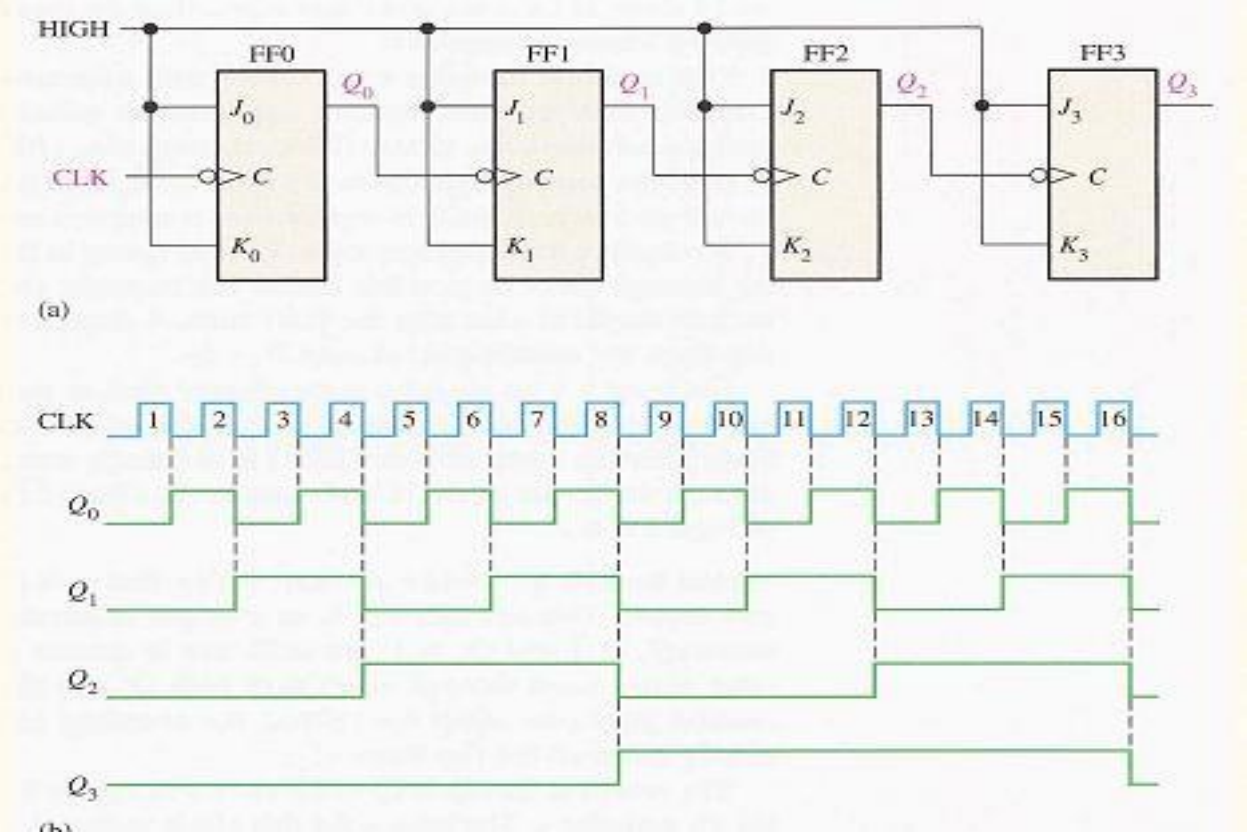
Asynchronous: In asynchronous counters, commonly called ripple counters, the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flip-flop.

- **Don't have fixed time relationship with each other.**
- **Don't occur at the same time.**
- **Don't have a common clock pulse**

Synchronous: In synchronous counters, the clock input is connected to all of the flip-flops so that they are clocked simultaneously.

4-bit Asynchronous Counters: In an asynchronous counter, the clock is applied only to the first stage. Subsequent stages derive the clock from the previous stage.

The 4-bit asynchronous counter shown is typical. It uses J-K flip-flops in the toggle mode



Synchronous Counters: In a synchronous counter all flip-flops are clocked together with a common clock pulse. Synchronous counters overcome the disadvantage of accumulated propagation delays, but generally they require more circuitry to control states changes.

2-Bit Synchronous Counters:

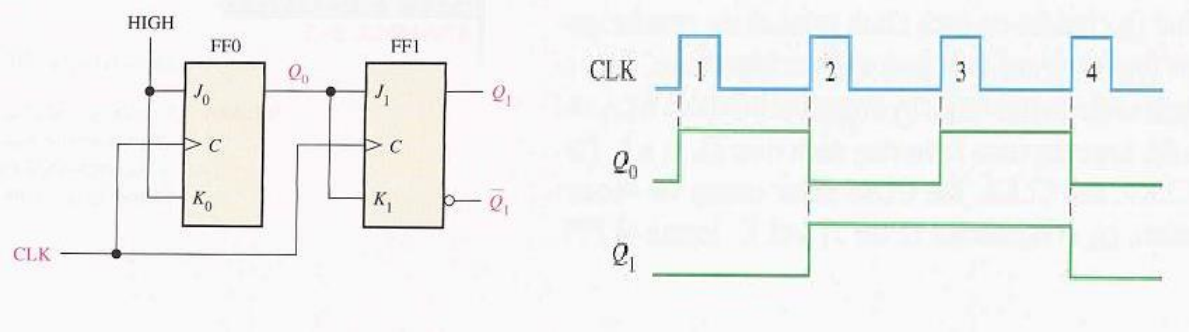
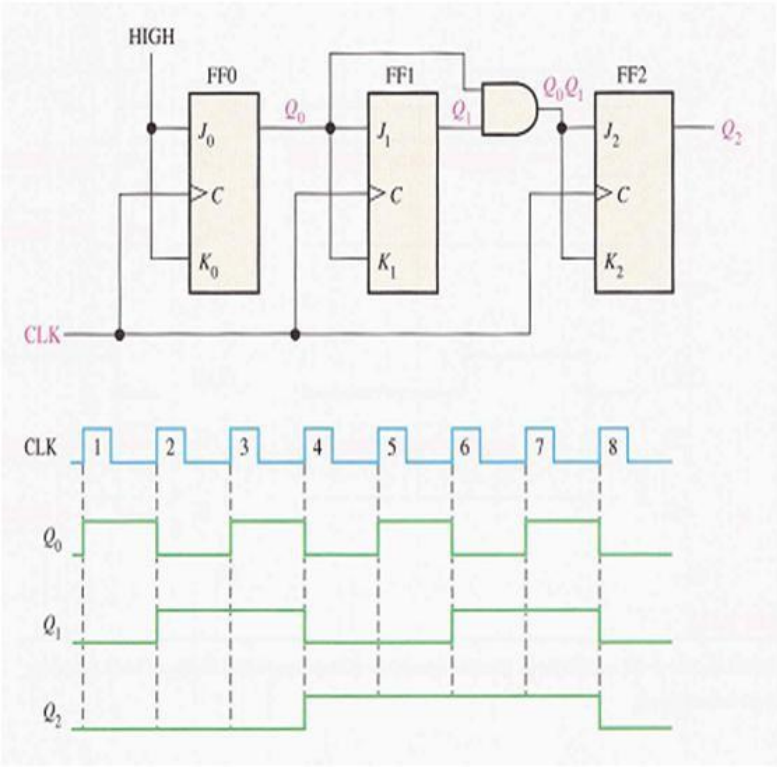


Figure: 2-Bit Synchronous Counters and its Wave form

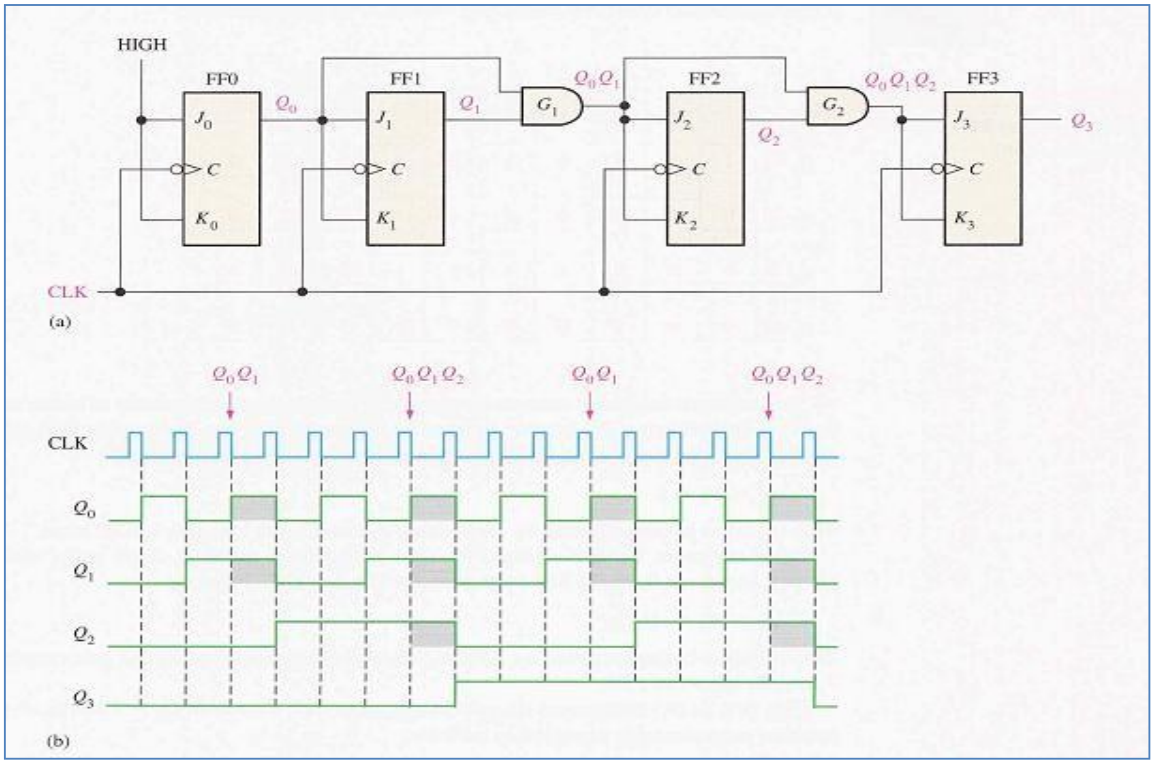
3-Bit Synchronous Binary Counters:



The Binary State Sequence for a 3-bit Binary Counter

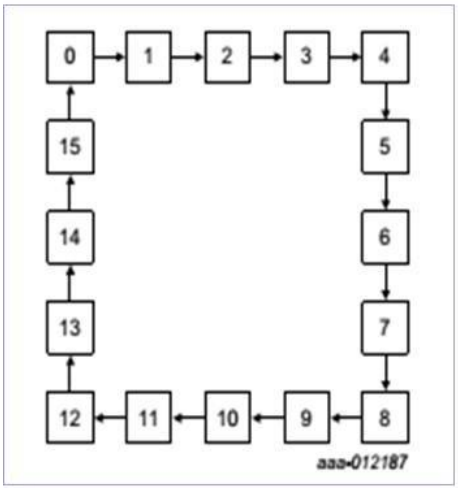
CLOCK PULSE	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

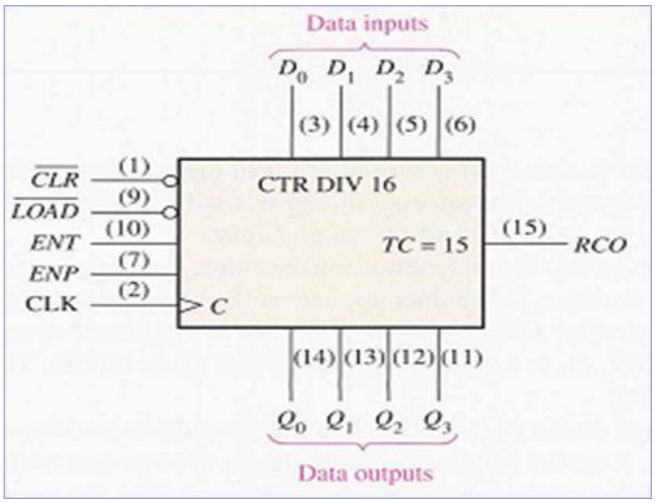
4-Bit Synchronous Binary Counters: This counter is implemented with negative edge-triggred flip-flops. The 4-bit binary counter has one more AND gate than the 3-bit counter. The shaded areas show where the AND gate outputs are HIGH causing the next FF to toggle.

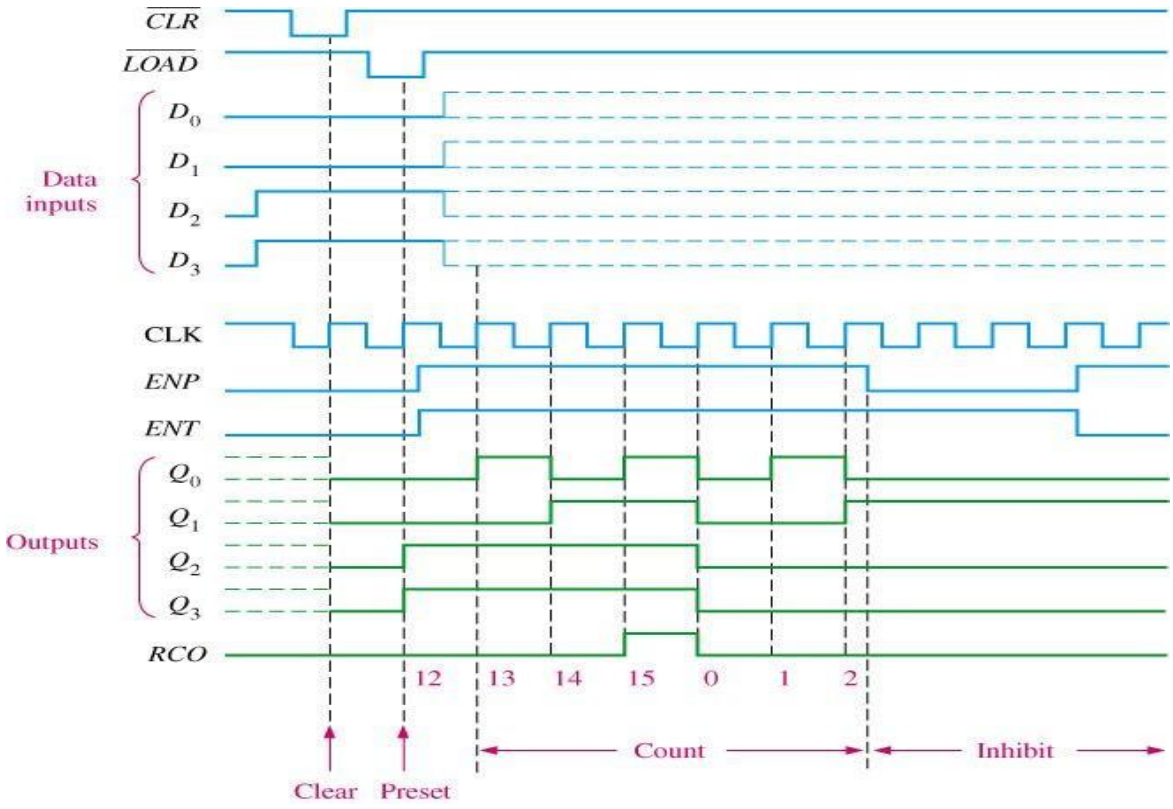


74HC163 4-Bit Synchronous Binary Counters:

- It is a 4-bit IC synchronous counter with additional features over a basic counter.
- It has parallel load, a *CLR* input, two count enables, and a ripple count output that signals when the count has reached the terminal count.
- The counter can synchronously preset to any 4-bit binary number by applying the proper levels to the parallel data inputs.
- When a LOW is applied to the LOAD input, the counter will assume the state of the data inputs on the next clock pulse, the counter sequence can be started with any 4-bit binary number.
- The active-LOW clear input ($\overline{CLR}$) synchronously resets all four flip-flops in the counter.
- The Enable inputs ENP (ENable parallel) and ENT (Enable Trickle) are active-HIGH inputs are used to enable the counter when both are HIGH.
- The ripple clock output(RCO) goes HIGH when the counter reaches the last state in its sequence of fifteen called the terminal count (TC=15)


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
aaa-012187


Data inputs
D_0 D_1 D_2 D_3
(3) (4) (5) (6)
$\overline{CLR}$ (1)
$\overline{LOAD}$ (9)
ENT (10)
ENP (7)
CLK (2)
C
CTR DIV 16
TC = 15
(15)
RCO
(14) (13) (12) (11)
Q_0 Q_1 Q_2 Q_3
Data outputs


$\overline{CLR}$
$\overline{LOAD}$
Data inputs
D_0
D_1
D_2
D_3
CLK
ENP
ENT
Outputs
Q_0
Q_1
Q_2
Q_3
RCO
12 13 14 15 0 1 2
Clear
Preset
Count
Inhibit

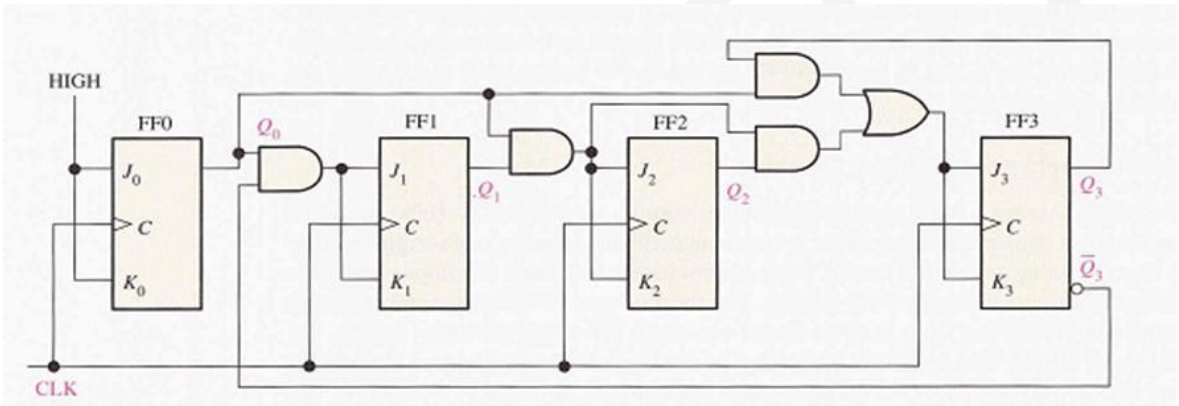
4-Bit Synchronous Decade Counter: The BCD decade counter exhibits a truncated binary sequence and goes from 0000 through the 1001 state. The counter operation can be examined by using states in the truth table.

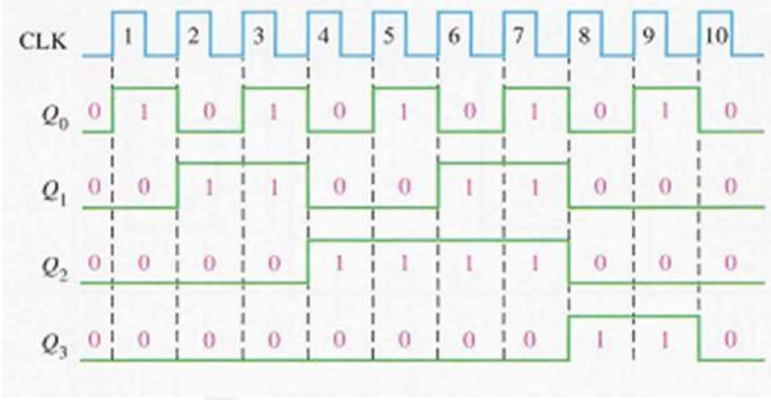
FF0 (Q0) toggles on each CLK pulse. The logic equation is J0=K0=1

FF1 (Q1) changes on the next clock pulse each time when Q0=1 and Q3=0, The logic equation is J1=K1=Q0$\overline{Q3}$

FF2 (Q2) changes on the next clock pulse each time when both Q0=Q1=1, The logic equation is J2=K2=Q0Q1

FF3 (Q3) changes to the opposite state on the next clock pulse each time when Q0=Q1=Q2=1 or Q0=Q3=1 The logic equation is J3=K3=Q0Q1Q2+Q0Q3





CLOCK PULSE	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (recycles)	0	0	0	0

74F162 4-Bit Synchronous Decade Counter: It can preset to any BCD count by the use of the data inputs and low on $\overline{PE}$ input. A LOW on the asynchronous $\overline{SR}$ will reset the counter. The enable inputs CEP (count enable parallel) and CET (count enable trickle) must be both HIGH for the counter to advance through its sequence of states in response to rising edge of

the CLK input. The enable inputs along with terminal count, TC (1001), provide for cascading several decade counters.

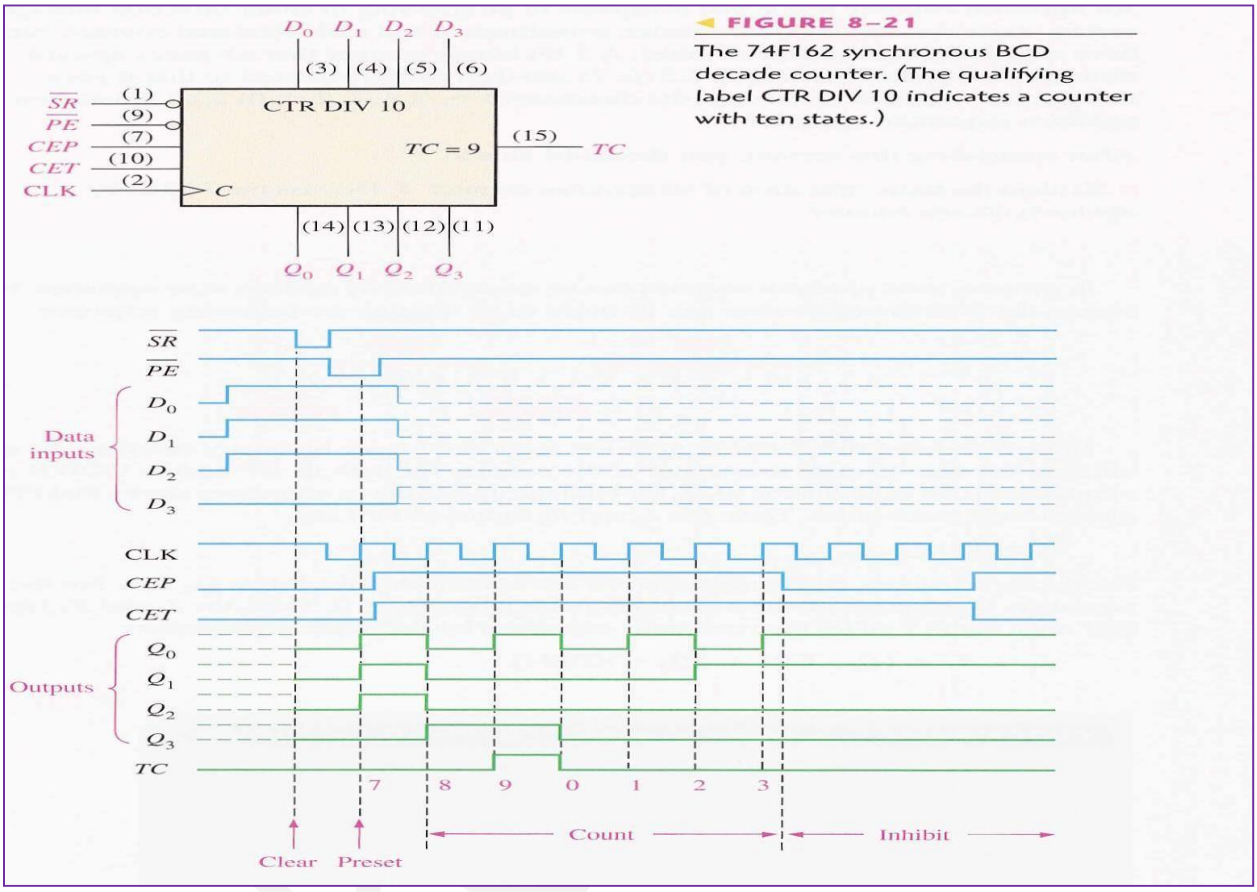


FIGURE 8–21
The 74F162 synchronous BCD decade counter. (The qualifying label CTR DIV 10 indicates a counter with ten states.)

Shift Register:

- A Register can consists of one more flip-flops used to store and shift the data
- Shift Register is sequential device that loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle.
- A shift register is an arrangement of flip-flops with important applications in storage and movement of data.
- A shift register is a digital memory circuit found in calculators, computers, and data-processing systems.
- Bits (binary digits) enter the shift register at one end and emerge from the other end.

Applications of shift registers :

- Computer and Data Communications
- Serial and Parallel Communications
- Multi-bit number storage
- Basic arithmetic such as scaling (a serial shift to the left or right will change the value of a binary number a power of 2)
- Logical operations

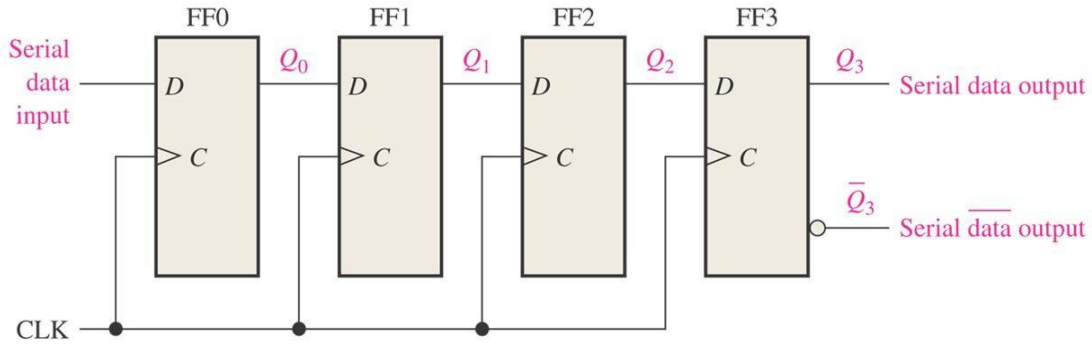
Types of Shift Registers: They are basically classified into four types

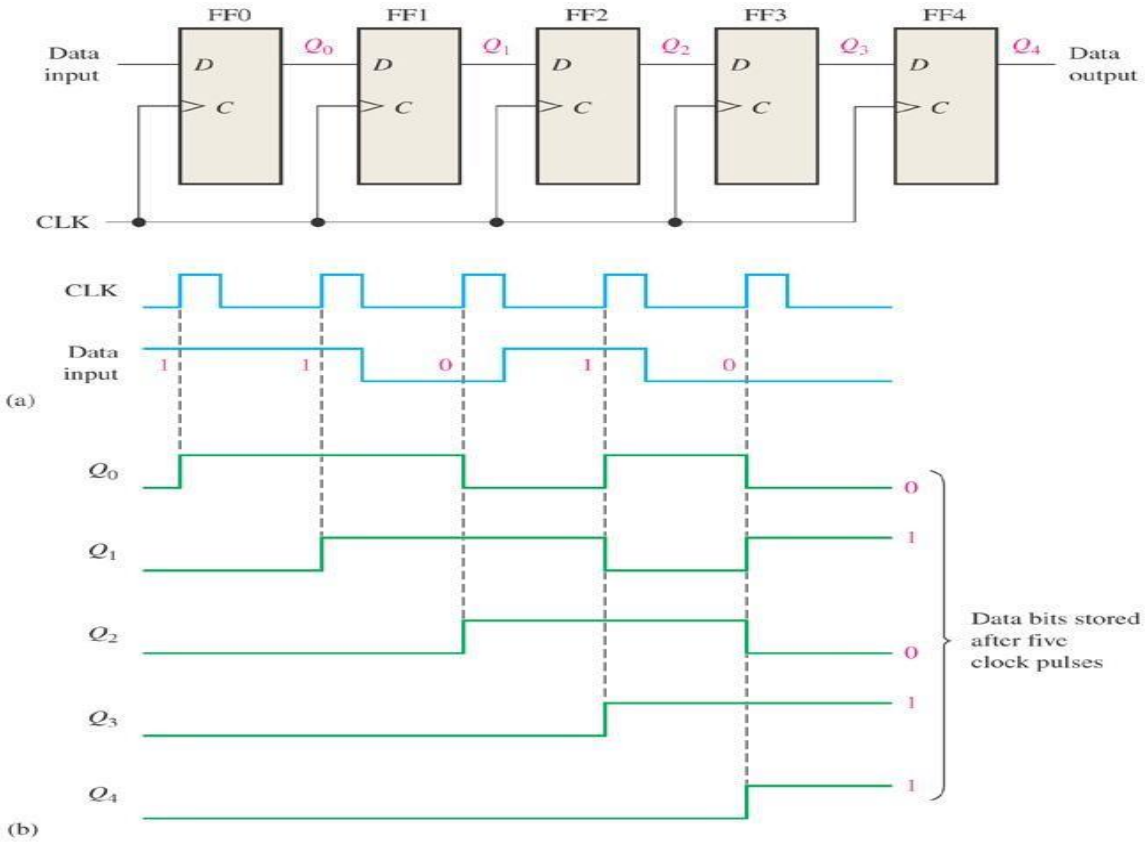
1. **Serial-in to Serial-out (SISO)**
2. **Serial-in to Parallel-out (SIPO)**
3. **Parallel-in to Serial-out (PISO)**.
4. **Parallel-in to Parallel-out (PIPO)**

1. Serial in/serial out shift register (SISO) : The data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control

Shift registers are available in IC form or can be constructed from discrete flip-flops as is shown here with a four-bit serial-in serial-out register.

Each clock pulse will move an input bit to the next flip-flop





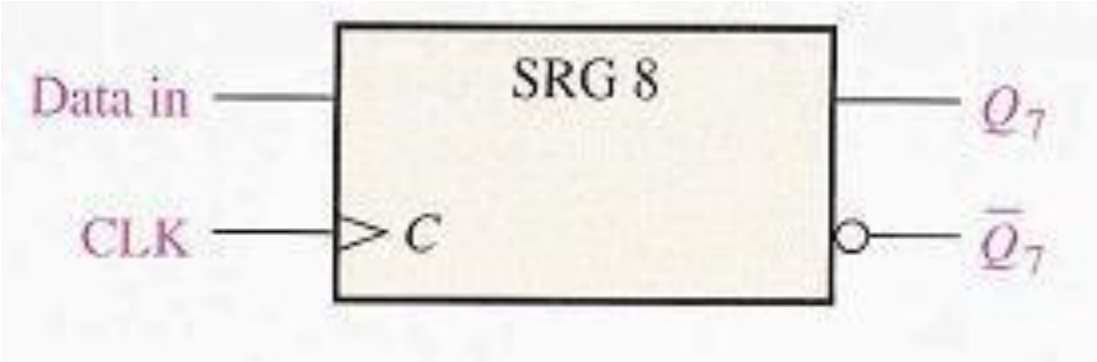
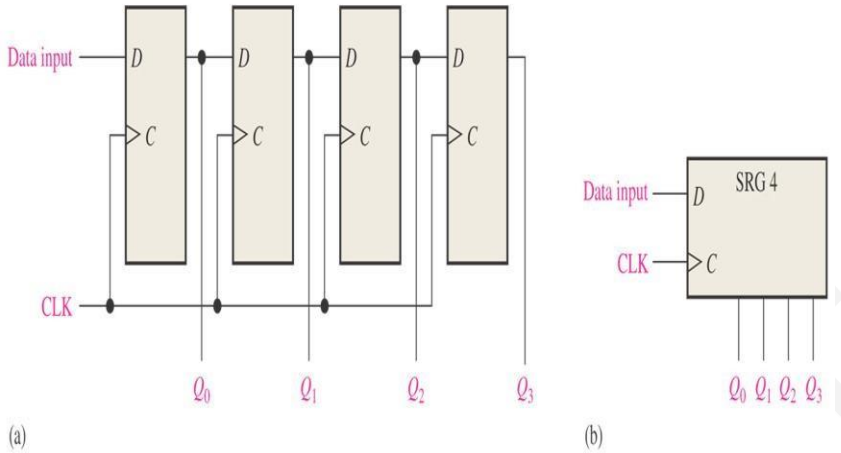


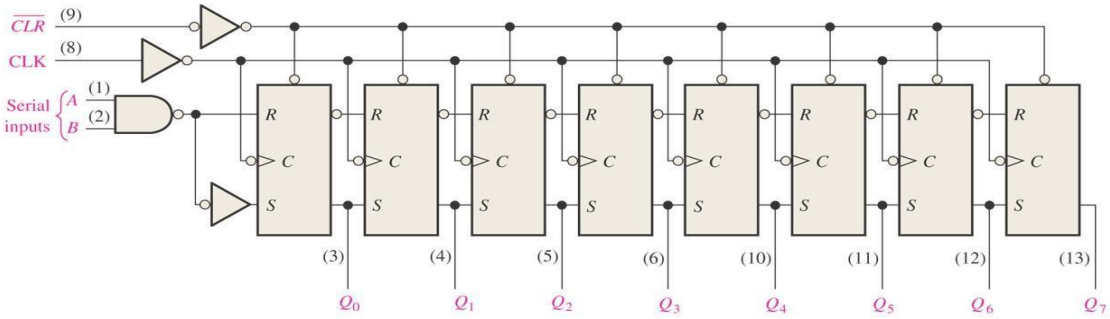
Figure: **Logic symbol.**

2. A serial in/parallel out shift register (SIPO): The register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.

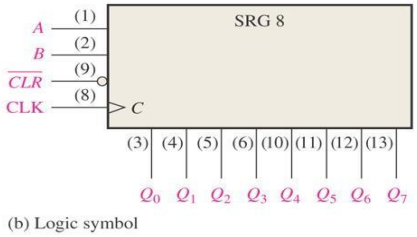


The 74HC164 8-bit serial in/parallel out shift register :

- 8-bit serial in/parallel out shift register
- One of the two serial data inputs may be used as an active HIGH enable to gate the other input.
- If no enable is needed, the other serial input can be connected to *Vcc*.
- The 74HC164A has an active LOW asynchronous clear.
- Data is entered on the leading-edge of the clock.



(a) Logic diagram



(b) Logic symbol

- *B* acts as an active HIGH enable for the data on *A*.

- As with CMOS devices, unused inputs should *always* be connected to a logic level; unused outputs should be left open.

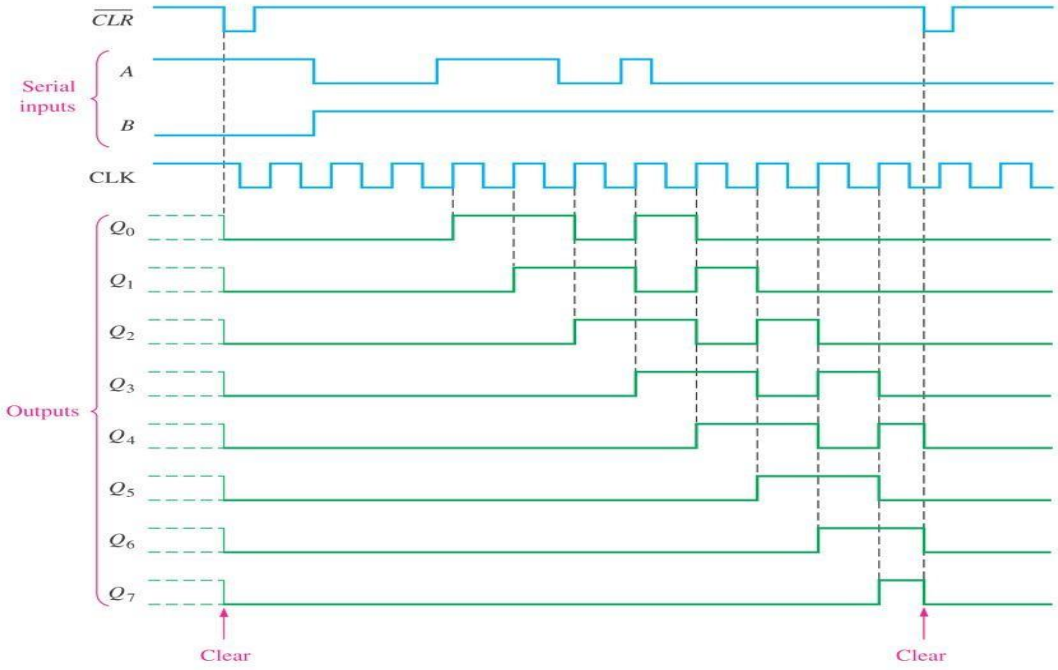
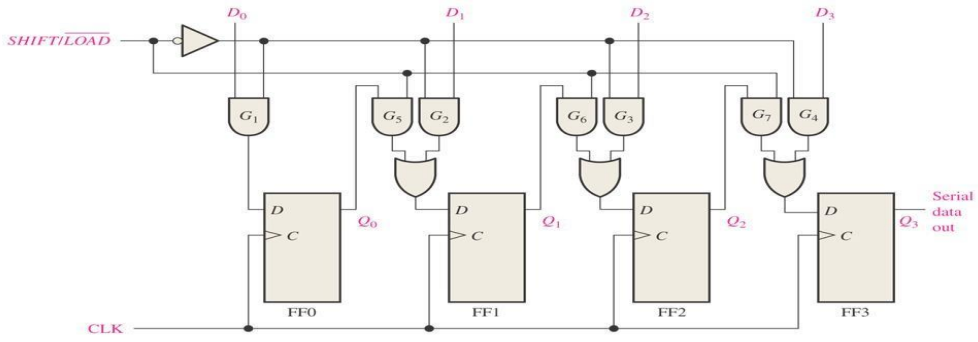


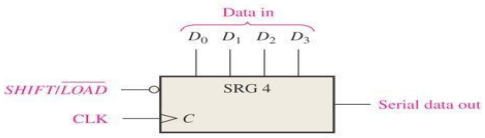
Figure: Timing Diagram

3. Parallel In/Serial Out Shift Registers (PISO) :

- The parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- The data is loaded into the register in a parallel format in which all the data bits enter their inputs simultaneously, to the parallel input pins of the register.
- The data is then read out sequentially in the normal shift-right mode from the register
- This data is outputted one bit at a time on each clock cycle in a serial format.
- It is important to note that with this type of data register a clock pulse is not required to parallel load the register as it is already present, but four clock pulses are required to unload the data.
- Shift registers can be used to convert parallel data to serial form.



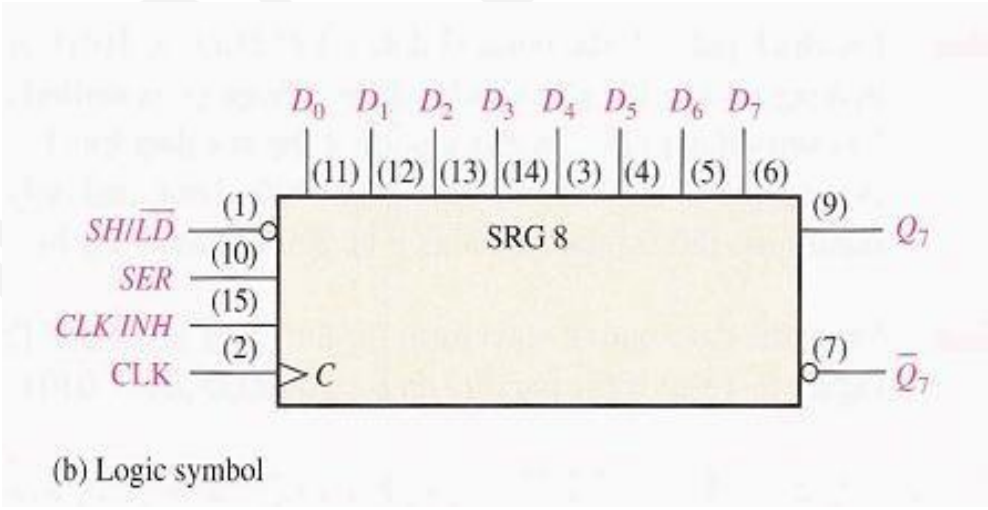
(a) Logic diagram



(b) Logic symbol

74HC165 Shift Register:

- 8-bit parallel in/serial out shift register
- The clock (*CLK*) and clock inhibit (*CLK INH*) lines are connected to a common OR gate, so either of these inputs can be used as an active-LOW clock enable with the other as the clock input.
- Data is loaded *asynchronously* when *SH/$\overline{LD}$* is LOW and moved through the register *synchronously* when *SH/$\overline{LD}$* is HIGH and a rising clock pulse occurs.



(b) Logic symbol

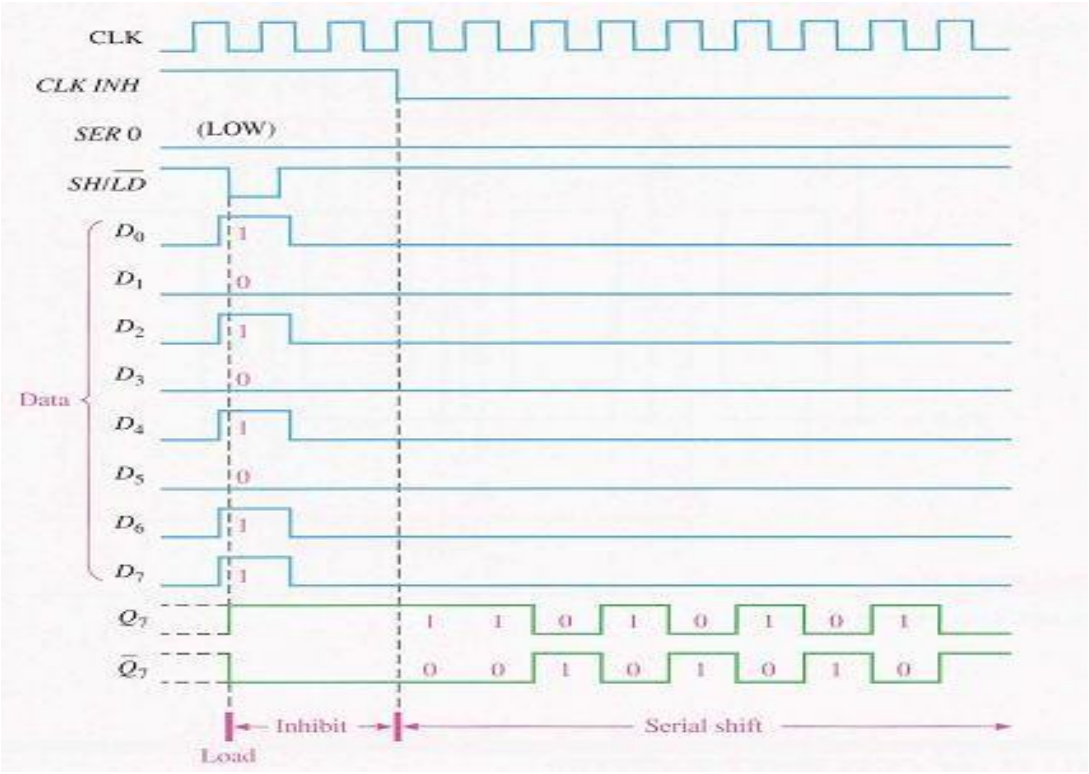
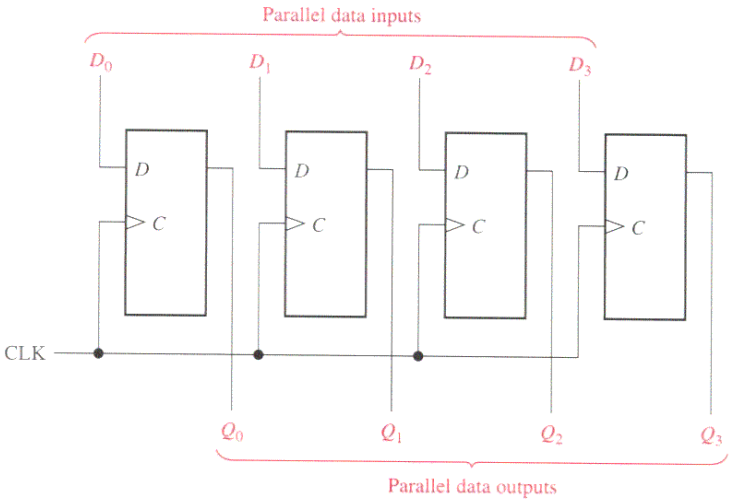


Figure: Timing Diagram

Parallel In/Parallel Out Shift Registers (PIPO): This type of shift register also acts as a temporary storage device or as a time delay device. The data is presented in a parallel format to the parallel input pins and then transferred together directly to their respective output pins by the same clock pulse. Then one clock pulse loads and unloads the register



74HC195 4-bit Parallel in parallel out shift Register: It can be used for parallel in/parallel out, serial in/ serial out and serial in/parallel out operations. It can be used for parallel in/ serial out operation by using Q_3 as the output.

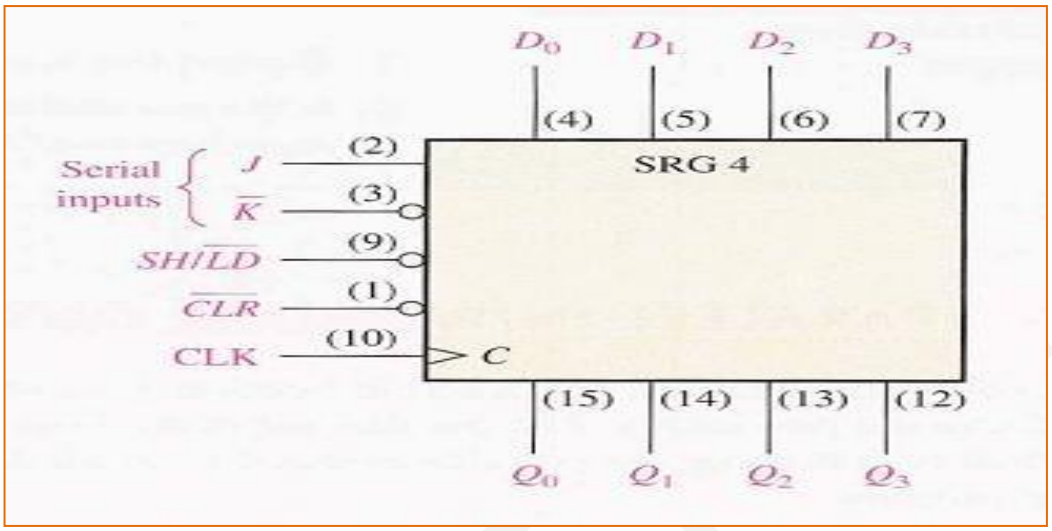


Figure: Logic Symbol

When the SHIFT/$\overline{\text{LOAD}}$ input (SH/$\overline{\text{LD}}$) is LOW, the data on the parallel inputs are entered synchronously on the positive edge of the clock. when SH/$\overline{\text{LD}}$ is HIGH ,the stored data will shift right synchronously with clock .J and K are serial data Inputs to the first stage of the register (Q_0) , Q_3 can be used for serial output data. The active-LOW clear input is asynchronous to clear the register

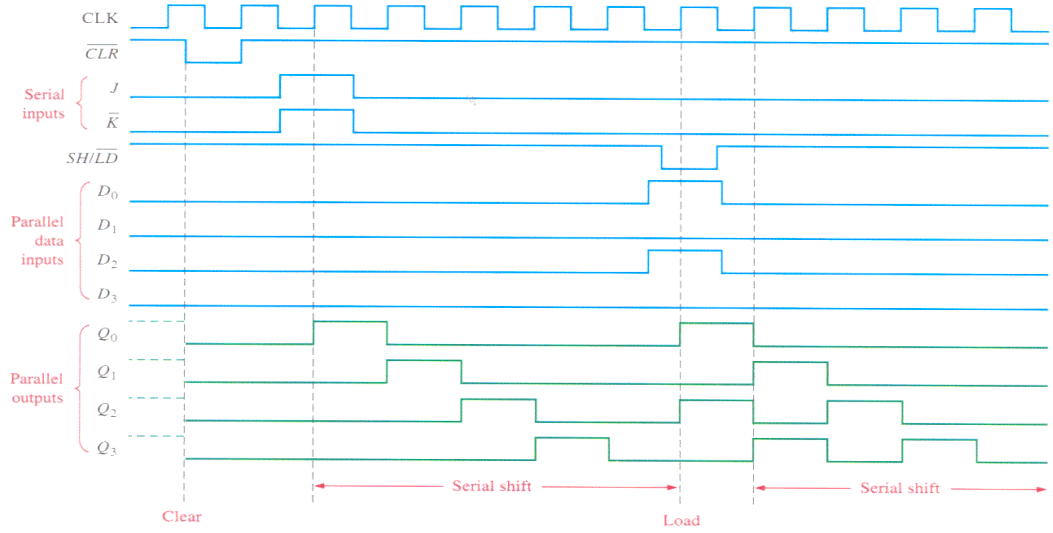


Figure: Timing Diagram