IC APPLICATIONS

LECTURE NOTES

B.TECH (III-EEE I-SEM)

(2018-19)

Prepared by
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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

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MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

III Year B.Tech EEE- I Sem **L T/P/D C**
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(R17A0408) IC APPLICATIONS

COURSE OBJECTIVES:

The main objectives of the course are:

- To introduce the basic building blocks of linear integrated circuits.
- To teach the linear and non-linear applications of operational amplifiers.
- To teach the theory of ADC and DAC.
- To introduce the concepts of waveform generation and introduce some special function ICs.
- To understand and implement the working of basic digital circuits.

UNIT - I

OPERATIONAL AMPLIFIER: Ideal and Practical Op-Amp, Op-Amp Characteristics, DC and AC Characteristics, Features of 741 Op-Amp, Modes of Operation - Inverting, Non-Inverting, Differential, Instrumentation Amplifier, AC Amplifier, Differentiators and Integrators, Comparators, Schmitt Trigger, Introduction to Voltage Regulators, Features of 723 Regulator, Three Terminal Voltage Regulators.

UNIT - II

OP-AMP, IC-555 & IC 565 APPLICATIONS: Introduction to Active Filters, Characteristics of Band pass, Band reject and All Pass Filters, Analysis of 1st order LPF & HPF Butterworth Filters, waveform Generators - Triangular, Sawtooth, Square wave, IC555 Timer - Functional Diagram, Monostable and Astable Operations, Applications, IC565 PLL - Block Schematic, Description of Individual Blocks, Applications.

UNIT - III

DATA CONVERTERS: Introduction, Basic DAC techniques, Different types of DACs-Weighted resistor DAC, R-2R ladder DAC, Inverted R-2R DAC, Different Types of ADCs - Parallel Comparator Type ADC, Counter Type ADC, Successive Approximation ADC and Dual Slope ADC, DAC and ADC Specifications.

UNIT - IV

DIGITAL INTEGRATED CIRCUITS: Classification of Integrated Circuits, Combinational Logic ICs - Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs - Code Converters, Decoders,Encoders,PriorityEncoders,Multiplexers,Demultiplexers,ParityGenerators/Checkers, Parallel Binary Adder/ Subtractor, Magnitude Comparators.

UNIT - V

SEQUENTIAL LOGIC IC'S AND MEMORIES: Familiarity with commonly available 74XX & CMOS 40XX Series ICs - All Types of Flip-flops, conversion of Flip flops, Synchronous Counters, Decade Counters, Shift Registers.

MEMORIES - ROM Architecture, Types of ROMS & Applications, RAM Architecture, Static & Dynamic RAMs.

TEXT BOOKS:

1. Linear Integrated Circuits – D. Roy Chowdhury, New Age International (p) Ltd, 2nd Edition,2003.
2. Op-Amps & Linear ICs - Ramakanth A. Gayakwad, PHI,2003.
3. Digital fundamentals – Floyd and Jain, Pearson Education,8th Edition,2005.

REFERENCE BOOKS:

1. Op Amps & Linear Integrated circuits-Concepts and Applications James M.Fiore, Cengage Learning/Jaico,2009.
2. Operational Amplifiers with linear integrated circuits by K.Lalkishore-Pearson,2009.
3. Linear integrated circuits and applications-Salivahana,TMH.
4. Modern digital electronics-RPJain-4/e-TMH,2010.
5. Digital design principles and practices-John.F.Wakerly3/e,2005.
6. Operational amplifiers with linear integrated cuircuits,4/e William D.Stanley,Pearson educationIndia,2009.

COURSE OUTCOMES:

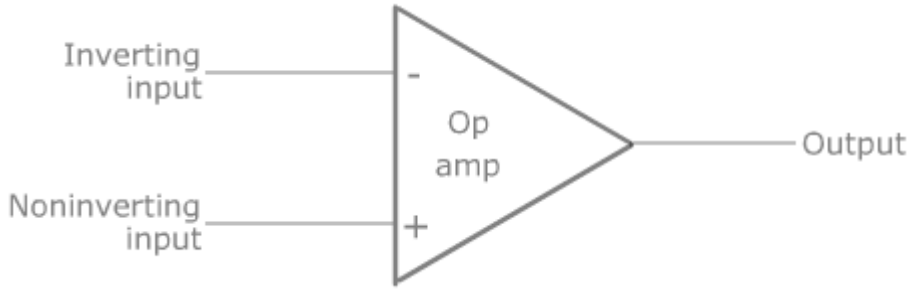
After completion of this course, the students will have:

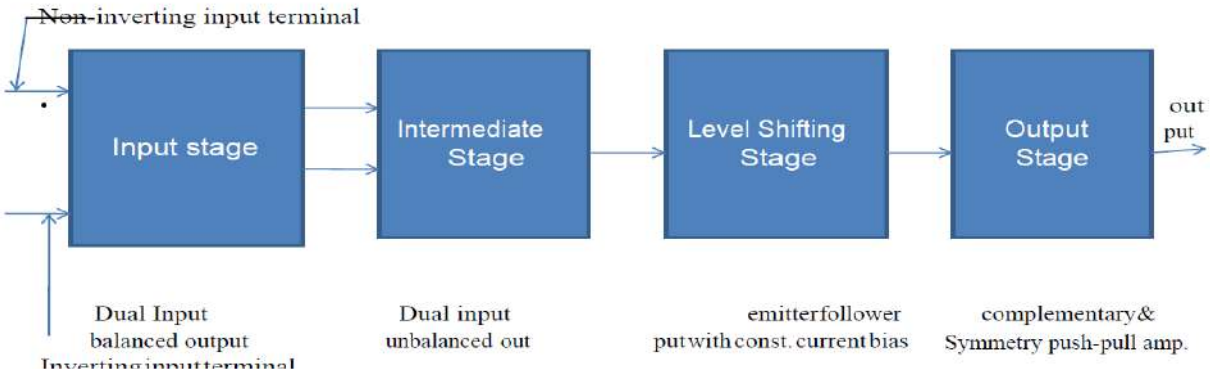
- A thorough understanding of operational amplifiers with linear integrated circuits.
- Understanding of the different families of digital integrated circuits and their characteristics.
- Also students will be able to design circuits using operational amplifiers for various applications.

INDEX

INTRODUCTION:

An operational amplifier is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output stage. An operational amplifier is available as a single integrated circuit package. The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication, and integration. Thus the name operational amplifier stems from its original use for these mathematical operations and is abbreviated to op-amp. With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications, such as ac and dc signal amplification, active filters, oscillators, comparators, regulators, and others.





Ideal and Practical Op Amps:

Ideal Op – Amp is a device which holds the following characteristics.

1. It has infinite voltage gain.

2. It has zero offset voltage. That is, the zero output voltage obtained in Op – Amp even for the zero differential input voltage.

3. It has infinite bandwidth.

4. It has zero output impedance.

5. It has infinite input impedance.

But practically these are not possible due to the imperfections in the manufacturing of practical Op – Amp.

Practical Op – Amp holds the following characteristics.

1. The open loop gain of practical Op – Amp is around 7000.

2. Practical Op – Amp has non zero offset voltage. That is, the zero output is obtained for the non – zero differential input voltage only.

3. The bandwidth of practical Op – Amp is very small value. This can be increased to desired value by applying an adequate negative feedback to the Op – Amp.

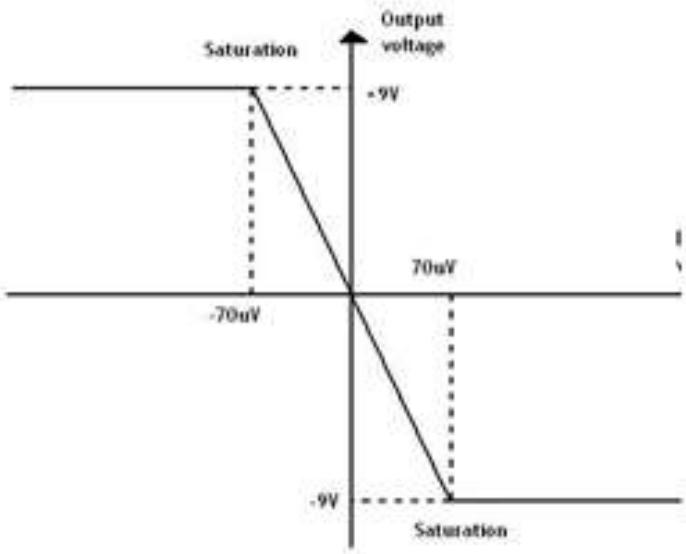
4. The output impedance is in the order of hundreds. This can be minimized by applying an adequate negative feedback to the Op – Amp.

5. The input impedance is in the order of Mega Ohms only. (Whereas the ideal Op – Amp has infinite input impedance).

Input/output characteristics of Practical Opamp:

The maximum output of an opamp is limited by dc power supply voltages supplied to opamp. At most output voltage excursions are limited within +Vcc and –Vcc where Vcc is the power supply voltage. Similarly output currents from the opamp are also limited by these saturation voltages. Below is an example of opamp with gain 1,28,571 and power supply voltages equal to

9volts.When input voltages exceeds +or- 70 micro volts opamp starts to exhibit nonlinear characteristics and output voltage saturates at + or- 9volts.



Differences between Ideal and practical Op-Amps:

Characteristics	Ideal Op-amp	PracticalOp-amp
Voltage gain	Infinite	High
Input resistance	Infinite	High
Output resistance	Zero	Low
Outputvoltagewheninputvoltageis zero	Zero	Low
Band width	Infinite	High
CMRR	Infinite	High
Slew Rate	Infinite	High

DC and AC Characteristics:

DC Characteristics: DC Characteristics include inputbiascurrent,inputoffsetcurrent,Input offset voltage, Output offset voltage and Thermaldrift.

ACCharacteristics:ACcharacteristicsinclude

- Frequency Response
- Slew Rate

Dc characteristics:

An ideal op- amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source into the op-amp inputs. Also the inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non- ideal dc characteristics that add error components to the dc output voltage are:

1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift

1. Input bias current:

It is defined as the average value of the base currents entering into the input terminals of an op-amp during the input bias current.

The op-amp input is a differential amplifier, which may be made of BJT or FET. In either case, the input transistors must be biased into their linear region by supplying

current is drawn from the input terminals. However, practically, input terminals do conduct a small value of dc current to bias the input transistors. The base currents entering into the inverting and non-inverting terminals are shown as IB^ (-) and IB^ (+) respectively. Even though both the transistors are identical, IB^ (-) and IB^ (+) are not exactly equal due to internal imbalances between the two inputs. IB= IB^ (+) + IB^ (-)/ 2 ,Where IB^ (+) – bias current at non- inverting terminal

IB (-) - bias current at inverting terminal

Input bias current compensation:

- IB for BJT is 500mA
- IB for FET is 50pA

By introducing compensation resistor at the non-inverting input terminal we can able to reduce the input bias current.

Rcomp=R1/ Rf= (R1* Rf) / (R1+Rf)

2. Input offset current:

Bias current compensation will work efficiently if both the bias currents IB^ (+) and IB^ (-) are equal. The input transistors cannot be made identical. Hence there will be difference in bias currents. This difference is called as input offset current Ios and can be written as

$$| Ios | = IB^{\wedge} (+) - IB^{\wedge} (-)$$

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.
Input offset current for BJT is 200nA.
Input offset current for FET is 10pA.
The effect of Ios can be minimized by having the feedback resistor value to be small.
3. Input offset voltage:

In spite of the use of the above compensation techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminals to make output voltage zero. This voltage is called input offset voltage Vios. This is the voltage required to be applied at the input for making output voltage to zero volts.

The voltage V_2 at negative terminal is

$$V_2 = R_1.V_0/R_1+R_f$$

Or $V_0 = (R_1 +R_f)V_2/R_1 = (1+ R_f/R_1)V_2$

Since $V_{os} = |V_i - V_2|$ and $V_i = 0$

$V_{os} = |0 - V_2| = V_2$

4. Thermal drift:

Bias current, offset current and offset voltage change with temperature. A circuit carefully mulled at 25 degree Celsius may not remain so when the temperature rises to 35 degree Celsius. This is called drift. Often, offset current drift is expressed in nA/0C and offset voltage drift in mV/0C. These indicate the change in offset for each degree Celsius change in temperature.

There are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be equal be used to keep op-amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.

Ac characteristics:

For small signal sinusoidal applications the a.c. characteristics are
1. Frequency response 2. Slew rate

1. Frequency response:

An ideal op-amp has infinite band width that is open loop gain is 90dB with d.c.signal and this gain should remain the same through audio and radio frequency.

But practically op-amp gain decreases at high frequency. This is due to a capacitive component in the equivalent circuit of op-amp.

Due to R0C, the gain decreases by 20 dB per decay and the frequency is said to be brake or corner frequency and is given by

$$f1 = 1/ (2*3.14*R0*C)$$

$$|A| = A0*L/ (1+ (f/f1) ^2)$$

2. Slew rate:

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μs. for e.g. A 1V/μs slew rate means that the output rises or falls by 1V in one 1μs.

The rate of change of output voltage due to the step input voltage and is usually specified as V/micro sec.

For example: 1V/micro sec. slew rate denotes the output rises or falls by 1 volts in 1 micro seconds.

The rate at which the voltage across the capacitor dVc/dt is given by

$$dVc/dt = I/C$$

Slew rate SR $dVc/dt|_{max} = Imax/C$

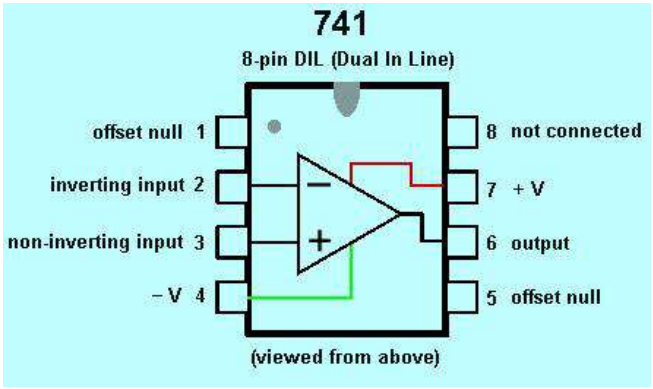
For IC741

Imax= 15 micro amps, C= 30 Pico farad

Slew rate = 0.5V/ micro sec.

Features of 741 Op-Amps:

The pin configuration of the IC 741 operational amplifier is shown below. It comprises of eight pins where the function of each pin is discussed below.



Pin-1 is Offset null.

Pin-2 is Inverting (-) i/p terminal.

Pin-3 is a non-inverting (+) i/p terminal.

Pin-4 is -Ve voltage supply (VCC)

Pin-5 is offset null.

Pin-6 is the o/p voltage.

Pin-7 is +ve voltage supply (+VCC)

Pin-8 is not connected.

- The μA741 is a high performance monolithic operation amplifier constructed using the planar epitaxial process.

The op-amp features are given below

1. High common mode voltage range make the μA741 ideal for use as voltage follower.
2. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.
3. 741 is internally frequency compensated op-amp
4. 741 is available in all 3 packages viz 8-pin metal can, 10-pin flat pack, and 8 or 14 pin DIP.
5. Offset voltage null capability is available.
6. It consumes low power

Modes of Operation - Inverting, Non Inverting amplifier:

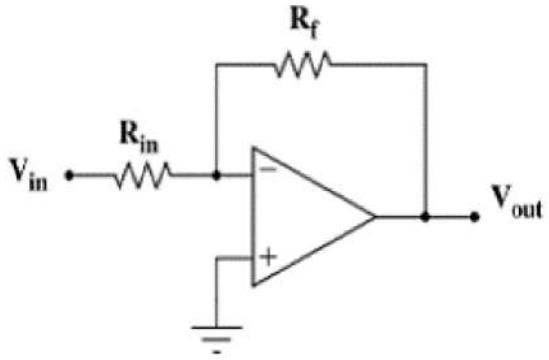
Open loop op-amp configurations:

When connected in open loop mode op-amp simply functions as a high gain amplifier. Three configurations are

1. Differential Amplifier
2. Inverting Amplifier
3. Non inverting Amplifier

Inverting Amplifier:

This is the most widely used of all the op-amp circuits. The output voltage V_0 is feedback to the inverting input terminal through $R_f - R_1$ network where R_f is the feedback resistor. Input signal is applied to the inverting input through R_1 and non-inverting input terminal is grounded.



Analysis:

For simplicity assume an ideal op-amp for analysis. As $V_d = 0$, node'a' is at ground potential an the current i_1 through R_1 is

$$i_1 = V_i / R_1$$

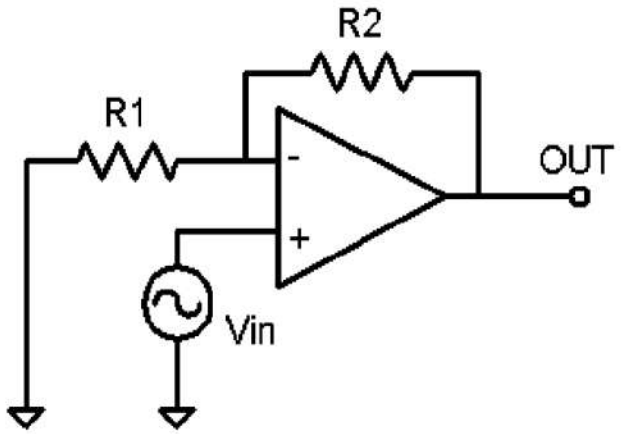
Since op-amp draws no current all the current flowing through R_1 must flow through R_f.
Therefore Output voltage ,

$V_0 = -i_1 R_f = -V_i R_f / R_1$

Gain $A_{CL} = V_0/V_i = -R_f/R_1$

Negative sign indicates a phase shift of 180^0 between V_i and V_0. R_1 should be kept fairly large to avoid loading effect.

Non Inverting Amplifier:



Here the signal is applied to the positive input terminal and feedback is given; the circuit amplifies without inverting the input signal hence it is called non-inverting amplifier.

The voltage at node 'a' is V_i.

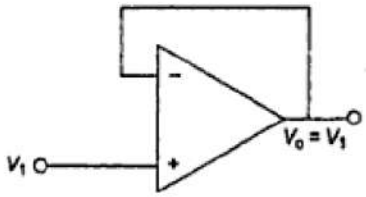
$$V_i = (V_0/R_1+R_f).R_1$$

$$V_0/V_i = (R_i+R_f)/R_1 = 1+R_f/R_1$$

i.e. $A_{CL} = 1+R_f/R_1$

The gain can be adjusted to unity or more by proper seletion of resistors R_f and R_1. Comparin with inverting amplifier the input resistance R_i is extremely large.

Voltage follower:



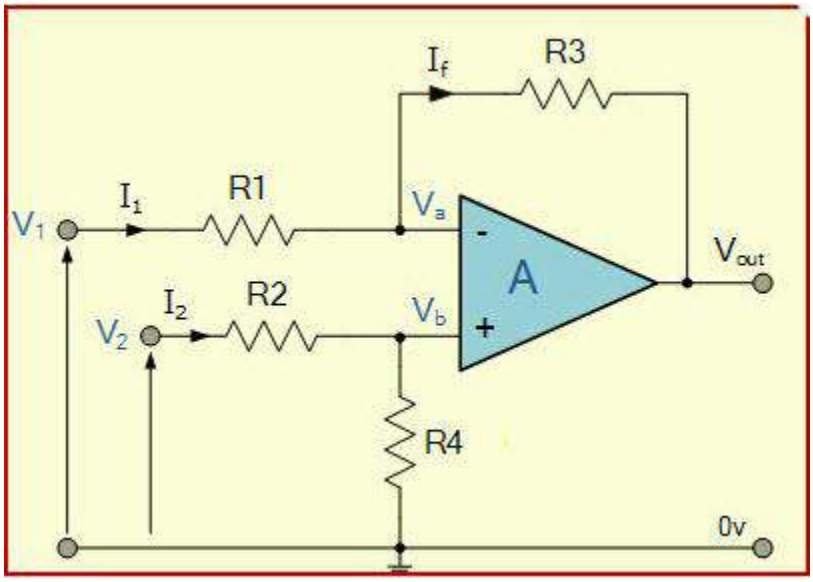
The output voltage follows the input voltage exactly hence the circuit is called a voltage follower. Voltage follower is obtained from the non-inverting amplifier if $R_f = 0$ and $R_1 = \infty$.

$$V_0 = V_i$$

Voltage follower is used as buffer for impedance matching. i.e. to connect a high impedance source to a low impedance load.

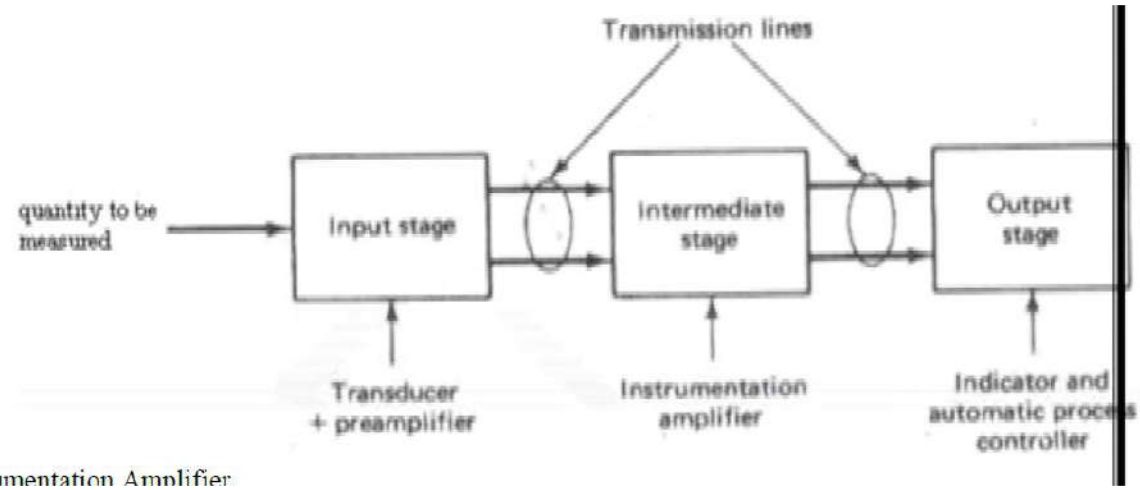
Differential amplifier:

The main function of the differential amplifier is, it amplifies the changes between two i/p voltages. But, conquers any voltage common to the two i/ps. This article gives an overview of differential amplifier along with its mathematical expressions.



Instrumentation Amplifier:

In many industrial and consumer applications the measurement and control of physical conditions are very important.For example measurements of temperature and humidity inside a dairy or meat plant permit the operator to make necessary adjustments to maintain product quality.Similarly,precise temperature control of plastic furnace is needed to produce a particular type of plastic.



2.1 Instrumentation Amplifier

The transducer is a device that converts one form of energy into another. For example a strain gage when subjected to pressure or force undergoes a change in its resistance (electrical energy).An instrumentation system is used to measure the output signal produced by a transducer and often to control the physical signal producing it.

Above fig shows a simplified form of such a system.The input stage is composed of a pre-amplifier and some sort of transducer,depending on the physical quantity to be measured..The output stage may use devices such as meters,oscilloscopes,charts,or magnetic records.

In Figure 2.1 the connecting lines between the blocks represent transmis- sion lines, used especially when the transducer is at a remote test site monitoring hazardous conditions such as high temperatures or liquid levels of flammable chemicals. These transmission lines permit signal transfer from unit to unit. The length of the transmission lines depends primarily on the physical quantities tobe monitored and on system requirements.

The signal source of the instrumentation amplifier is the output of the trans- ducer. Although some transducers produce outputs with sufficient strength to per- m.; their use directly, many do not. To amplify the low-level output signal of the transducer so that it can drive the indicator or display is the major function of the instrumentation amplifier. In short, the instrumentation amplifier is intended for precise, low-level signal amplification where low noise, low thermal and time
drifts, high input resistance, and accurate closed-loop gain are required. Besides, low power consumption, high common-mode rejection ratio, and high slew rate are desirable for superior performance.

There are many instrumentation operational amplifiers, such as the /LA 725, ICL7605, and LH0036, that make a circuit extremely stable and accurate. These
ICs are, however, relatively expensive; they are very precise special-purpose cir- cuits in which most of the electrical parameters, such as offsets, drifts, and power consumption, are minimized, whereas input resistance, CMRR, and supply range are optimized. Some instrumentation amplifiers are even available in modular form to suit special installation requirements.

Obviously, the requirements for instrumentation op-amps are more rigid than those for general-purpose applications. However, where the requirements are not too strict, the general-purpose op-amp can be employed in the differential mode.
We will call such amplifiers differential instrumentation amplifiers. Since most instrumentation systems use a transducer in a bridge circuit, we will consider a simplified differential instrumentation system arrangement using a transducer bridge circuit.

AC Amplifier:

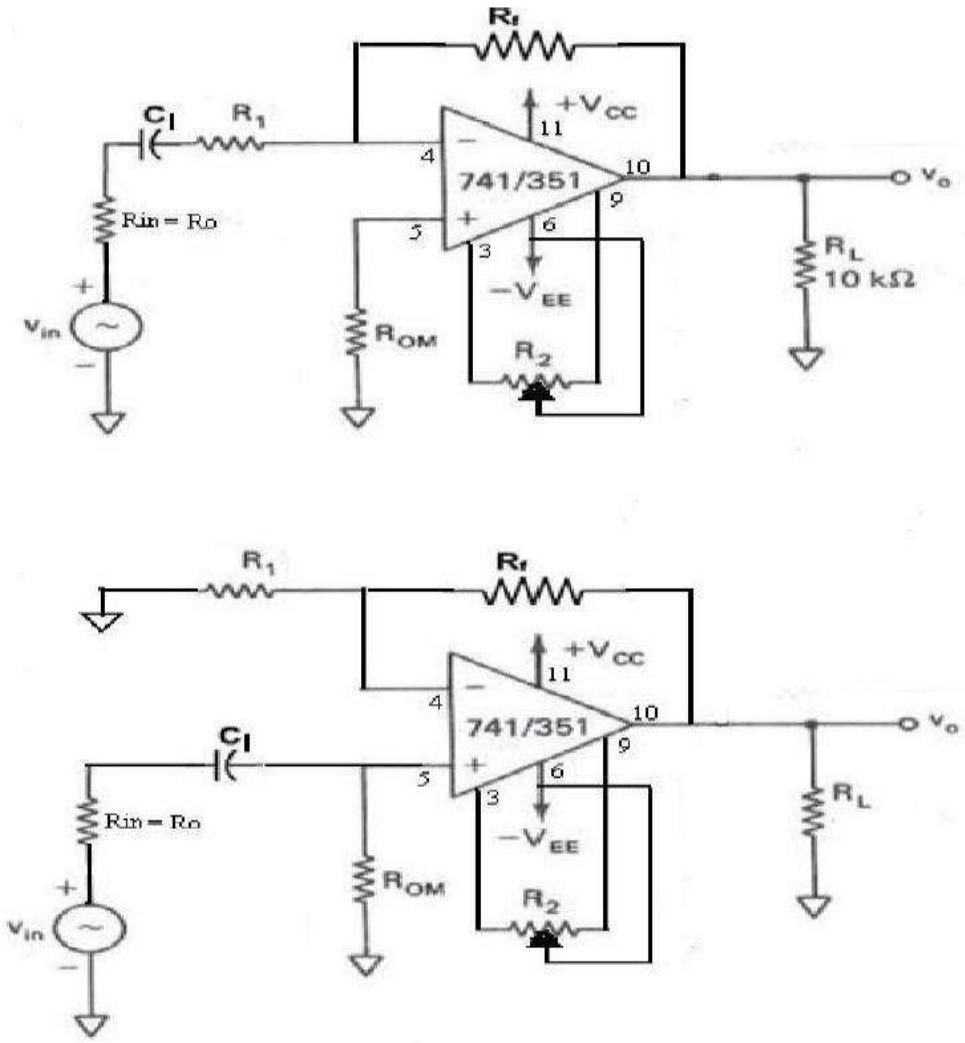


Fig 2.2.1(a) AC Inverting Amplifier (b)AC Non Inverting Amplifier

IfanACinputisridingonsomeDClevel,itisnecessary touseanACamplifierwithacouplingcapacitorto blockthe DCamplification.

Forexample,inanaudioreceiversystemthatconsists of a number of stages, because of thermal drift, componenttolerances,andvariationstheDClevelis produced.

TopreventtheamplificationofsuchDClevels,the couplingcapacitorsmustbeusedbetweenthestages.

Thefigure7-3showstheACinvertingandnon- invertingamplifierswithcouplingcapacitors.

Diffrentiator:

A circuit in which the output voltage waveform is the differentiation of input voltage is called differentiator as shown infig.2.10.

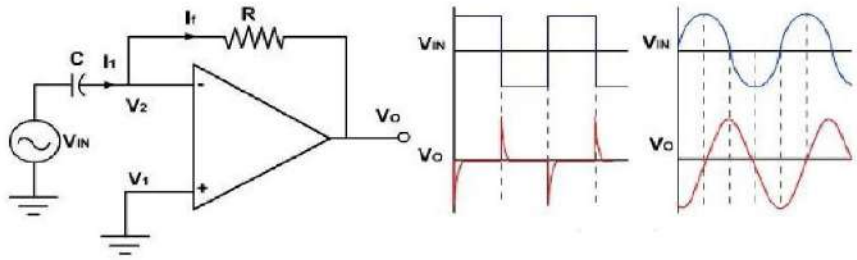


Fig.2.10 Circuit Diagram of Differentiator

The expression for the output voltage can be obtained from the Kirchoff's current equation written at node v_2.

$$\text{Since,} \quad i_{in} = i_f$$

$$\text{Therefore,} \quad C\frac{d}{dt}(V_{in}-0)=\frac{0-V_o}{R}$$

$$V_o = -RC\frac{dV_{in}}{dt}$$

Thus

the output v_o is equal to the RC times the negative instantaneous rate of change of the input voltage v_{in} with time. A cosi

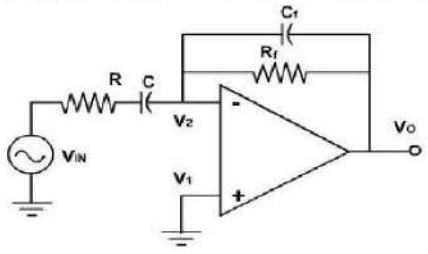


Fig.2.11 Circuit Diagram of Differentiator produces sine output. fig.2.10 also shows the output waveform for different input

The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to $R_f C$.

As the frequency changes, the gain changes. Also at higher frequencies the circuit is highly susceptible at high frequency noise and noise gets amplified. Both the high frequency noise and problem can be corrected by adding, few components. as shown in fig.2.11.

Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is called integrator. Fig.2.12, shows an integrator circuit using OPAMP.

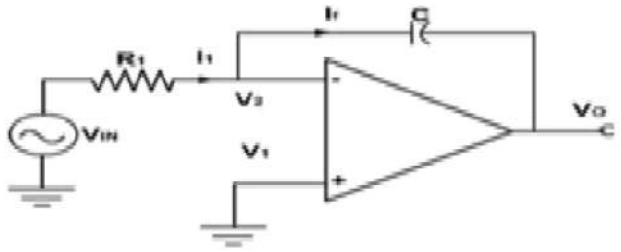


Fig.2.12 Circuit Diagram of Integrator

Here, the feedback element is a capacitor. The current drawn by OPAMP is zero and also the V_2 is virtually grounded.

Therefore, $i_1 = i_f$ and $v_2 = v_1 = 0$

$$\frac{v_{in} - 0}{R} = C \frac{d(0 - v_o)}{dt}$$

Integrating both sides with respect to time from 0 to t, we get

$$\int_0^t \frac{v_{in}}{R} dt = \int_0^t C \frac{d(-v_o)}{dt} dt$$

$$= C(-v_o) + v_o|_{t=0}$$

$$\text{if } V_o|_{t=0} = 0 \text{ V, then}$$

$$v_o = \frac{-1}{R} \int_0^t v_{in} \, dt$$

The output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant RC.

If the input is a sine wave the output will be cosine wave. If the input is a square wave, the output will be a triangular wave. For accurate integration, the time period of the input signal T must be longer than or equal to RC.

Fig.2.13, shows the output of integrator for square and sinusoidal inputs.

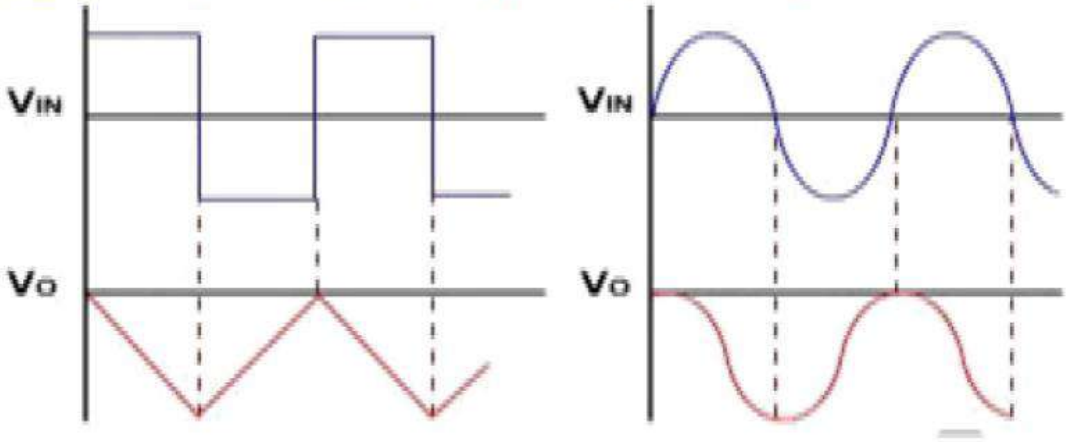


Fig.2.13 Input and Out put wave forms

Comparators:

Voltage comparator circuit.

Voltage comparator is a circuit which compares two voltages and switches the output to either high or low s depending upon which voltage is higher. A voltage comparator based on opamp is shown here. Fig2.14 shov voltage comparator in inverting mode and Fig shows a voltage comparator in non inverting mode.

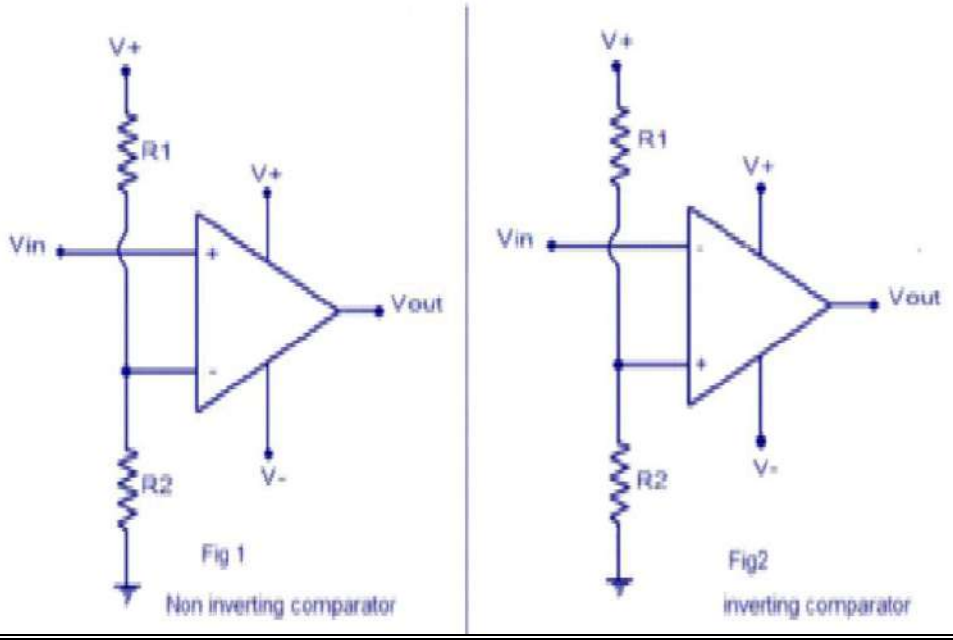


Fig 1
Non inverting comparator

Fig2
inverting comparator

2.8.1.Non inverting comparator.

In non inverting comparator the reference voltage is applied to the inverting input and the voltage to be compared is applied to the non inverting input. Whenever the voltage to be compared (Vin) goes above the reference voltage , the output of the opamp swings to positive saturation (V+) and vice versa. Actually what happens is that, the difference between Vin and Vref, (Vin – Vref) will be a positive value and is amplified to infinity by the opamp. Since there is no feedback resistor Rf, the opamp is in open loop mode and so the voltage gain (Av) will be close to infinity. So the output voltage swings to the maximum possible value ie; V+. Remember the equation Av = 1 + (Rf/R1). When the Vin goes below Vref, the reverse occurs.

2.8.2.Inverting comparator.

In the case of an inverting comparator, the reference voltage is applied to the non inverting input and voltage to be compared is applied to the inverting input. Whenever the input voltage (Vin) goes above the Vref, the output of the opamp swings to negative saturation. Here the difference between two voltages (Vin-Vref) is inverted and amplified to infinity by the opamp. Remember the equation Av = -Rf/R1. The equation for voltage gain in the inverting mode is Av = -Rf/R1.Since there is no feedback resistor, the gain will be close to infinity and the output voltage will be as negative as possible ie; V-.

2.8.3.Practical voltage comparator circuit.

A practical non inverting comparator based on uA741 opamp is shown below. Here the reference voltage is set using the voltage divider network comprising of R1 and R2. The equation is Vref = (V+/ (R1 + R2)) x R2. Substituting the values given in the circuit diagram into this equation gives Vref = 6V. Whenever Vin goes above 6V, the output swings to ~+12V DC and vice versa. The circuit is powered from a +/- 12V DC dual supply.

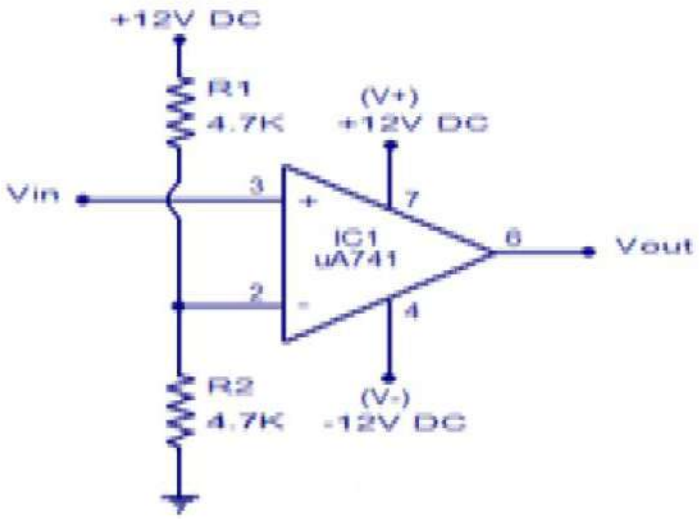
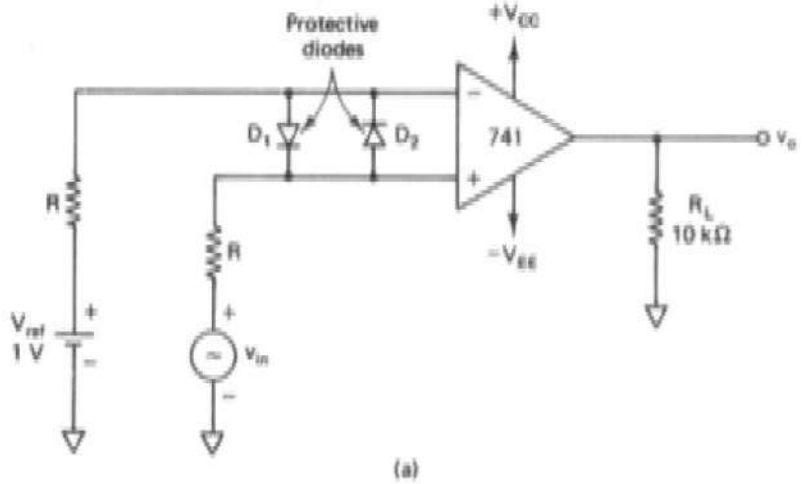


Fig2.15 Circuit diagram of Practical voltage comparator.

2.8.4.Op-amp voltage comparator



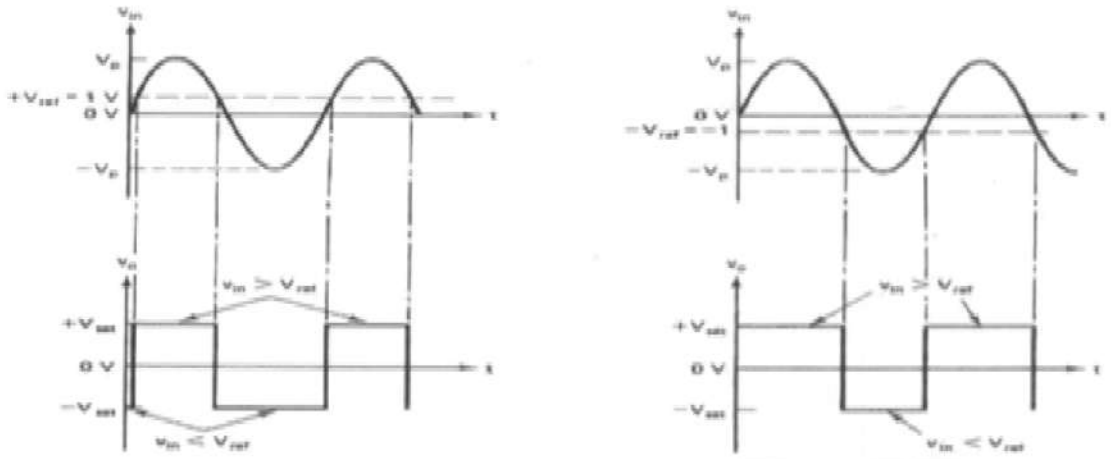
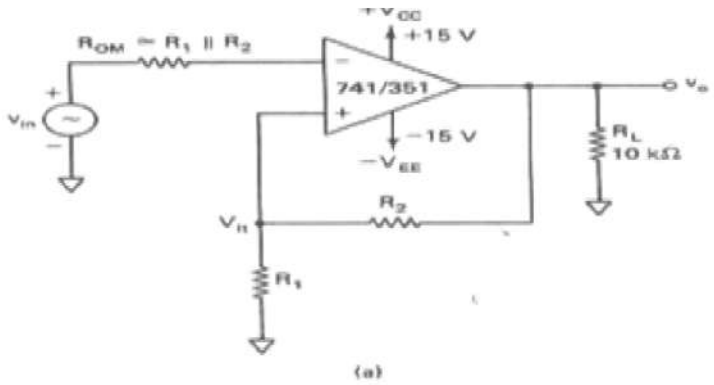


Figure 2.16 OP-AMP voltage comparator input and out put wave forms(a,b,c)

2.9 SCHMITT TRIGGER:

Below fig shows an inverting comparator with +ve feed back. This ckt converts an irregular shaped wave forms to a square wave form or pulse.The ckt is known as schitt trigger or squaring circuit.The i/p voltage being triggers the o/p Vo every time it exceeds certain voltage levels called the upper threshold voltage Vut and lower threshold voltage Vlt as shown in fig2.17 (b).In fig2.17(a) these thresold voltages are obtained by using the voltage divider R1,R2,whrere the voltage across R1 is F/B to +ve i/p.The voltage across R1 is a variable refference,thershold voltage that dependens on the value and polarity of the out put voltageVo.when Vo=+Vsat,the voltage across R1 is called the uper thershold voltage,Vut.

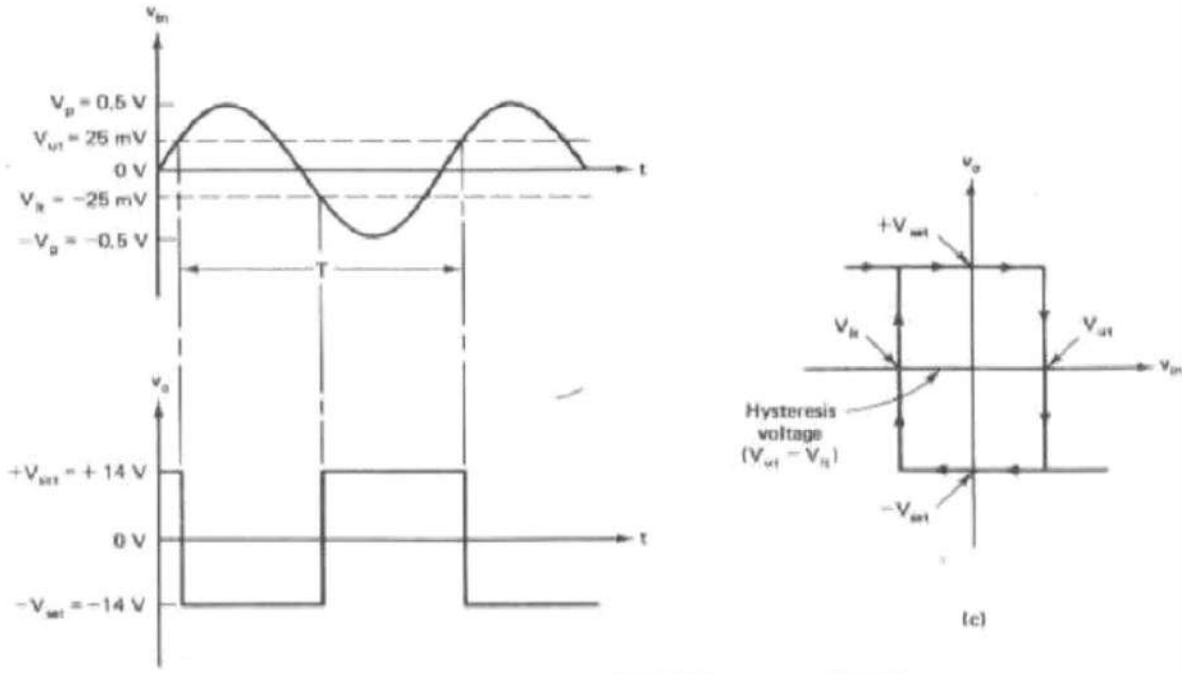


(a)

The input voltage Vin must be slightly more positive then Vut in order to cause the out put Vo to switch from +Vsat to –Vsat.as long as Vin less then Vut,Vo is at +Vsat.using the voltage divider rule,

On the other hand,when Vo=-Vsat, the voltage across R1 is referred to as the lower threshold voltage,Vlt.Vin must be slightly more negative than Vlt.in order to cause Vo to switch from-Vsat to +Vsat.in other words,for Vin values greater than Vlt,Vo is at –Vsat.Vlt is given by the following equation;

Thus if the threshold voltages Vut and Vlt are made large than the input noise voltages, the positive fed back will eliminate the false output transitions.Also the +ve feedback because of its regenerative action will make Vo switch faster between +Vsat and –Vsat.



(b)

Fig2.16.(a).inverting comparator as a schmitt trigger (b).input and output wave forms.(c).Vo versus Vin plot of the hysteresis voltage

Introduction to Voltage Regulators Features of 723 Regulator:

An unregulated power supply consists of a transformer (step down), a rectifier and a filter. These power supplies are not good for some applications where constant voltage is required irrespective of external disturbances. The main disturbances are:

1. As the load current varies, the output voltage also varies because of its poor regulation.
2. The dc output voltage varies directly with ac input supply. The input voltage may vary over a wide range thus dc voltage also changes.
3. The dc output voltage varies with the temperature if semiconductor devices are used.

An electronic voltage regulator is essentially a controller used along with unregulated power supply to stabilize the output dc voltage against three major disturbances

a. Load current (IL)
b. Supply voltage (Vi)
c. Temperature (T)

Fig.2.18, shows the basic block diagram of voltage regulator. where

Vi = unregulated dc voltage.

Vo = regulated dc voltage.

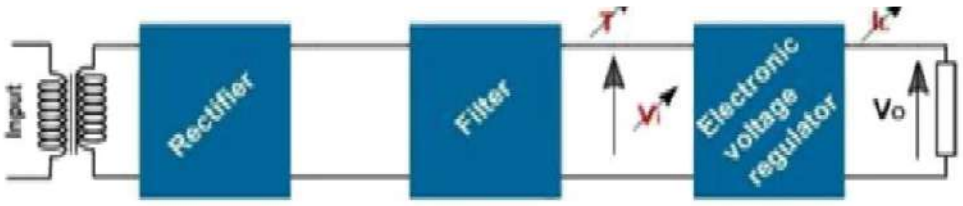


Fig.2.18 Block Diagram of voltage regulator

Since the output dc voltage VLo depends on the input unregulated dc voltage Vi, load current IL and the temperature t, then the change ΔVo in output voltage of a power supply can be expressed as follows

$$VO = VO(Vi, IL, T)$$

VO = VO(Vi, IL, T)

Take partial derivative of VO, we get,

$$\Delta V_0 \frac{\partial V_0}{\partial V_i}\Delta Vi + \frac{\partial V_0}{\partial IL}\Delta I_L + \frac{\partial V_0}{\partial T}\Delta T$$

or

$$\Delta V_0 = S_V\ \Delta V_i + R_L\ \Delta I_L + S_T\ \Delta T$$

$$S_V = \frac{\Delta V_0}{\Delta V_i}\Big|_{\substack{\Delta I_L=0 \\ \Delta T=0}}$$

$$R_0 = \frac{\Delta V_0}{\Delta I_L}\Big|_{\substack{\Delta V=0 \\ \Delta T=0}}$$

$$S_T = \frac{\Delta V_0}{\Delta T}\Big|_{\substack{\Delta V=0 \\ \Delta IL=0}}$$

SV gives variation in output voltage only due to unregulated dc voltage. RO gives the output voltage variation only due to load current. ST gives the variation in output voltage only due to temperature.

The smaller the value of the three coefficients, the better the regulations of power supply. The input voltage variation is either due to input supply fluctuations or presence of ripples due to inadequate filtering. A voltage regulator is a device designed to maintain the output voltage of power supply nearly constant. It can be regarded as a closed loop system because it monitors the output voltage and generates the control signal to increase or decrease the supply voltage as necessary to compensate for any change in the output voltage. Thus the purpose of voltage regulator is to eliminate any output voltage variation that might occur because of changes in load, changes in supply voltage or changes in temperature.

Zener Voltage Regulator:

The regulated power supply may use zener diode as the voltage controlling device as shown in fig.2.19. The output voltage is determined by the reverse breakdown voltage of the zener diode. This is nearly constant for a wide range of currents. The load voltage can be maintained constant by controlling the current through zener.

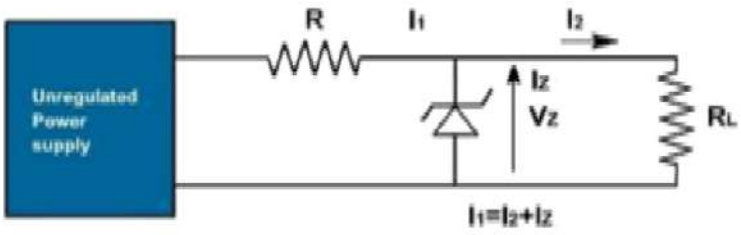


Fig.2.19Circuit diagram of Zener voltage regulator

The zener diode regulator has limitations of range. The load current range for which regulation is maintained, is the difference between maximum allowable zener current and minimum current required for the zener to operate in breakdown region. For example, if zener diode requires a minimum current of 10 mA and is limited to a maximum of 1A (to prevent excessive dissipation), the range is 1 - 0.01 = 0.99A. If the load current variation exceeds 0.99A, regulation may be lost.

Features of IC 723 Regulator:

3 terminal voltage regulators are capable of producing only fixed +ve or –ve output voltages. Moreover, such regulatorsdonothaveshortcircuitprotection.

Thereforethese3terminalregulatorsevolvedintodual polarity variable voltage regulators and further evolved into the monolithic linear voltage regulators and monolithic switchingregulators.

Oneexampleformonolithiclinearvoltageregulatoris IC723.

IC723generalpurposeregulatorovercomesthe limitationsof3terminalfixedvoltageregulators

IC723is a low current device.

Three Terminal Voltage Regulators:

There are basically two types of Three Terminal Fixed Voltage regulator ICs are available. One is positive output voltage and other has negative output voltage; but the output voltage is fixed.

There are two IC series.

1. 78XX series:

This is a positive regulator. The first two digits i.e.78 indicates that the output voltage is positive. The second two digits 'XX' indicates output voltage of the regulator. The available ICs of this series are 7805(+5V), 7812 (+12V), 7815(+15V) etc. The output voltages are shown in brackets.

2. 79XX series:

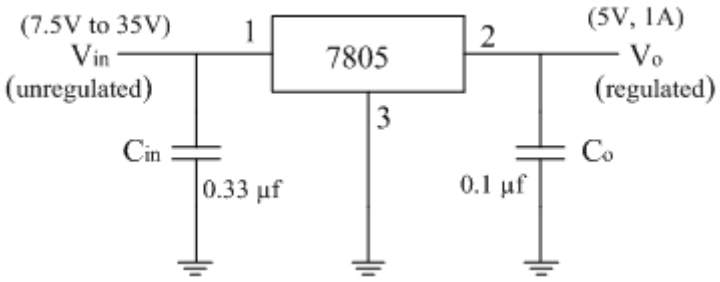
This is a negative voltage regulator. The first two digits i.e.79 indicates that the output voltage is

negative. The second two digits 'XX' indicates output voltage of the regulator. The available ICs of this series are 7905(-5V), 7912 (-12V), 7915(-15V) etc. The output voltages are shown in brackets.

These ICs are provided with adequate heat sinking and can deliver output currents more than 1A. These ICs require less external components. These are provided with internal thermal shut down, overload and short circuit protection.

These two series are available in two versions, like low power and high power. The low power versions are available in plastic and metal packages like transistors.

The high power versions are packaged in TO-3 type metal can or in T-220 type modulated plastic packages like power transistors. The typical value of output resistance is 8mΩ.



UNIT-II

OP-AMP, IC-555 & IC 565 APPLICATIONS

Introduction to Filters:

Anelectricfilterisoftenafrequency-selectivecircuitthatpassesaspecifiedbandoffrequencies andblocksorattenuatessignalsoffrequenciesoutsidethisband.Filtersmaybeclassifiedina numberof ways:

1. Analog ordigital

2. Passiveoractive

3. Audio (AF) or radio frequency (RF)

Analogfiltersaredesignedtoprocessanalogsignals,whiledigitalfiltersprocessanalogsignals usingdigitaltechniques.Dependingonthetypeofelementsusedintheirconstruction,filters maybe classifiedas passive or active. Elementsusedinpassivefiltersareresistors,capacitors,andinductors.Activefilters,onthe otherhand,employ transistorsorop-ampsinadditiontotheresistorsandcapacitors.Thetypeof element used dictates theoperatingfrequencyrangeof the filter.

Forexample,RCfiltersarecommonlyusedforaudioorlow-frequencyoperation,whereasLC orcrystalfiltersareemployedatRF orhighfrequencies.Especiallybecauseoftheirhigh Q value (figureof merit), the crystal providemorestable operation at higher frequencies.

- Basedonthecomponentsusedinthecircuitthe filtersaredividedintofollowingcategories.
  - Active filters
  - Passive filters

Active Filters:

- Activefiltersemploytransistorsorop-ampsin additiontoresistorsandcapacitors.

Passive Filters:

- Herethetypeofelementuseddictatesthe operatingfrequencyrangeofthefilter.

Eg:

- RCfiltersareusedforaudioorlowfrequency operation.
- LCorCrystalfiltersareusedatRForHighfrequencies. Anactivefilteroffersthefollowingadvantagesovera Passive filter.
- **GainandFrequencyadjustmentflexibility:**Sincethe op-ampiscapableofprovidingagain,theinputsignal is notattenuatedasitisinapassivefilter.Inaddition, theactivefilteriseasiertotuneoradjust.

Anactive filteroffers the following advantages overa passivefilter:

1.Gainandfrequencyadjustmentflexibility. Sincetheop-amp is capable of providing again, theinputsignalisnotattenuatedasitisinapassivefilter.Inaddition,theactivefilteriseasierto tune or adjust.

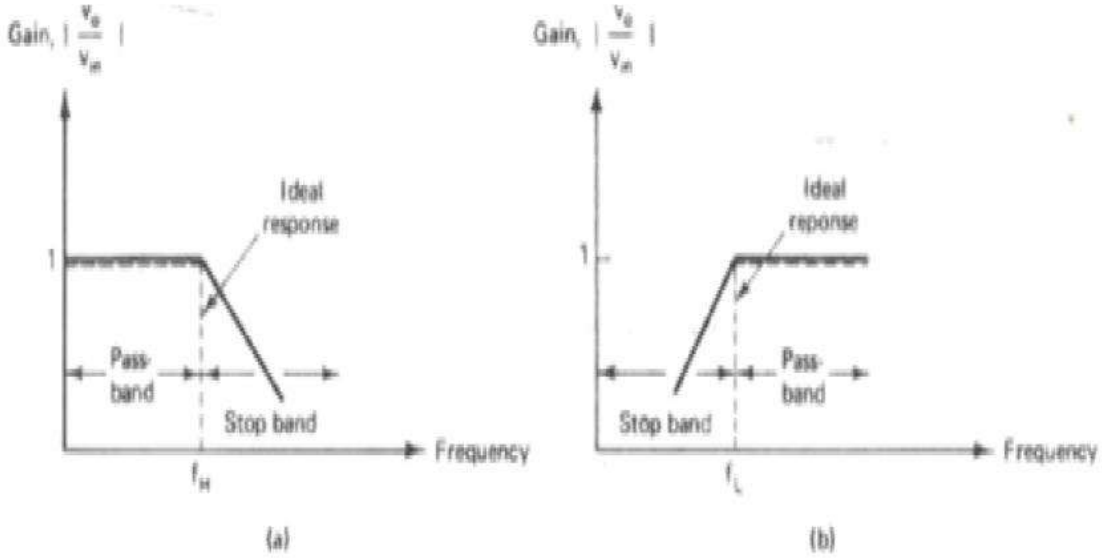
2.Noloadingprob1em. Because of the high inputresistanceand low outputresistance oftheop- amp, the active filterdoes not cause loading ofthesourceor load.

3.Cost. Typically,activefiltersaremoreeconomicalthanpassivefilters.Thisisbecauseofthe varietyof cheaper op-amps and the absenceof inductors.

Themostcommonlyused filters arethese:

1. Low-pass filter
2. High-pass filter
3. Band-pass filter
4. Band-reject filter
5. All-pass filter

Characteristics of Band Pass,Band Reject filters:



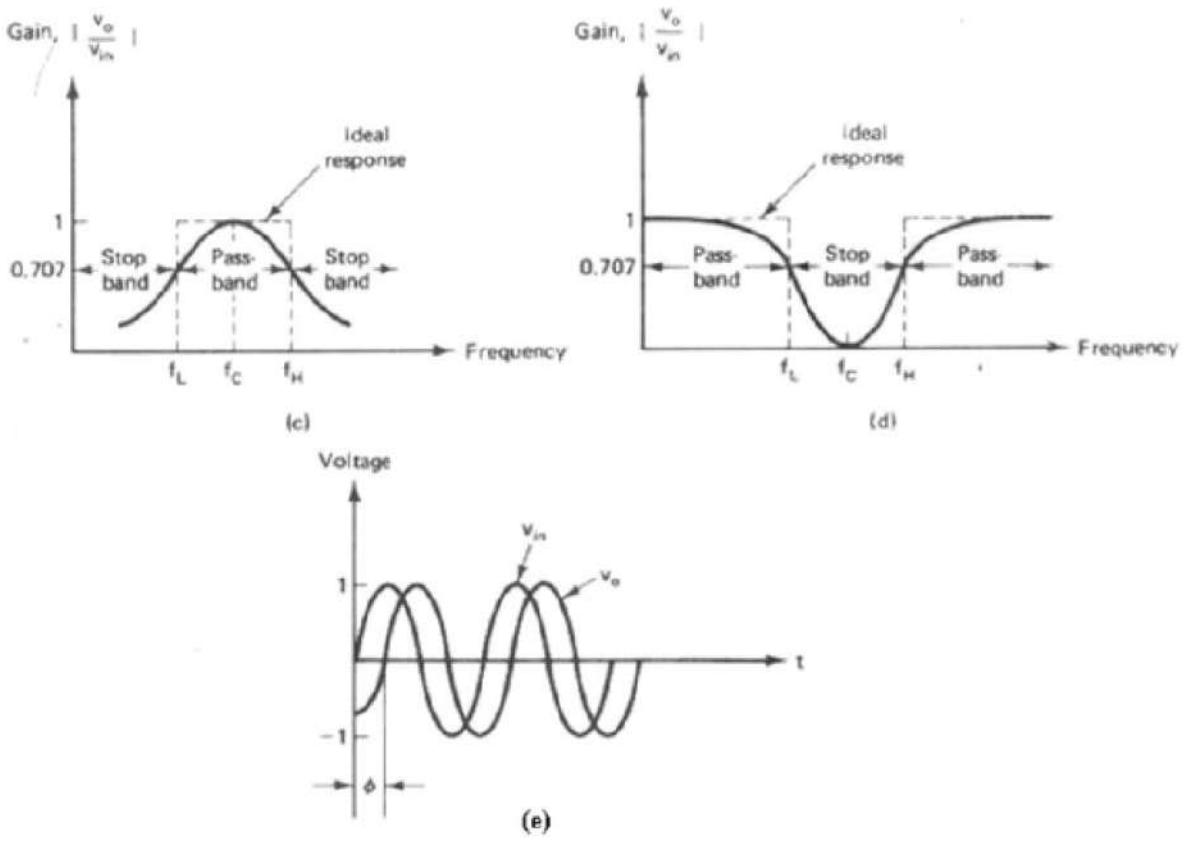


Fig 3.1 frequency response of major active filters (a)Low pass (b)High pass (c)Band pass (d)Band reject (e) All pass

Fig.3 . 1 showsthefrequencyresponsecharacteristicsofthefivetypesoffilters.Theideal responseisshownby dashedcurves,whilethesolidlinesindicatethepracticalfilterresponse.A low-passfilterhasaconstantgain from0Hztoahighcutofffrequencyf_H.Therefore,the bandwidth is also f_H.

Atf_H thegainisdownby3dB;afterthat ($f>f_H$)itdecreaseswiththeincreaseininput frequency. The frequencies between 0 HzandfH areknownas thepassbandfrequencies,whereas therangeoffrequencies,thosebeyondf_H thatareattenuatedincludesthestopbandfrequencies.

Fig.3.1(a)showsthefrequencyresponseofthelow-passfilter.Asindicatedbythedashedline, anidealfilterhasa zerolossinitspassbandandinfinitelossinitsstopband.Unfortunately,ideal filter response is not practical because linear networks cannot produce the discontinuities. However,itispossibletoobtainapractical responsethatapproximatestheidealresponseby usingspecial design techniques, as well as precision component values andhigh-speed op-amps.

Butterworth,Chebyshev,andCauerfiltersaresomeofthemostcommonlyusedpracticalfilters thatapproximatetheidealresponse.ThekeycharacteristicoftheButterworthfilteristhatithas a flat passbandas wellasstopband. Forthis reason, itis sometimes calledaflat-flatfilter.

TheChebyshevfilterhasaripplepassbandandflatstopband,i.e.theCauerfilterhasaripple passbandanda ripplestopband.Generally,theCauerfiltergivesthebeststopbandresponse amongthethree.Becauseoftheirsimplicityofdesign,thelow-passandhigh-passButterworth filters arediscussed here.

Figure3 -1(b)showsahigh-passfilterwithastopband0<f<f_L andapassbandf>f_L.f_L isthe low cutoff frequency, andfis the operating frequency. Aband-pass filterhas apassband between twocutoff frequencies f_H and f_L,wheref_H>$f_L$and two stop-bands: 0<f<$f_L$and f>f_H.Thebandwidthoftheband-passfilter,therefore,isequaltof$_H$ - f_L.Theband-rejectfilter performs exactly oppositetotheband-pass;thatis,ithas aband-stop betweentwo cutoff frequenciesf_H andf_L andtwopassbands:0<f<f_L andf>f_H.Theband-rejectisalsocalleda band-stoporband-eliminationfilter.The frequencyresponsesofband-passandband-reject filtersareshowninFigure3-1(c)and(d),respectively.Inthesefigures,fc iscalledthecenter frequencysinceit is approximatelyat thecenter ofthe passband orstopband.

Fig.3.1(e)showsthephaseshiftbetweeninputandoutputvoltagesofanall-passfilter.Thisfilter passesallfrequenciesequallywell;thatis,outputandinputvoltagesequalinamplitudeforall frequencies,withthephaseshiftbetweenthetwoafunctionoffrequency.Thehighestfrequency uptowhichtheinput andoutput amplitudesremainequal isdependentontheunitygain bandwidthoftheop-amp.(Atthisfrequency, however, thephaseshiftbetweentheinputand outputismaximum.

Therateatwhichthegainofthefilterchangesinthestopbandisdeterminedbytheorderofthe filter.Forexample,forthefirstorderlow-passfilterthegain-rolls-offattherateof20dB/decade inthestopband,thatis,forf>f_H;ontheotherhand,forthesecond-orderlow-passfiltertheroll-offrateis40dB/decadeandsoon.By contrast,forthefirst-orderhigh-passfilterthegain increases at the rate of 20 dB/decade in the stopband, that is, until f=f_L;the increase is 40dB/decade for thesecond-order high-pass filter;

Analysis of 1st order LPF & HPF Butterworth Filters:

Fig. 3-2 shows a first-order low-passButterworthfilterthat uses an RCnetwork for filtering. Notethat the op-amp is used in thenon-invertingconfiguration; henceitdoes not load down the RCnetwork. ResistorsR1 and RF determinethegain of the filter.Accordingto thevoltage-divider rule, the voltageat thenon-invertingterminal (acrosscapacitor C)is

$$V_1 = \frac{-jX_C}{R - jX_C} V_{in}$$

$$j = \sqrt{-1} \ and \ -jX_C = \frac{1}{j2\pi fC}$$

$$V_1 = \frac{V_{in}}{1 + j2\pi fRC}$$

$$V_o = 1 + \frac{R_F}{R_1} V_1$$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) \frac{V_{in}}{1 + j2\pi fRC}$$

$$\frac{V_o}{V_{in}} = \frac{A_F}{1 + j\left(f / f_H\right)} \qquad \ldots\ldots\ldots 3.1$$

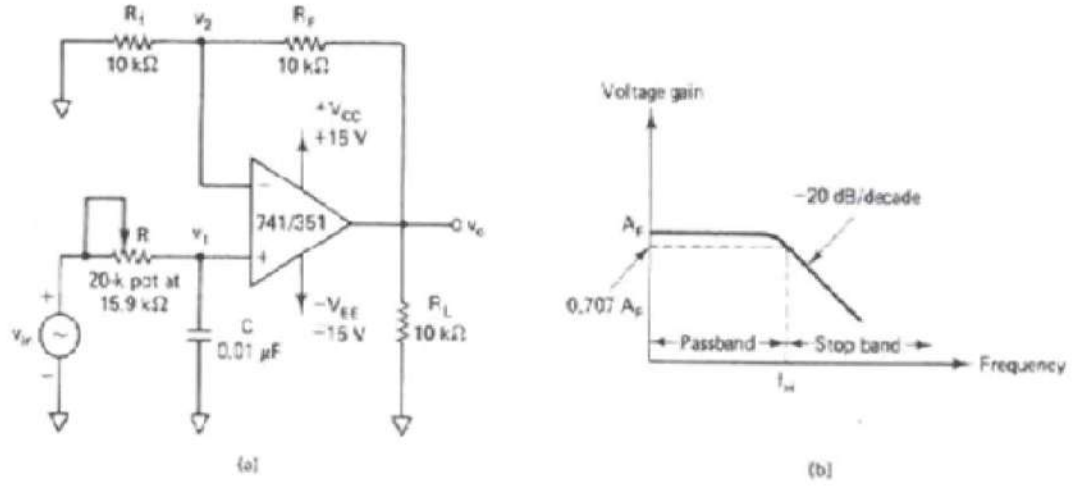


Fig.3.2.First order Low Pass Butter Worth Filter (a)circuit (b)Response

Where V_o/V_{in} = gain of the filter as a function of frequency

$A_F = \left(1 + \frac{R_F}{R_1}\right)$ = passaband gain of the filter

f = input frequency of the filter

$f_H = \frac{1}{2\pi RC}$ = upper cut-off frequency of the filter.

Thegain magnitude andphase angleequations ofthe low-pass filter can beobtained by convertingEquation 3.1into its equivalent polar form, as follows:

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}}$$

$$\phi = -tan^{-1}\left(\frac{f}{f_H}\right)$$

Whereφ is the phase angle in degrees.

The operation of the low pass filter can be verified from the gain magnitude equation:

1. At very low frequencies that is , f<f_H, $\left|\frac{V_o}{V_{in}}\right| = A_F$
2. At f=f_H, $\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{2}}$ = 0.707 A_F
3. At f>f_H , $\left|\frac{V_o}{V_{in}}\right| < A_F$

FilterDesign

Alow-pass filtercan bedesignedbyimplementingthe foI1owingsteps:

1. Chooseavalue ofhigh cutoff frequencyf_H.

2. Select a value of C less than or equal to 1 μF. Mylar or tantalum capacitors are recommendedforbetterperformance.

3. Calculate thevalue of Rusing $R = \frac{1}{2\pi f_H C}$

4.Finally, select values ofR1 and $R_F$dependent on thedesired passband gain $A_F$using

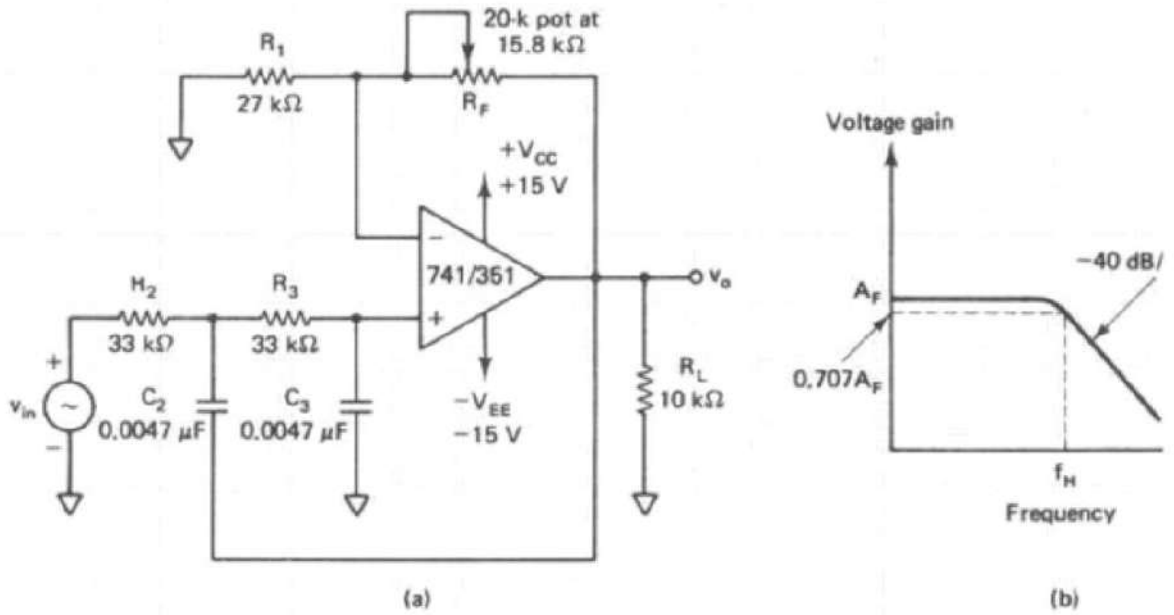
$$A_F = 1 + \frac{R_f}{R_1}$$

Frequency Scaling

Onceafilterdesigned;theremaysometimes beaneed to changeits cutofffrequency. The procedureusedto convert an originalcutofffrequency$f_H$toa new cutofffrequencyf'_Hiscalled frequencyscaling.Frequencyscalingis accomplished as follows. To change ahigh cutoff frequency, multiple RorC. but notboth, bytheratio of theoriginalcutoff frequencyto thenew cutofffrequency.

3.1.2 SECOND-ORDER LOW-PASSBUTTER WORTH FILTER

A stop-band response having a 40-dB/decade roll-off is obtained with the second order low-passfilter. A first-order low-pass filter can be converted into a second order type simply by using anadditional RC network, as shown in Fig.3.3.



Second-order filters are important because higher-order filters can be designed using them. Thegain of the second-order filter is set by R_1 and R_F, while the high cutoff frequency f_H isdetermined by R_2, C_2, R_3, and C_3, as follows

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

Furthermore, for asecond-order low-passButterworth response, thevoltagegain magnitude equation is

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^4}}$$

Where V_o/V_{in} = gain of the filter as a function of frequency

$A_F = \left(1+\frac{R_F}{R_1}\right)$ = passaband gain of the filter

f = input frequency of the filter

$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$ = upper cut-off frequency of the filter

3.2 HIGH PASS FILTER

3.2.1 .FIRST-ORDER HIGH-PASSBUITERWORTH FILTER

allfrequencies higher than f_L arepassband frequencies,with thehighest requency determined bythe closed-loop bandwidth of the op-amp.

Notethat the high-pass filter of Figure3.4(a) and thelow-pass filter of Figure3.4(a) arethe same circuits, except thatthe frequency-determiningcomponents(R and C) areinterchanged.

Forthe first-order high-pass filter ofFigure3.4(a), the outputvoltageis

$$V_o = \left(1 + \frac{R_f}{R_1}\right)\frac{j2\pi fRC}{1 + j2\pi fRC}V_{in}$$

$$\frac{V_o}{V_{in}} = A_F\frac{j(f/f_L)}{\sqrt{1 + j(f/f_L)}}$$

Hencethemagnitudeof thevoltagegain is

$$\left|\frac{V_o}{V_{in}}\right| = A_F\frac{(f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

Where $A_F = \left(1 + \frac{R_F}{R_1}\right)$ = passaband gain of the filter

f = input frequency of the filter

$f_L = \frac{1}{2\pi RC}$ = Lower cut-off frequency of the filter

Sincehigh-pass filters are formed from low-pass filters simplybyinterchangingR's and*C's,* the design and frequencyscalingprocedures of thelow-pass filters are also applicable to the high- pass filters.

Waveform Generators

Therearedifferenttypesofwaveform generatorswhicharegivenbelow.

1 Square wavegenerator

2 Triangular wave generator 3Sawtoothwavegenerator

SquarewaveGenerator(AstableMultivibrator)

- Asimpleop-ampsquarewavegeneratoris shown inFigure 5.10a.

Square wave generator

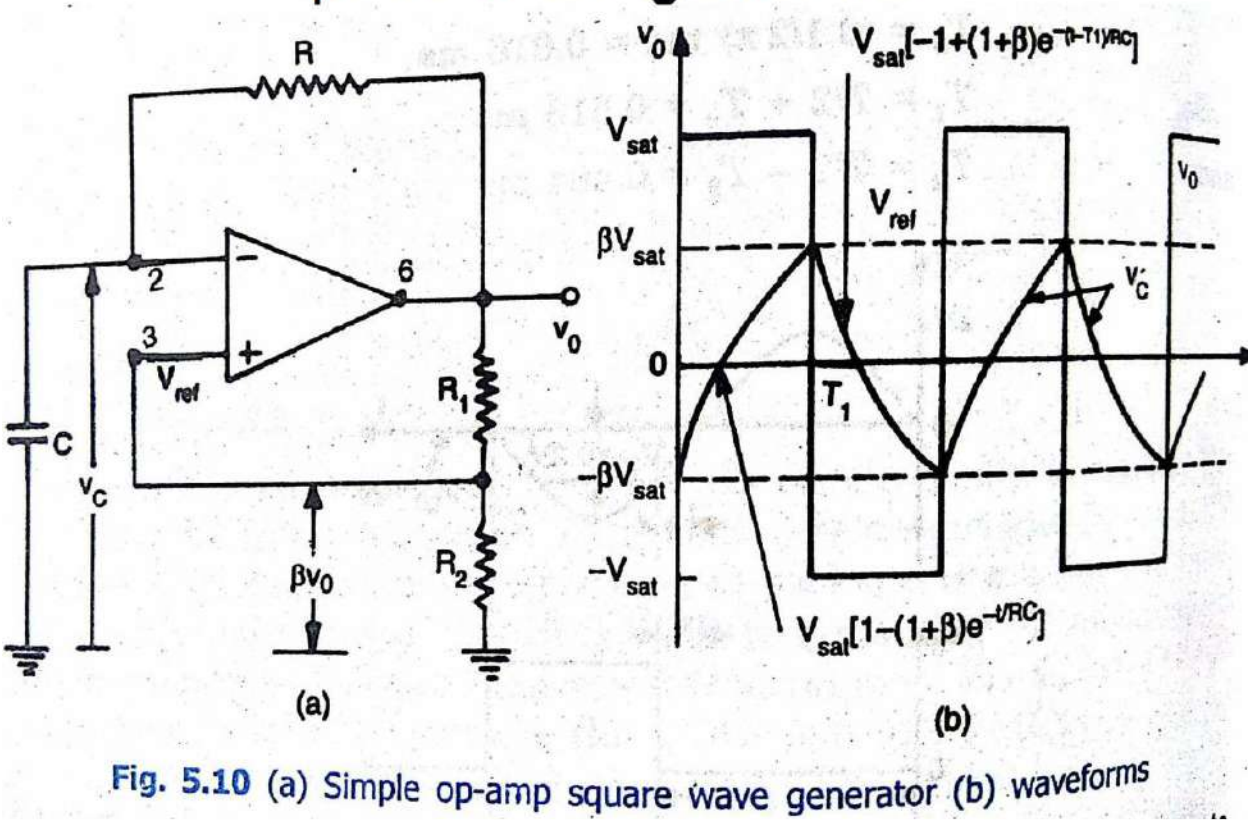


Fig. 5.10 (a) Simple op-amp square wave generator (b) waveforms

- ItisalsocalledaFreerunningoscillator.
- Theprincipleofgenerationofsquarewave outputistoforceanop-amptooperatein saturationregion.
- InFigure5.10(a),fractionβ=R2/(R1+R2)of the output is fed back to the +ve input terminal. Thus the reference voltage Vref is βVoandmaytakevaluesas+βVsator–βVsat.

- Theoutputisalsofedbacktothe–veinput terminalafterintegratingbymeansofalow pass RCcombination.
- Wheneverinputatthe–veinputterminaljust exceeds Vref, switching takes place resulting in a square wave output.
- InAstablemultivibrator,boththestatesare quasi stable.

Frequency Derivation

Thefrequencyisdeterminedbythetimeittakesthecapacitor tochargefrom–βVsatto+βVsatandviceversa.

Thevoltageacrossthecapacitorasafunctionoftimeisgiven by

Vc(t)=Vf+(Vi–Vf)e^-t/RC where,thefinalvalue,Vf=

+Vsat andtheinitialvalue,Vi=–βVsat

Therefore Vc(t)=+Vsat+(–βVsat–Vsat)e^-t/RC Vc(t)=Vsat–Vsat(1+β)e^-t/RC

Att=T1,voltageacrossthecapacitorreachesβVsatand switching takesplace.

- Therefore

Vc(T1)=βVsat=Vsat–Vsat(1+β)e^-T1/RC Afteralgebraicmanipulation,weget

T1 = RC ln (1+ β)/(1- β)

This gives only one half of the period.

Therefore the total time period,

=2*T1=2RCln(1+β)/(1-β)andtheoutputwaveform is symmetrical.

IfR1=R2,thenβ=0.5andT=2RCln3 and for

R1=1.16R2,itcanbeseenthat

T = 2RC or fo = 1/2RC

Triangular Wave Generator

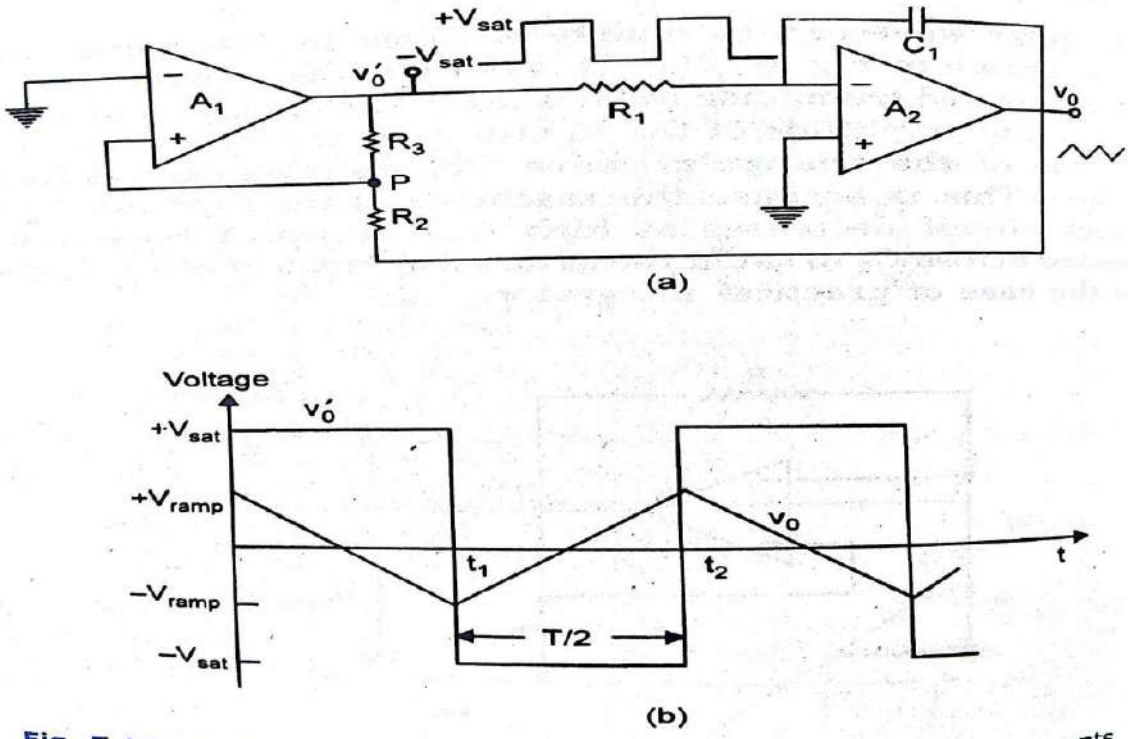


Fig. 5.13 (a) Triangular waveform generator using lesser components (b) Waveforms

Itbasicallyconsistsofatwolevelcomparator followedbyanintegrator.

TheoutputofthecomparatorA1isasquare waveofamplitude+or–Vsatandisapplied tothe–veinputterminalofthe integratorA2 producingatriangularwave.Thistriangular waveisfedbackasinputtothecomparator A1througha voltagedividerR2R3.

Initially,letusconsiderthattheoutputofthe comparatorA1isat+Vsat.Theoutputofthe integratorA2willbea–ve goingrampasshown in figure 5.13b. This one end of the voltage dividerR2R3isatavoltage+Vsatandtheotherat the–vegoingrampofA2.

Atatimet=t1,whenthe–vegoingrampattainsa valueof–Vramp,theeffectivevoltageatpointp becomesslightlyless than0volts.Thisswitches theoutputofA1,frompositivesaturationlevelto negativesaturationlevel–Vsat.

DuringthetimewhentheoutputofA1isat -Vsat, theoutputofA2increasesinthepositivedirection.

Andattheinstantt=t2,thevoltageatpointpbecomes justabove0volts,therebyswitchingtheoutputofA1 from–Vsatto +Vsat.Thecyclerepeatsandgeneratesa triangularwaveform.

Itcanbeseenthatthefrequencyofthesquarewave andtriangularwavewillbethesame.

However, the amplitude of the triangular wave dependsupontheRCvalueoftheintegratorA2and output voltagelevelofA1.

DerivationofFrequencyofTriangularWaveform

- Theeffectivevoltageatpointpduringthetime whenoutputofA1isat+Vsatlevelisgivenby

-Vramp+(R2/(R2+R3))[+Vsat–(-Vramp)]--Eq(1)

At t=t1, the voltage at point p becomes approximatelyequaltozero.Thereforefrom Eq(1),weget
Vramp = (-R2/R3)(+Vsat)

Similarlyatt=t2,whentheoutputofA1switches from –Vsat to+Vsat

Vramp = (-R2/R3) (-Vsat) = (R2/R3) Vsat

hereforepeaktopeakamplitudeofthetriangularwaveis Vo (pp) = +Vramp – (-Vramp)
Vo (pp) =2Vramp =2(R2/R3) Vsat ----Eq(2)

Theoutputswitchesfrom–Vrampto+Vrampinhalfthetime period T/2.

PuttingthevaluesinthebasicintegratorequationVo=- (1/RC) ∫Vi dt, we get

Vo(pp)=-(1/R1C1) 0∫T/2 (-Vsat)dt =(Vsat/R1C1) (T/2) Therefore T=2 R1C1 Vo(pp)/Vsat

PuttingthevalueofVo(pp)fromEq(2),weget T = 4R1 C1 R2/R3

Hencethefrequencyofoscillationfois

fo =1/T=R3/4R1C1R2

SawtoothWaveGenerator

- Thedifferencebetweenthetriangularand sawtoothwaveformsisthat

risetimeandfalltimeareequal–Triangular risetimeandfalltimeareunequal–Sawtooth

- Thetriangularwavegeneratorcanbeconverted intoasawtoothwavegeneratorbyinjectinga variable DC voltage into the non-inverting terminaloftheintegratorA2.
- This can be accomplished by using the potentiometerandconnectingittothe+Vccand

-VeeasshowninFigure 8-24(a)

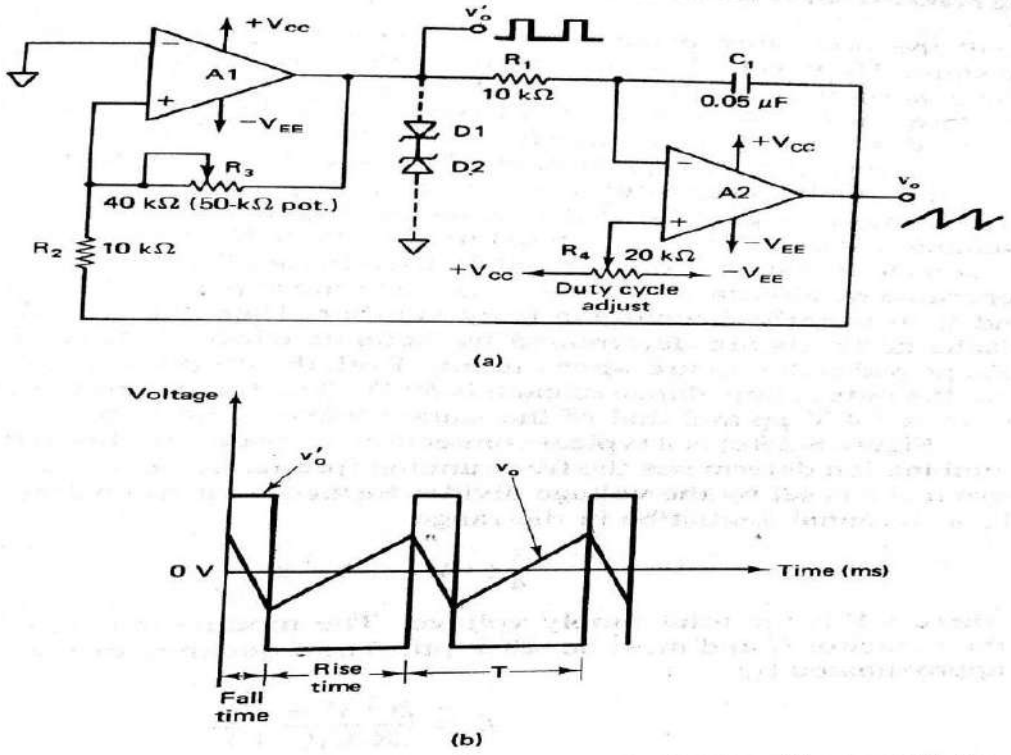


Figure 8–24 Sawtooth wave generator. (a) Circuit. A_1 and A_2 dual op-amp: 1458/353. D_1 and D_2: IN4735 with $V_Z = 6.2$ V. (b) Output waveform when noninverting input of A_2 is at some nega-

- DependingontheR4setting,acertainDClevelis insertedin theoutputofA2.
- NowsupposethattheoutputofA1isasquarewave andthepotentiometerR4isadjustedforacertainDC level.
- ThismeansthattheoutputofA2willbeatriangular wave,ridingonsomeDClevelthatisafunctionofthe R4 setting.
- Thedutycycleofthesquarewavewillbedetermined bythepolarityandamplitudeofthisDClevel.
- Adutycyclelessthan50%willthencausetheoutput ofA2 to be a sawtooth.

- Withthewiperatthecenterof R4,theoutput of A2 is a triangular wave. For any other positionofR4wiper,the outputisasawtooth waveform.

R4wiperistowards**–Vee**,the**risetimeismore**

R4wiperistowards**+Vcc**,the**falltimeismore**

IC555 Timer – Functional Diagram

One of the most versatile linear integrated circuits is the 555 timer. A sample of these applications includes mono-stable and astable multivibrators, dc-dc converters, digital logic probes, waveform generators, analog frequency meters and tachometers, temperature measurement and control, infrared transmitters, burglar and toxic gas alarms, voltage regulators, electric eyes, and many others.

The 555 is a monolithic timing circuit that can produce accurate and highly stable time delays or oscillation. The timer basically operates in one of the two modes: either as monostable (one-shot) multivibrator or as an astable (free running) multivibrator.The device is available as an 8-pin metal can, an 8-pin mini DIP, or a 14-pin DIP.

The SE555 is designed for the operating temperature range from -55°Cto + 125°C, while the NE555 operates over a temperature range of 0° to +70°C. The important features of the 555 timer are these: it operates on +5 to + 18 V supply voltage in both free-running (astable) and one- shot (monostable) modes; it has an adjustable duty cycle; timing is from microseconds hrough hours; it has a high current output; it can source or sink 200 mA; the output can drive TTL and has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature, or equivalently 0.005%/°C.

Like general-purpose op-amps, the 555 timer is reliable, easy to us, and low cost.

Pin 1: Ground. All voltages are measured with respect to this terminal.

Pin 2: Trigger. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. The output is low if the voltage at this pin is greater than 2/3 Vcc. However,when a negative-going pulse of amplitude larger than 1/3 Vcc is applied to this pin, the comparator 2 output goes low, which in turn switches the output of the timer high [see Figure 4-

1(b)]. The output remains high as long as the trigger terminal is held at a low voltage.

Pin 3: Output. There are two ways a load can be connected to the output terminal: either between pin 3 and ground (pin 1) or between pin 3 and supply voltage + Vcc (pin 8) . When the output is low, the load current flows through the load connected between pin 3 and + Vcc into the output terminal and is called the sink current.

However, the current through the grounded load is zero when the output is low. For this reason, the load connected between pin 3 and + Vcc is called the normally on load and that connected between pin 3 and ground is called the normally off load.

On the other hand, when the output is high, the current through the load connected between pin 3and + Vcc (normally on load) is zero. However, the output terminal supplies current to the normally off load. This current is called the source current. The maximum value of sink or source current is 200 mA.

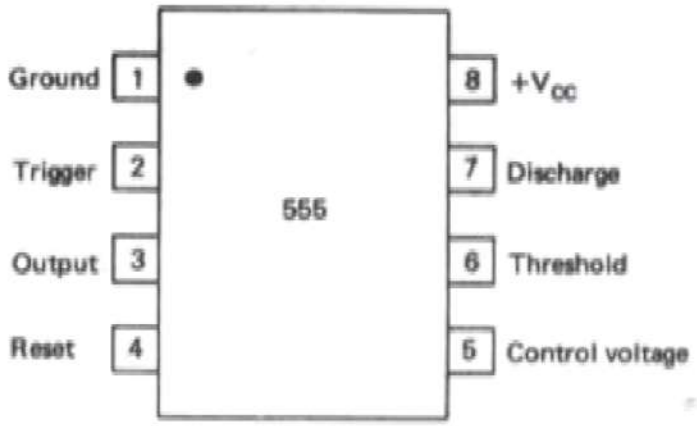


Fig 4-1 Pin diagram of 555Timer

Pin 4: Reset. The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to + Vcc to avoid any possibility of false triggering.

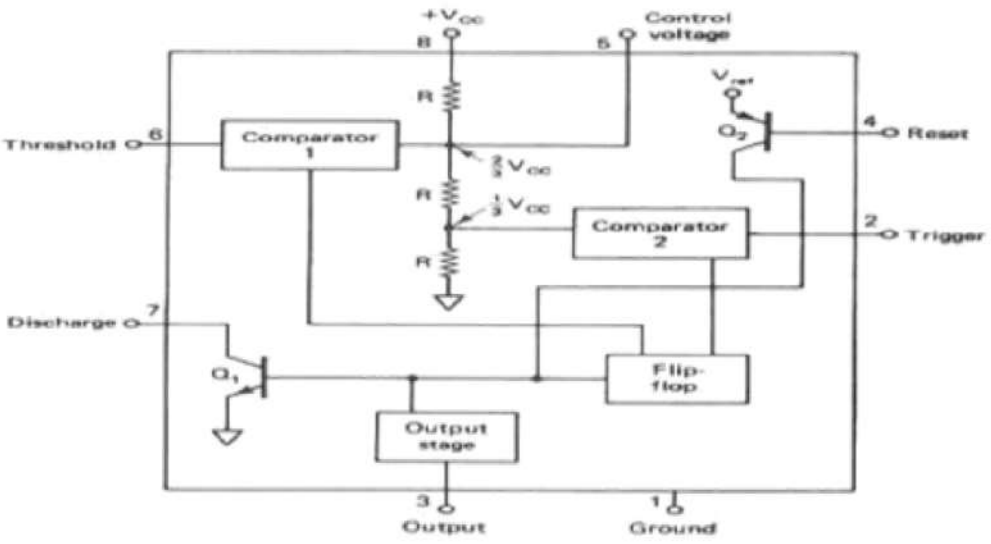


Fig 4-1(a) Block Diagram

Pin 5: Control voltage. An external voltage applied to this terminal changes the threshold as well

as the trigger voltage . In other words, by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a 0.01-μF capacitor to prevent any noise problems.

Pin 6: Threshold. This is the non-inverting input terminal of comparator 1, which monitors the voltage across the external capacitor . When the voltage at this pin is threshold voltage 2/3 V, the output of comparator 1 goes high, which in turn switches the output of the timer low.

Pin 7: Discharge. This pin is connected internally to the collector of transistor Q1, as shown in Figure 4-1(b). When the output is high, Q1 is off and acts as an open circuit to the external capacitor C connected across it. On the other hand, when the output is low, Q1 is saturated and acts as a short circuit, shorting out the external capacitor C to ground.

Pin 8: + Vcc. The supply voltage of +5 V to +18 is applied to this pin with respect to ground (pin 1).

4.2. FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER

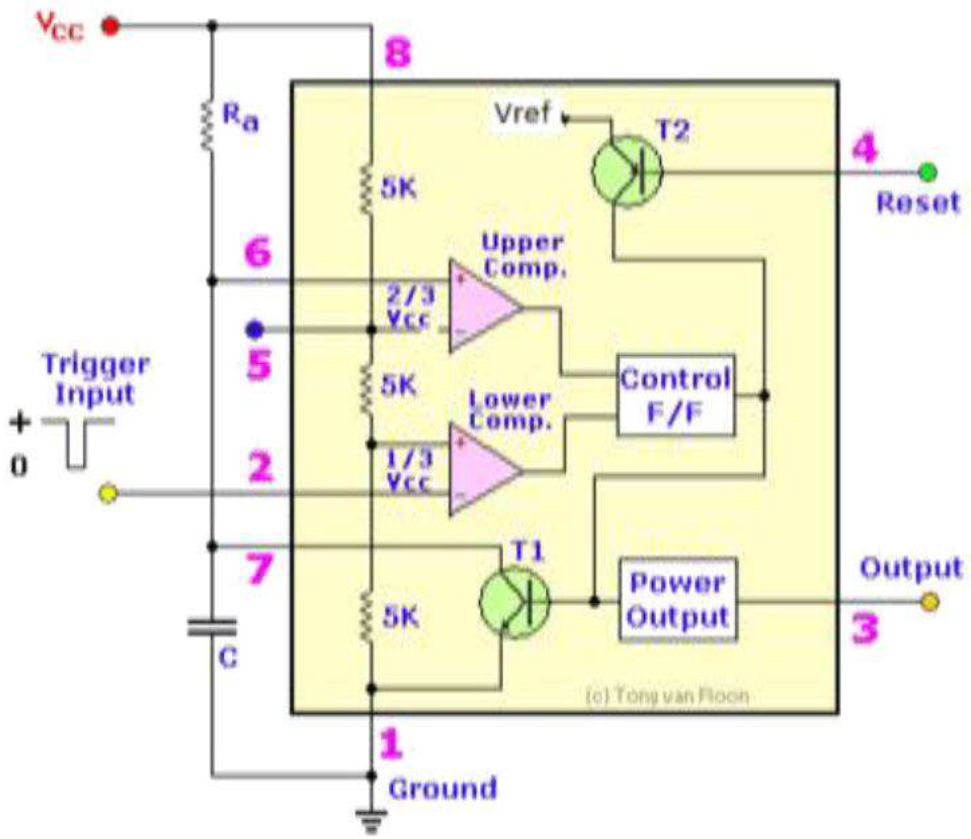


Fig 4-1(b) Block diagram of timer

Monostable Multivibrators:

A monostable multivibrator, often called a one-shot multivibrator, is a pulse- generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer.

In a stable or standby state the output of the circuit is approximately zero or at logic-low level. When an external trigger pulse is applied, the output is forced to go high (≈Vcc). The time the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats.

The monostable circuit has only one stable state (output low), hence the name mono-stable. Normally, the output of the mono- stable multivibrator is low. Fig 4.2 (a) shows the 555 configured for monostable operation. To better explain the circuit's operation, the internal block diagram is included in Fig 4-2(b).

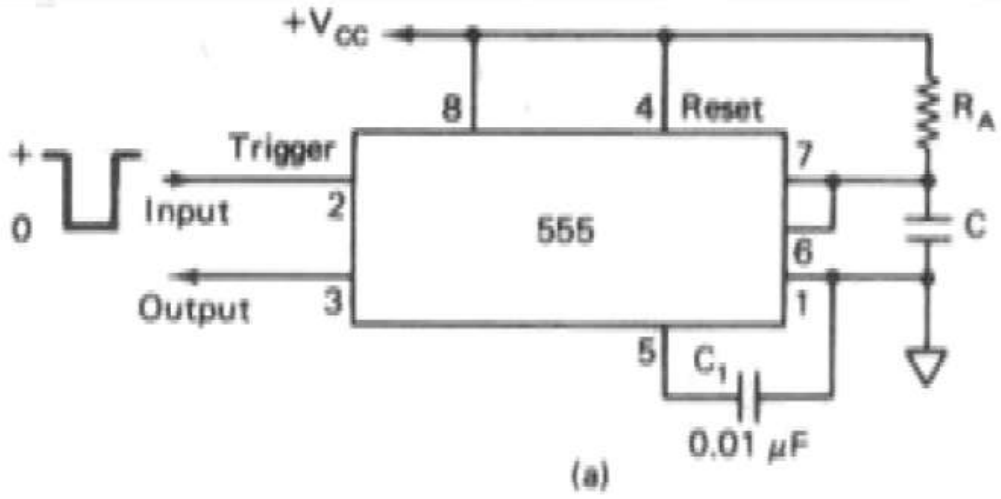


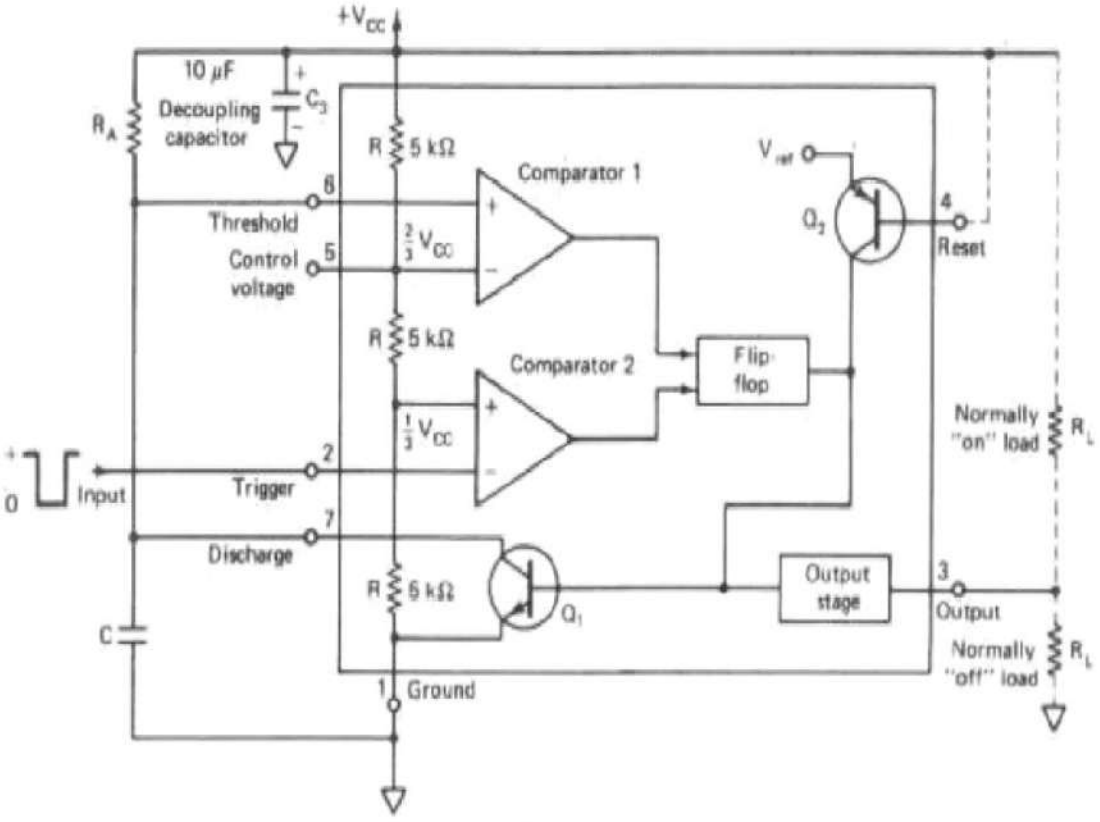
Figure 4-2(a) IC555 as monostable multivibrator

Mono-stable operation: According to Fig 4-2(b), initially when the output is low, that is, the circuit is in a stable state, transistor Q is on and capacitor C is shorted out to ground. However, upon application of a negative trigger pulse to pin 2, transistor Q is turned off, which releases the short circuit across the external capacitor C and drives the output high. The capacitorC now starts charging up toward V_{cc} through R_A.

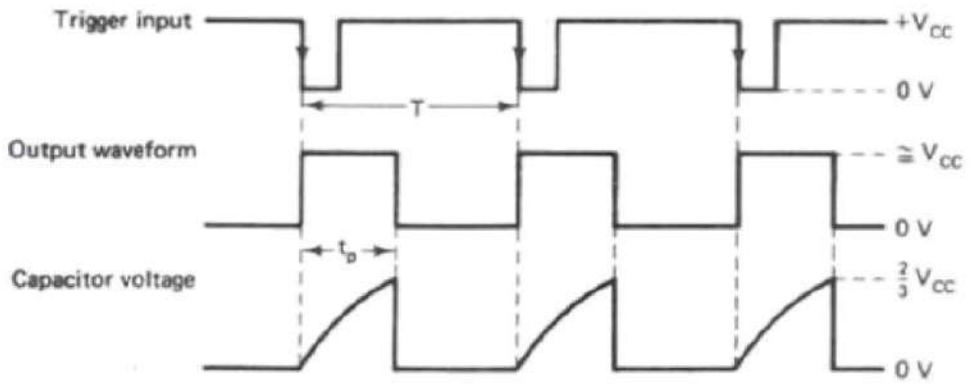
However, when the voltage across the capacitor equals 2/3 Va., comparator I 's output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time, the output of the flip-flop turns transistor Q on, and hence capacitor C rapidly discharges through the transistor.

The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats. Figure 4-2(c) shows the trigger input, output voltage, and capacitor voltage waveforms. As shownhere, the pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also, the trigger pulse must be a negative-going input signal with amplitude larger than 1/3 the time during which the output remains high is given by where

$t_p - 1.1R_AC$



(b)



(c)

Fig.4-2 (b)555 connected as a Monostable Multivibrator (c)input and output waveforms

4.3.1 Monostable Multivibrator Applications

(a) Frequency divider: The monostable multivibrator of Figure 4-2(a) can be used as a frequency divider by adjusting the length of the timing cycle t_p, with respect to the tine period T of the trigger input signal applied to pin 2. To use monostable multivibrator as a divide-by-2 circuit, the timing interval t_p must be slightly larger than the time period T of the trigger input signal, as shown in Figure 4-4. By the same concept, to use the monostable multivibrator as a divide-by-3 circuit, t_p must be slightly larger than twice the period of the input trigger signal, and

so on. The frequency-divider application is possible because the monostable multivibrator cannot betriggered during the timing cycle.

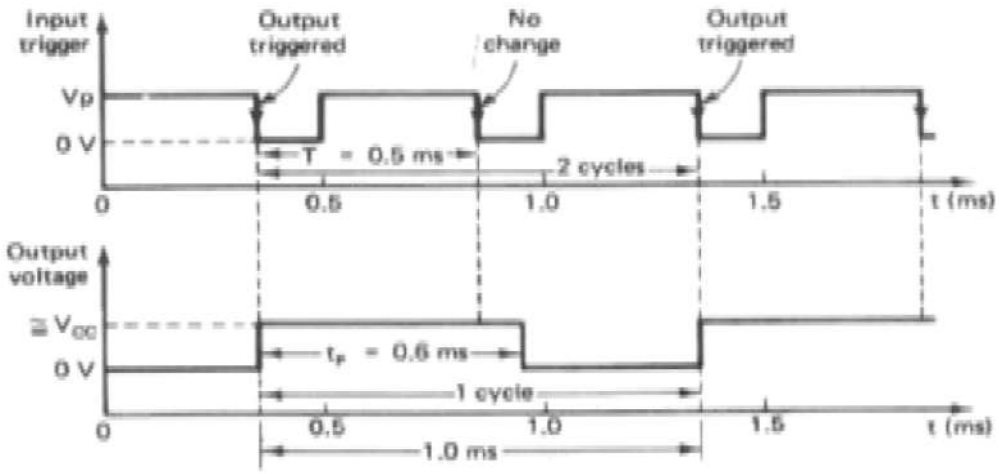


Fig 4-4 input and output waveforms of a monostable multi vibrator as a divide-by-2 network

(b) Pulse stretcher: This application makes use of the fact that the output pulse width (timing interval) of the monostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name pulse stretcher. Often, narrow-pulse- width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but is not visible to the eye because its on time is infinitesimally small compared to its off time. The 555 pulse stretcher can be used to remedy this problem

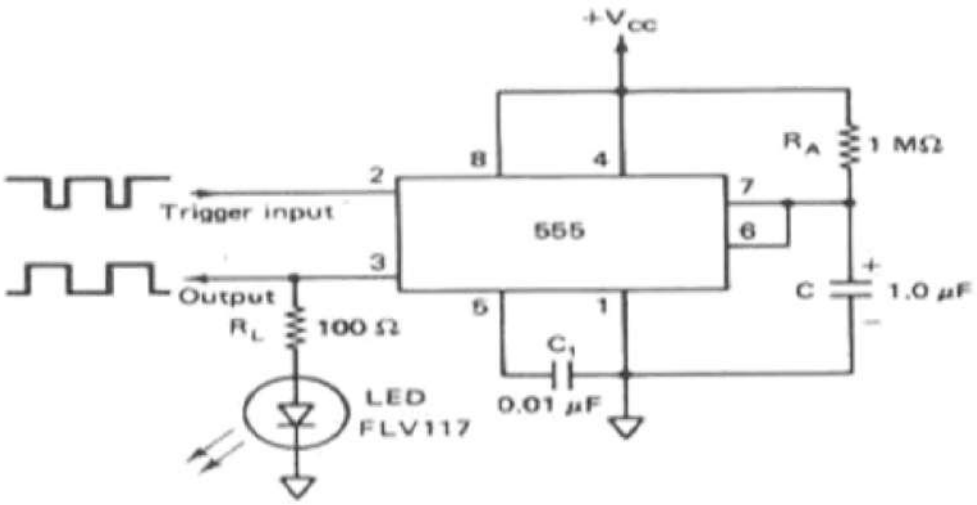


Fig 4-5 Monostable multi vibrator as aPulse stretcher

Figure 4-5 shows a basic monostable used as a pulse stretcher with an LED indicator at the output. The LED will be on during the timing interval $t_p = 1.1R_AC$, which can be varied by changing the value of R_A and/or C.

4.4 THE 555 AS AN ASTABLE MULTIVIBRATOR

The 555 as an Astable Multivibrator, often called a free-running multivibrator, is a rectangular-wave-generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name freerunning. However, the time during which the output is either high or low is determined by the two resistors and a capacitor, which are externally connected to the 555 timer. Fig 4-6(a) shows the 555 timer connected as an astable multivibrator. Initially, when the output is high, capacitor C starts charging toward V through RA and R8. However as soon as voltage across the capacitor equals 2/3 Vcc, comparator I triggers the flip flop, and the output switches low [see Fig 4-6(b)]. Now capacitor C starts discharging through R8 and transistor Q. When the voltage across C equals 1/3 comparator 2's output triggers the flip-flop, and the output goes high. Then the cycle repeats.

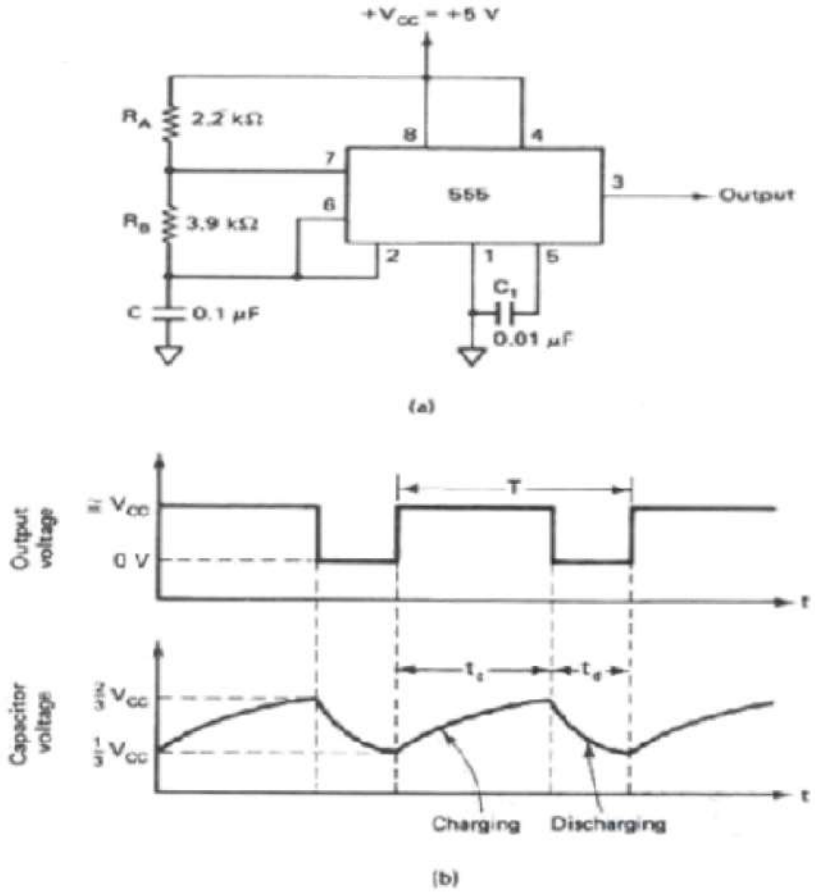


Fig 4-6 The 555 as a Astable Multivibrator (a)Circuit(b)Voltage across Capacitor and O/P waveforms.

The output voltage and capacitor voltage waveforms are shown in Figure 4-6(b). As shown in this figure, the capacitor is periodically charged and discharged between 2/3 Vcc and 1/3 V, respectively. The time during which the capacitor charges from 1/3 V to 2/3 V. is equal to the time the output is high and is given by

$$t_C = 0.69(R_A + R_B)C$$

where RA and R3 are in ohms and C is in farads. Similarly, the time during which the capacitor discharges from 2/3 V to 1/3 V is equal to the time the output is low and is given by

$$t_d = 0.69(R_B)C$$

where RB is in ohms and C is in farads. Thus the total period of the output waveform is

$$T = t_C + t_d = 0.69(R_A + 2R_B)C$$

This, in turn, gives the frequency of oscillation as

$$f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

Above equation indicates that the frequency f_o is independent of the supply voltage V. Often the term duty cycle is used in conjunction with the astable multivibrator . The duty cycle is the ratio of the time t during which the output is high to the total time period T. It is generally expressed as a percentage. In equation form,

$$\% \, duty \, cycle = \frac{t_C}{T} \times 100$$

$$= \frac{R_A + 2R_B}{R_A + 2R_B} \times 100$$

4.4.1 Astable Multivibrator Applications:

Square-wave oscillator: Without reducing $R_A = 0$, the astable multivibrator can be used to produce a square wave output simply by connecting diode D across resistor R_B, as shown in Figure 4-7. The capacitor C charges through R_A and diode D to approximately 2/3 Vcc and discharges through R_B and terminal 7 until the capacitor voltage equals approximately 1/3 Vcc;

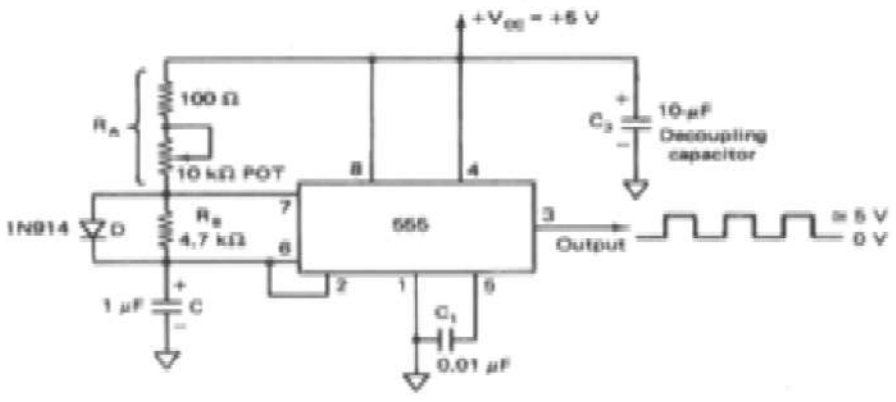


Fig 4-7 Astable Multivibrator as a Square wave generator

then the cycle repeats. To obtain a square wave output (50% duty cycle), R_A must be a combination of a fixed resistor and potentiometer so that the potentiorneter can be adjusted for the exact square wave.

Free-running ramp generator: The asable multivibrator can be used as a free-running ramp generator when resistors R_A and R_3 are replaced by a current mirror. Figure 4-8(a) shows an astable multivibrator configured to perform this function. The current mirror starts charging capacitor C toward V_{cc} at a constant rate.

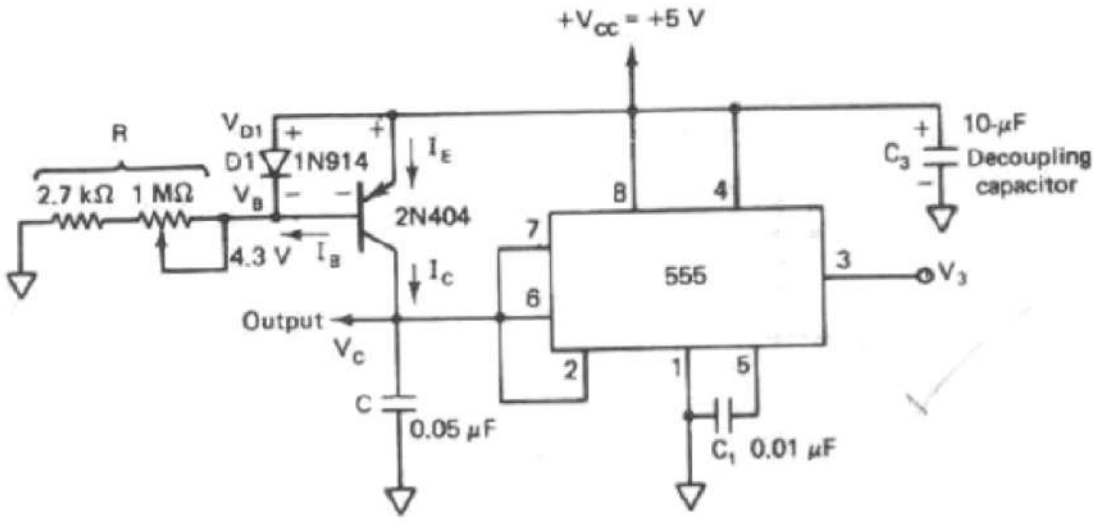
Free-running ramp generator: The asable multivibrator can be used as a free-running ramp generator when resistors R_A and R_3 are replaced by a current mirror. Figure 4-8(a) shows an astable multivibrator configured to perform this function. The current mirror starts charging capacitor C toward V_{cc} at a constant rate.

When voltage across C equals 2/3 V_{cc}, comparator 1 turns transistor Q on, and C rapidly discharges through transistor Q. However, when the discharge voltage across C is approximately equal to 1/3 V_{cc} comparator 2 switches transistor Q off, and then capacitor C starts charging up again. Thus the charge—discharge cycle keeps repeating. The discharging time of the capacitor is relatively negligible compared to its charging time; hence, for all practical purposes, the time period of the ramp waveform is equal to the charging time and is approximately given by

$$T = \frac{V_{cc}C}{3I_C}$$

Where $I = (V_{cc} — V_{BE})/R$ = constant current in amperes and C is in farads. Therefore, the freerunningfrequency of the ramp generator is

$$f_o = \frac{3I_C}{V_{cc}C}$$



(a)

IC565 PLL:

Today the phase-locked loop is even available as a single package, typical examples of which include the Signetics SE/NE 560 series (the 560, 561, 562, 564, 565, and 567). However, for more economical operation, discrete ICs can be used to construct a phase-locked loop.

4.6 PHASE-LOCKED LOOPS

4.6.2 Bloch Schematic and Operating Principle

Figure 4-10 shows the phase-locked loop (PLL) in its basic form. As illustrated in this figure, the phase-locked loop consists of (1) a phase detector, (2) a low-pass filter, and, (3) a voltage controlled oscillator.

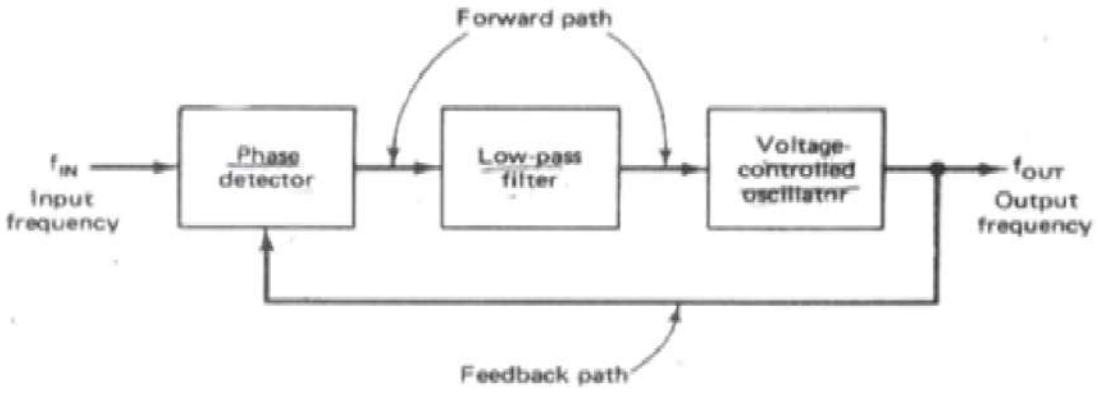


Fig 4-10 Block Diagram of Phase Locked Loop

The phase detectors or comparator compares the input frequency f_{IN} with the feedback frequency f_{OUT}. The output voltage of the phase detector is a dc voltage and therefore is often referred to as the error voltage. The output of the phase is then applied to the low-pass filter, which removes the high-frequency noise and produces a dc level.

This dc level, in turn, is the input to the voltage-controlled oscillator (VCO). The filter also helps in establishing the dynamic characteristics of the PLL circuit. The output frequency of the VCO is directly proportional to the input dc level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies. In short, the phase-locked loop goes through three states: free-running, capture, and phase lock.

Before the input is applied, the phase-locked loop is in the free-running state. Once the input frequency is applied, the VCO frequency starts to change and the phase-locked loop is said to be in the capture mode. The VCO frequency continues to change until it equals the input frequency, and the phase-locked loop is then in the phase-locked state. When phase locked, the loop tracks any change in the input frequency through its repetitive action.

Before studying the specialized phase-locked-loop IC, we shall consider the discrete phaselocked

loop, which may be assembled by combining a phase detector, a low-pass filter, and a voltage-controlled oscillator.

(a) Phase detector:

The phase detector compares the input frequency and the VCO frequency and generates a voltage that is proportional to the phase difference between the two frequencies. Depending on the analog digital phase detector used, the PLL is either called an analog or digital type, respectively. Even though most of the monolithic PLL integrated circuits use analog phase detectors, the majority of discrete phase detectors in use are of the digital type mainly because of its simplicity.

A double-balanced mixer is a classic example of an analog phase detector. On the other hand,examples of digital phase detectors are these:

1. Exclusive-OR phase detector
2. Edge-triggered phase detector
3. Monolithic phase detector (such as type 4044)

The following fig 4.11 shows Exclusive-OR phase detector:

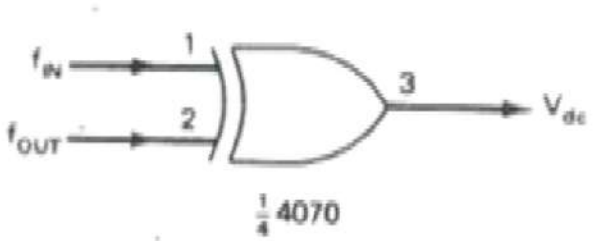
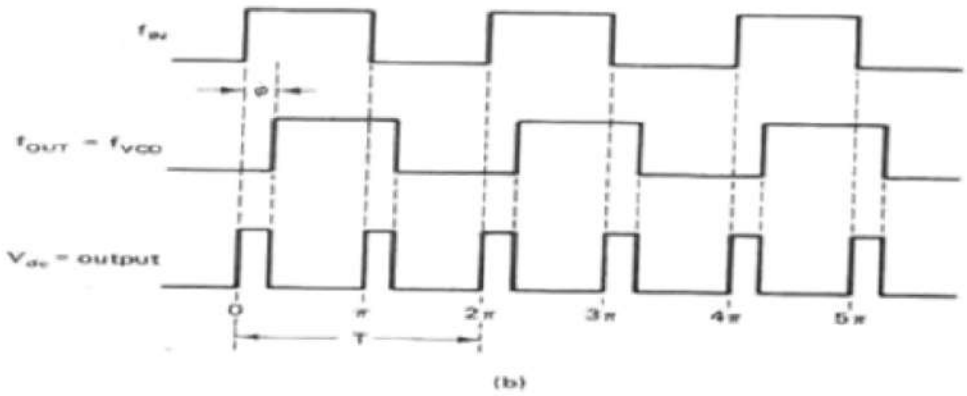


Fig (a)



(b)

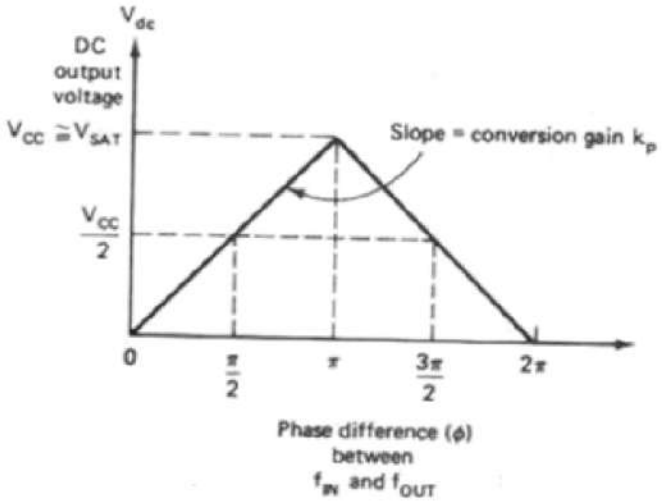


Fig (c)

Fig 4-11(a) Exclusive-OR phase detector: connection and logic diagram. (b) Input and output waveforms. (c) Average output voltage versus phase difference between f_{IN} and f_{OUT} curve.

(b) Low-pass filter.

The second block shown in the PLL block diagram of Figure 4-10 is a low-pass filter. The function of the low-pass filter is to remove the high-frequency components in the output of the phase detector and to remove high-frequency noise.

More important, the low-pass filter controls the dynamic characteristics of the phase-locked loop. These characteristics include capture and lock ranges, bandwidth, and transient response. The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency

f_{IN}. An equivalent term for lock range is tracking range. On the other hand, the capture range is the frequency range in which the PLL acquires phase lock. Obviously, the capture range is always smaller than the lock range.

(c) Voltage-controlled oscillator:

A third section of the PLL is the voltage-controlled oscillator.The VCO generates an output frequency that is directly proportional to its input voltage.Typical example of VCO is Signetics NE/SE 566 VCO, which provides simultaneous square wave and triangular wave outputs as a function of input voltage. The block diagram of the VCO is shown in Fig 4.12. The frequency of oscillations is determined by thee external R_1 and capacitor C_1 and the voltage V_C applied to the control terminal 5. The triangular wave is generated by alternatively charging the external capacitor C_1 by one current source and then linearly discharging it by another. The charging and discharging levels are determined by Schmitt trigger action. The schmitt trigger also provides square wave output. Both the wave forms are buffered so that the output impedance of each is 50 ohms.

Fig 4.12 (c) is a typical connection diagram. In this arrangement the R_1C_1 combination determines the free running frequency and the control voltage V_C at pin 5 is set by voltage divider formed with R_2 and R_3. The initial voltage V_C at pin 5 must be in the range

$$\frac{3}{4}(+V) \leq V_C \leq +V$$

Where +V is the total supply voltage.The modulating signal is ac coupled with the capacitor C and must be <3 V_{PP}. The frequency of the output wave forms is approximated by

$$f_O \cong \frac{2(+V - V_C)}{R_1 C_1 (+V)}$$

where R_1should be in the range $2K\Omega < R_1 < 20K\Omega$. For affixed VC and constant C_1, the frequency fO can be varied over a 10:1 frequency range by the choice of R1 between $2K\Omega < R_1 < 20K\Omega$.

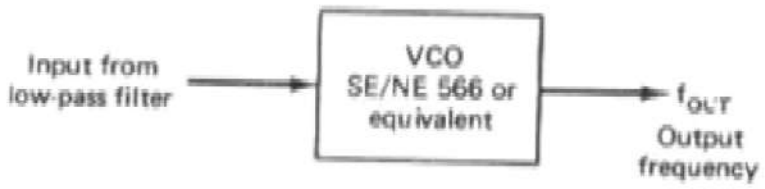


Fig 4.12 VCO Block Diagram

4.7 MONOLITHIC PHASE LOCK LOOPS IC 565:

Monolithic PLLs are introduced by signetics as SE/NE 560 series and by national semiconductors LM 560 series.

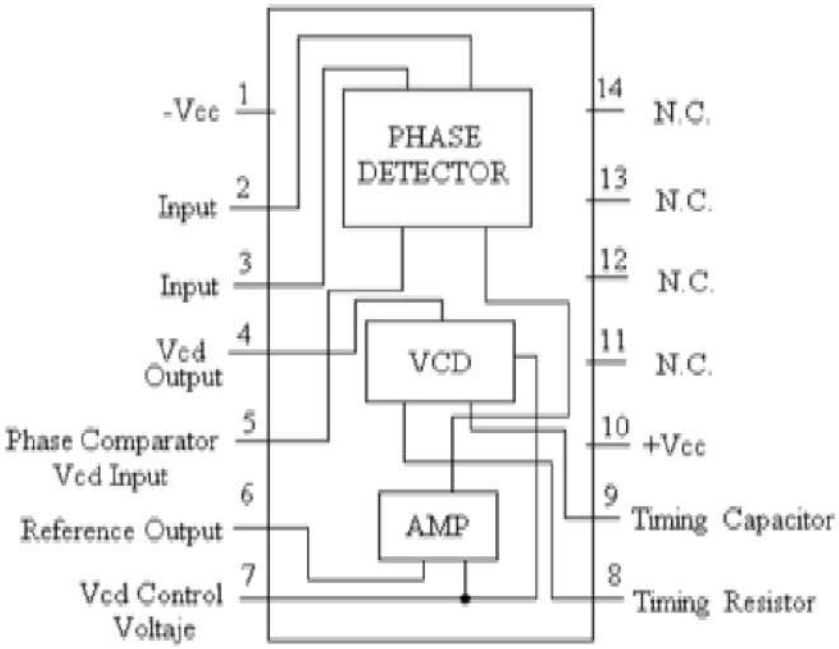


Fig 4.13 Pin configuration of IC 565

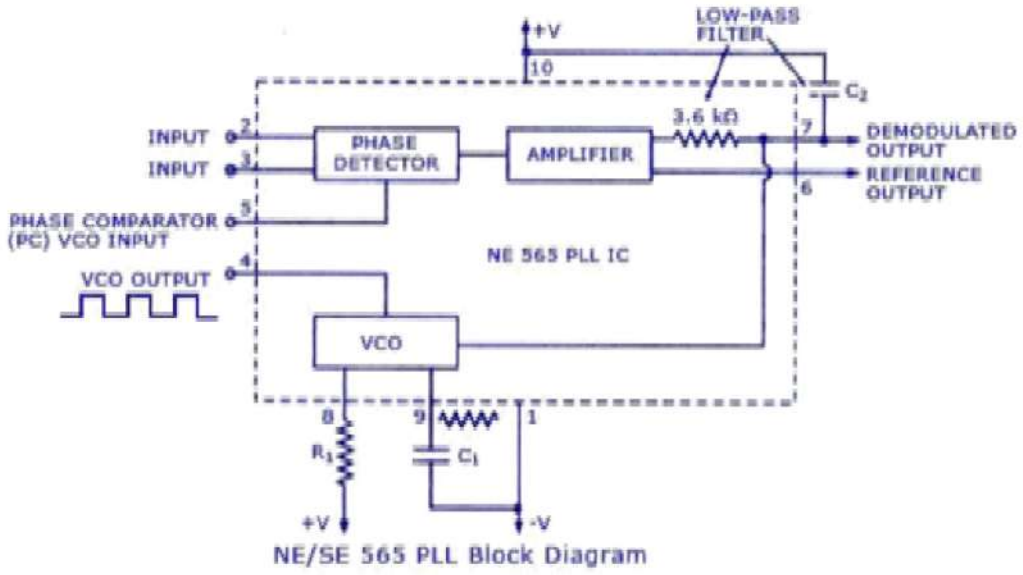


Fig 4.14 Block Diagram of IC 565

Fig 4.13 and 4.14 shows the pin diagram and block diagram of IC 565 PLL. It consists of phase detector,amplifier,low pass filter and VCO.As shown in the block diagram the phase locked feedback loop is not internally connected.Therefore,it is necessary to connect out put of VCO to the phase comparator input,externally.In frequency multiplication applications a digital frequency divider is inserted into the loop i.e between pin 4 and pin 5.

The centre frequency of the PLL is determined by the free-running frequency of the VCO and it is given by

$$f_o = \frac{1.2}{4R_1C_1}$$

Where R_1 and C_1 are an external resistor and capacitor connected to pins 8 and 9, respectively.The values of R_1 and C_1 are adjusted such that the free running frequency will be at the centre of the input frequency range.The values of R_1 are restricted from 2 kΩ to 20 kΩ,but a capacitor can have any value.A capacitor C_2 connected between pin 7 and the positive supply forms a first order low pass filter with an internal resistance of 3.6 kΩ.The value of filter capacitor C_2 should be larger enough to eliminate possible demodulated output voltage at pin 7 in order to stabilize the VCO frequency

The PLL can lock to and track an input signal over typically ±60% bandwidth w.r.t f_o as the center frequency. The lock range f_L and the capture range f_C of the PLL are given by the following equations.

$$f_L = \pm \frac{8 f_o}{V}$$

Where fo=free running frequency

V=(+V)-(-V)Volts

And

$$f_C = \pm \sqrt{\frac{f_L}{2\pi(3.6)10^3 C_2}}$$

From above equation the lock range increases with an increase in input voltage but decrease with increase in supply voltage.The two inputs to the phase detector allows direct coupling of an input signal,provided that there is no dc voltage difference between the pins and the dc resistances seen from pins 2 and 3 are equal.

Applications of PLL:

- FM demodulation networks for FM operations.
- It is used in motor speed controls and tracking filter.
- It is used in frequency shifting decodes for demodulation carrier frequencies.
- It is used in time to digital converters.
- It is used for Jitter reduction, skew suppression, clock recovery.

UNIT-III

DATA CONVERTERS

5.1 INTRODUCTION

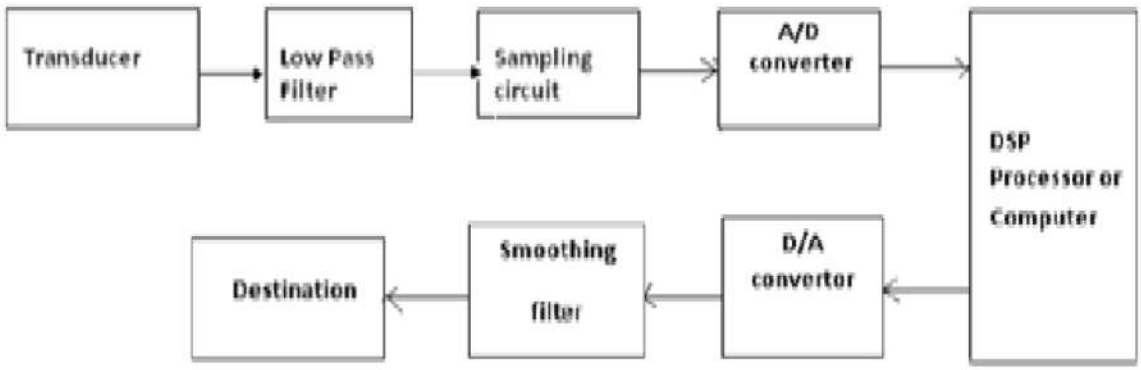


Fig 5.1 shows the application of A/D and D/A converters.

The transducer circuit will gives an analog signal. This signal is transmitted through the LPF circuit to avoid higher components, and then the signal is sampled at twice the frequency of the signal to avoid the overlapping. The output of the sampling circuit is applied to A/D converter where the samples are converted into binary data i.e. 0's and 1's. Like this the analog data converted into digital data.

The digital data is again reconverted back into analog by doing exact opposite operation of first half of the diagram. Then the output of the D/A convertor is transmitted through the smoothing filter to avoid the ripples.

5.2 BASIC DAC TECHNIQUES

The input of the block diagram is binary data i.e, 0 and 1,it contain 'n' number of input bits designated as $d_1, d_2, d_3, \ldots d_n$ .this input is combined with the reference voltage called V_{dd} to give an analog output.

Where d1 is the MSB bit and d_n is the LSB bit

$Vo=V_{dd}(d_1*2^{-1}+d_2*2^{-2}+d_3*2^{-3}+\ldots\ldots\ldots\ldots\ldots\ldots+d_n*2^{-n})$

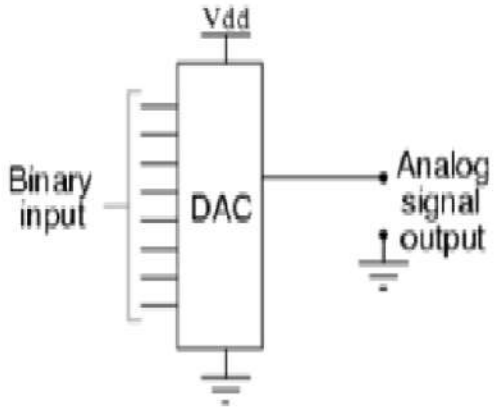


Fig 5.2: Basic DAC diagram

5.2.1 Weighted Resistor:

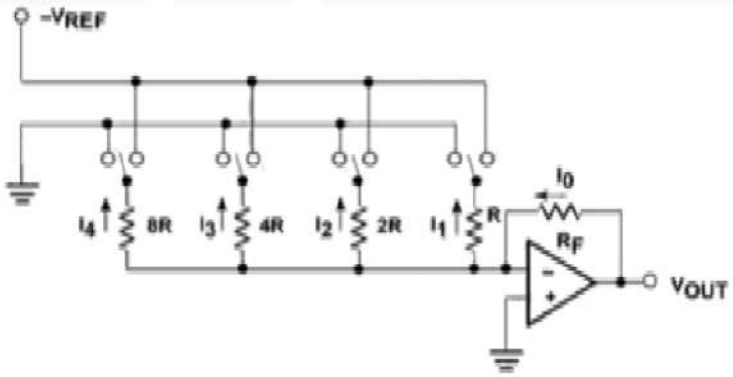


Fig: 5.3 simple 4-bit weighted resistor

Fig. 5.3 shows a simplest circuit of weighted resistor. It uses a summing inverting amplifier. It contains n-electronic switches (i.e. 4 switches) and these switches are controlled by binary input bits d1, d2, d3, d4. If the binary input bit is 1 then the switch is connected to reference voltage $-V_{REF}$, if the binary input bit is 0 then the switch is connected to ground.

The output current equation is

$$I_o = I_1 + I_2 + I_3 + I_4$$

$$I_o = V_{REF}\,(d_1 * 2^{-1} + d_2 * 2^{-2} + d_3 * 2^{-3} + d_4 * 2^{-4})$$

The transfer characteristics are shown below (fig 5.4) for a 3-bit weighted resistor

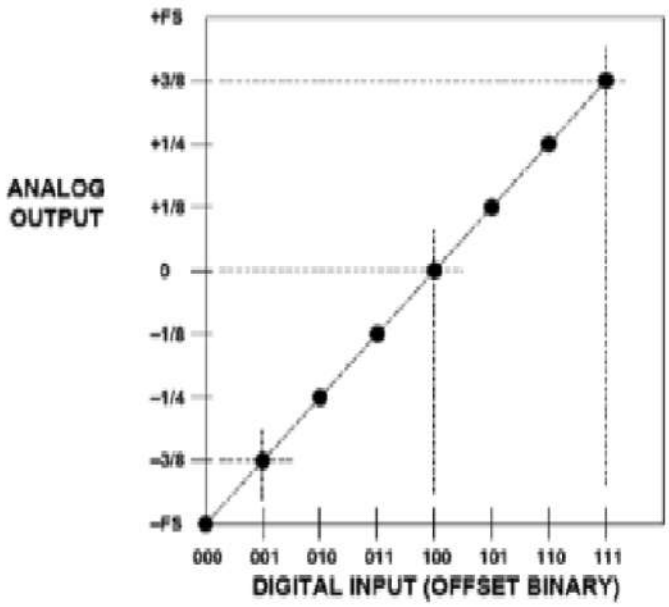


Fig 5.4 Transfer characteristics of 3-bit weighted resistor

Disadvantages of Weighted resistor D/A converter:

Wide range of resistor's are required in this circuit and it is very difficult to fabricate such a wide range of resistance values in monolithic IC. This difficulty can be eliminated using R-2R ladder network.

5.2.2 R-2R LADDER DAC

Wide range of resistors required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC. The circuit of R-2R ladder network is shown in fig 5.5. The basic theory of the R-2R ladder network is that current flowing through any input resistor (2R) encounters two possible paths at the far end. The effective resistances of both paths are the same (also 2R), so the incoming current splits equally along both paths. The half-current that flows back towards lower orders of magnitude does not reach the op amp, and therefore has no effect on the output voltage. The half that takes the path towards the op amp along

the ladder can affect the output. The inverting input of the op-amp is at virtual earth. Current flowing in the elements of the ladder network is therefore unaffected by switch positions.

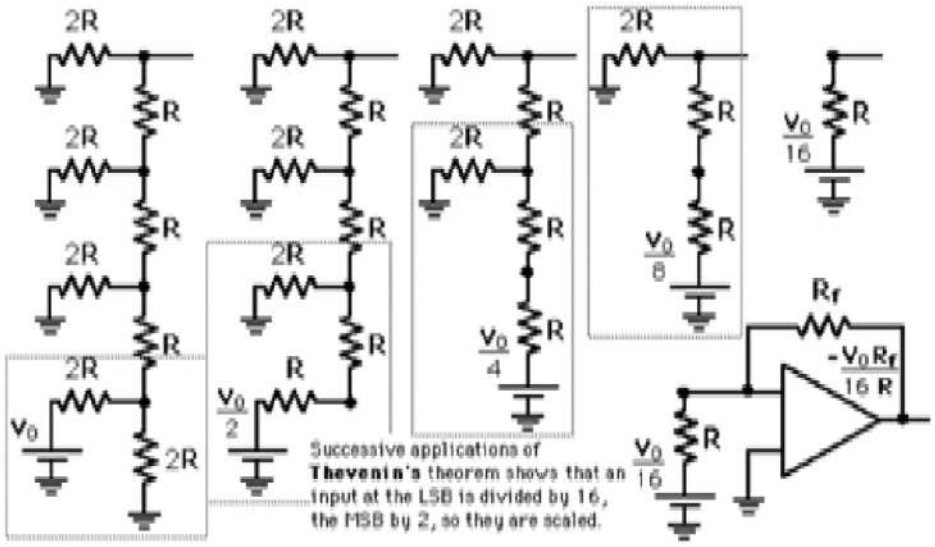


Fig 5.5: A 4-bit R-2R Ladder DAC

If we label the bits (or inputs) bit 1 to bit N the output voltage caused by connecting a particular bit to Vr with all other bits grounded is:

Vout = Vr/2N

where N is the bit number. For bit 1, Vout =Vr/2, for bit 2, Vout = Vr/4 etc.

Since an R/2R ladder is a linear circuit, we can apply the principle of superposition to calculate Vout. The expected output voltage is calculated by summing the effect of all bits connected to Vr. For example, if bits 1 and 3 are connected to Vr with all other inputs grounded, the output voltage is calculated by:

Vout = (Vr/2)+(Vr/8) which reduces to Vout = 5Vr/8.

An R/2R ladder of 4 bits would have a full-scale output voltage of 1/2 +1/4 + 1/8 + 1/16 = 15Vr/16 or 0.9375 volts (if Vr=1 volt) while a 10bit R/2R ladder would have a full-scale output voltage of 0.99902 (if Vr=1 volt).

NOTE:

The number of resistors required for an N-bit D/A converter is 2N in case of R-2R ladder D/A converter

whereas it is only N in the case of weighted resistor D/A converter.

5.2.3 INVERTED R-2R LADDER DAC

In weighted resistor and R-2R ladder DAC the current flowing through the resistor is always changed because of the changing input binary bits 0 and 1. More power dissipation causes heating, which in turn cerates non-linearity in DAC. This problem can be avoided by using INVERTED R-2R LADDER DAC (fig 5.6)

In this MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of op-amp which is also at virtual ground. When the input binary in logic 1 then it is connected to the virtual ground, when input binary is logic 0 then it is connected to the ground i.e. the current flowing through the resistor is constant.

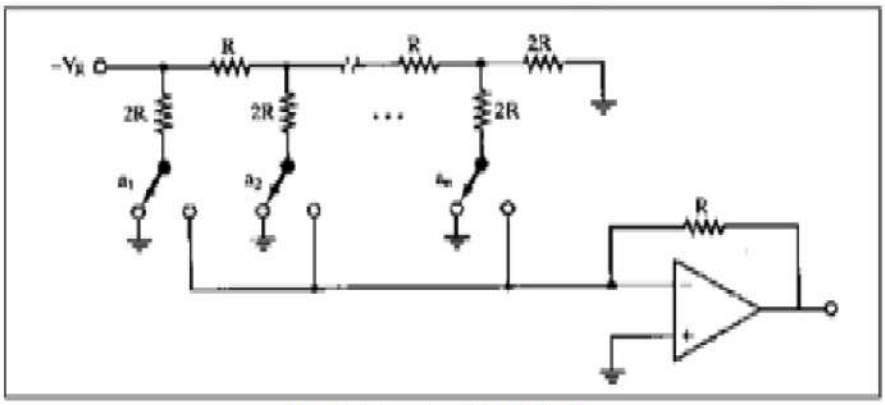


Fig 5.6: Inverted R-2R ladder

5.3 DIFFERENT TYPES OF ADC'S

It provides the function just opposite to that of a DAC. It accepts an analog input voltage Va and produces an output binary word $d_1,d_2,d_3\ldots.d_n$ Where d_1 is the most significant bit and d_n is the least significant bit.

ADCs are broadly classified into two groups according to their conversion techniques

1) Direct type

2) Integrating type

Direct type ADCs compares a given analog signal with the internally generated equivalent signal. This group includes

i) Flash (Comparator) type converter
ii) Successive approximation type convertor
iii) Counter type
iv) Servo or Tracking type

Integrated type ADCs perform conversion in an indirect manner by first changing the analog input signal to linear function of time or frequency and then to a digital code

i) Dual slope ADC

5.3.1 FLASH (COMPARATOR) TYPE CONVERTER:

A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, $2^N - 1$, doubles with each additional bit, requiring a large, expensive circuit. ADCs of this type have a large die size, a high input capacitance, high power dissipation, and are prone to produce glitches at the output (by outputting an out-of-sequence code). Scaling to newer submicrometre technologies does not help as the device mismatch is the dominant design limitation. They are often used for video, wideband communications or other fast signals in optical storage.

A Flash ADC (also known as a direct conversion ADC) is a type of analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are constructed of many resistors; however modern implementations show that capacitive voltage division is also possible. The output of these comparators is generally fed into a digital encoder which converts the inputs into a binary value (the collected outputs from the comparators can be thought of as a unary value).

Also called the *parallel* A/D converter, this circuit is the simplest to understand. It is formed of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output.

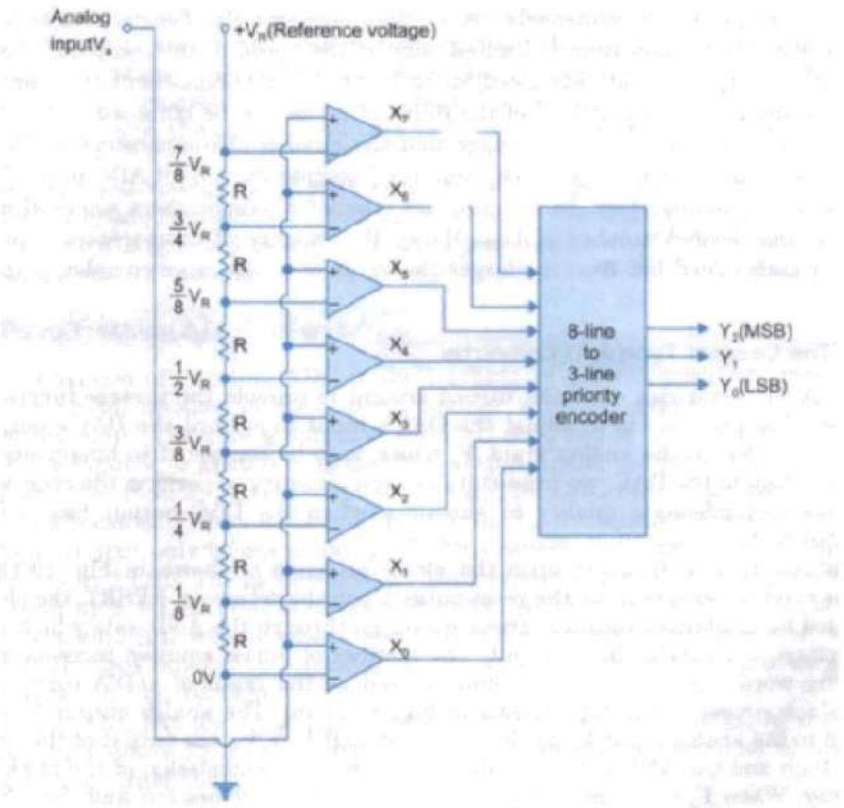


Fig-5.7: flash (parallel comparator) type ADC

The following (fig-5.7) illustration shows a 3-bit flashADC circuit:

V_R is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit, not shown in the schematic. As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state. The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.

5.3.2 COUNTER TYPE A/D CONVERTER

In the fig-5.8 the counter is reset to zero count by reset pulse. After releasing the reset pulse the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with

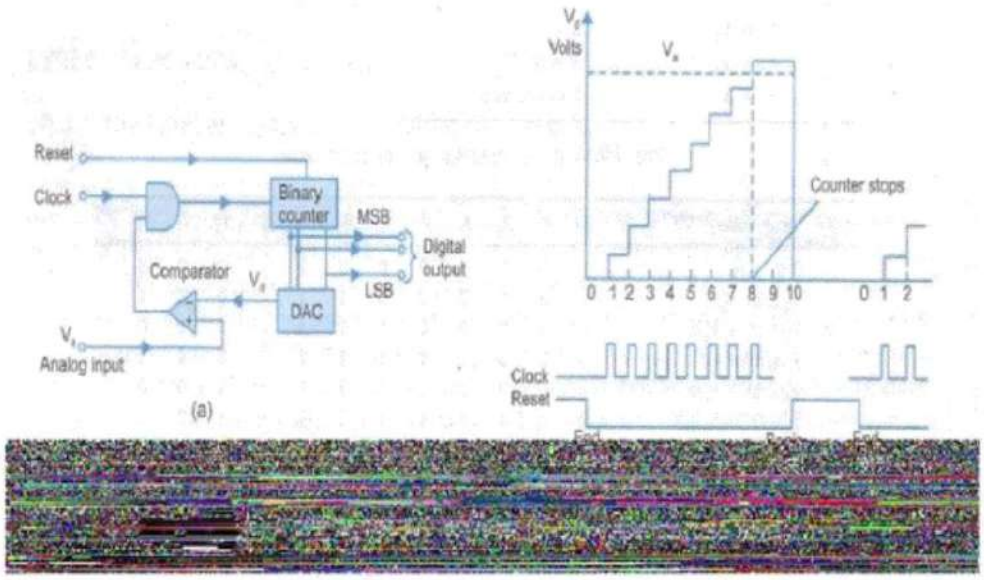


Fig-5.8 Countertype A/D converter

time. The binary word representing this count is used as the input of a D/A converter whose output is a stair case. The analog output Vd of DAC is compared to the analog input input Va by the comparator. If Va>Vd the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When Va<Vd the output of the comparator becomes low and the AND gate is disabled.This stops the counting we can get the digital data.

5.3.3 SERVO TRACKING A/D CONVERTER

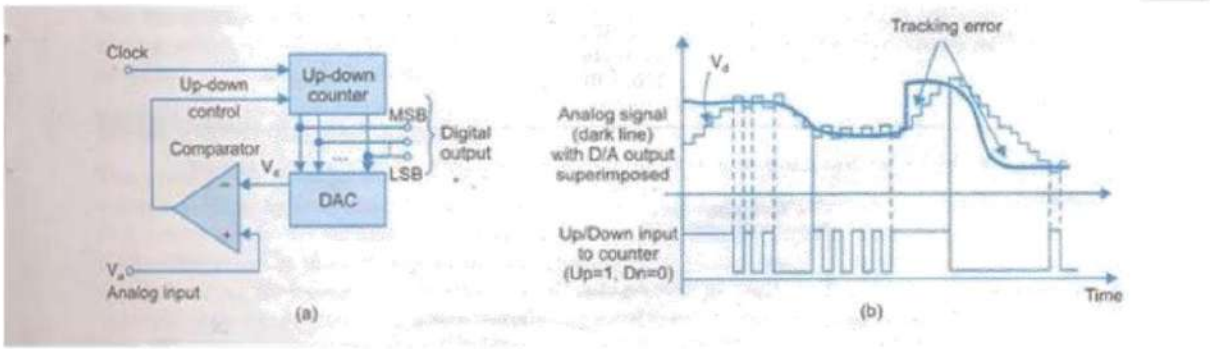


Fig: 5.9 A tracking A/D converter (b) waveforms associated with a tracking A/D converter

An improved version of counting ADC is the tracking or servo converter shown in fig 5.9. The circuit consists of an up/down counter with the comparator controlling the direction of the count. The analog output of the DAC is Vd and is compared with the analog input Va.If the input Va is greater than the DAC output signal, the output of the comparator goes high and the counter is

caused to count up. The DAC output increases with each incoming clock pulse when it becomes more than Va the counter reverses the direction and counts down.

5.3.4 SUCCESSIVE-APPROXIMATION ADC:

One method of addressing the digital ramp ADC's shortcomings is the so-called *successive-approximation*ADC. The only change in this design as shown in the fig 5.10 is a very special counter circuit known as a *successive-approximation register*. Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the most-significant bit and finishing at the least-significant bit. Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly. The way the register counts is identical to the "trial-and-fit" method of decimal-to-binary conversion, whereby different values of bits are tried from MSB to LSB to get a binary number that equals the original decimal number. The advantage to this counting strategy is much faster results: the DAC output converges on the analog signal input in much larger steps than with the 0-to-full count sequence of a regular counter.

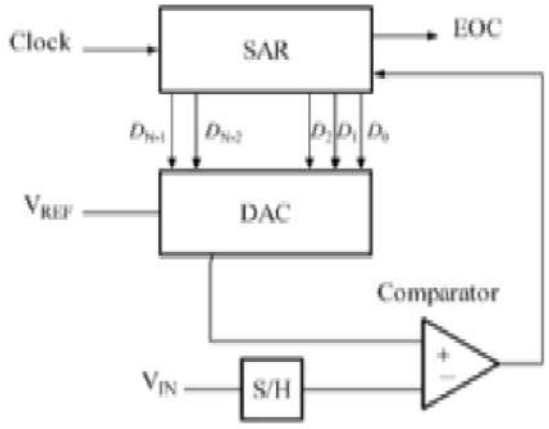


Fig: 5.10 successive approximation ADC

The successive approximation analog to digital converter circuit typically consists of four chief sub circuits:

1. A sample and hold circuit to acquire the input voltage (V_{in}).
2. An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR).
3. A successive approximation register sub circuit designed to supply an approximate digital

code of V_{in} to the internal DAC.

4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with V_{in}.

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

Mathematically, let $V_{in} = xV_{ref}$, so x in [-1, 1] is the normalized input voltage. The objective is to approximately digitize x to an accuracy of $1/2^n$. The algorithm proceeds as follows:

1. Initial approximation $x_0 = 0$.
2. ith approximation $x_i = x_{i-1} - s(x_{i-1} - x)/2^i$.

where, s(x) is the signum-function(sgn(x)) (+1 for $x \geq 0$, -1 for $x < 0$). It follows using mathematical induction that $|x_n - x| \leq 1/2^n$.

As shown in the above algorithm, a SAR ADC requires:

1. An input voltage source V_{in}.
2. A reference voltage source V_{ref} to normalize the input.
3. A DAC to convert the ith approximation x_i to a voltage.
4. A Comparator to perform the function $s(x_i - x)$ by comparing the DAC's voltage with the input voltage.
5. A Register to store the output of the comparator and apply $x_{i-1} - s(x_{i-1} - x)/2^i$.

A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved. At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR). The SAR uses a reference voltage (which is the largest signalthe ADC is to convert) for comparisons. For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V iscompared to 50 V (the reference,divided by two. This is the

voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V). At this point the first binary digit (MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V (halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros). The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for '1001' followed by zeros). The result of this would be in the binary form 1001. This is also called *bit-weighting conversion*, and is similar to a binary search. The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired. The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required. ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.

5.3.5 DUAL-SLOPE ADC

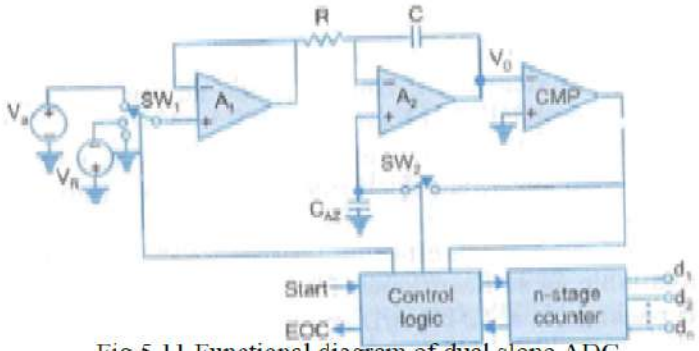


Fig 5.11 Functional diagram of dual slope ADC

An integrating ADC (also **dual-slope**ADC) shown in fig 5.11a applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measuredrun-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher

resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of t type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.

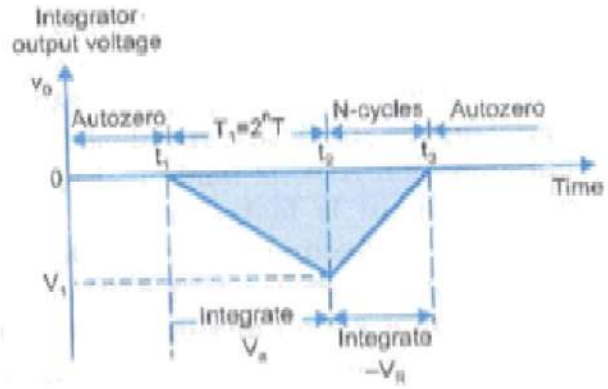


Fig 5.11b o/p waveform of dual slope ADC

In operation the integrator is first zeroed (close SW2), then attached to the input (SW1 up) for a fixed time *M* counts of theclock (frequency 1/*t*). At the end of that time it is attached to the reference voltage (SW1 dow and the number of counts *N*which accumulate before the integrator reaches zero volts output and t comparator output changes are determined. The waveform of dual slope ADC is shown in fig 5.11b.

The equations of operation are therefore:

$$T_1 = t_2 - t_1 = \frac{2^n\ counts}{clock\ rate}$$

And

$$t_3 - t_2 = \frac{digitalcount N}{clockrate}$$

For an integrator,

$$\Delta V_O = \frac{-1}{RC} V(\Delta t)$$

The voltage Vo will be equal to V_1 at the instant t_2 and can be written as

$$V_1 = \frac{-1}{RC} V_a (t_2 - t_1)$$

The voltage V_1 is also given by

$$V_1 = \frac{-1}{RC} (-V_R)(t_2 - t_3)$$

So,

$$V_a (t_2 - t_1) = (V_R)(t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$, we get

$$V_a(2^n) = (V_R)N$$

Or,

$$V_a = (V_R)\left(\frac{N}{2^n}\right)$$

5.4 SPECIFICATIONS FOR DAC/ADC

1. RESOLUTION: The Resolution of a converter is the smallest change in voltage which may be produced at the output of the converter.

Resolution (in volts)=(V_{FS})/(2^n-1)= 1 LSB increment

Ex: an 8-bit D/A converter have 2^8-1=255 equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range.

An 8-bit DAC is said to have: 8 bit resolution

: a resolution of 0.392 of full scale

: a resolution of 1 part in 255

Similarly the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output.

Ex: the input range of 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10V input range is 39.22 mV(=10V/255)

2. LINEARITY: The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal characteristics.

3. GLITCHES (PARTICULARLY DAC): In transition from one digital input to the next, like 0111 to 1000, it may effectively go through 1111 or 0000, which produces —unexpectedl voltage briefly. If can cause problems elsewhere.

4. ACCURACY: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.

5. MONOTONIC: A monotonic DAC is the one whose analog output increases for an increase in digital input. It is essential in control applications. If a DAC has to be monotonic, the error should de lessthan ±(1/2) LSB at each output level.

6. SETTLING TIME: The most important dynamic parameter is the settling time. It represents

the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input. It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Its ranges from 100ns to 10μs.

STABILITY: The performance of converter changes with temperature, age and power supply variations. So the stability is required.

UNIT-IV

DIGITAL INTEGRATED CIRCUITS

Classification of Integrated Circuits

1.1 CLASSIFICATION OF IC'S:

Integrated Circuitis a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon.

CLASSIFICATION:

1.1.1 Based on mode of operation

a. Digital IC's
b. Linear IC's

Digital IC's: Digital IC's are complete functioning logic networks that are equivalents of basic transistor logic circuits.
Ex:- gates ,counters, multiplexers, demultiplexers, shift registers.

Linear IC's: Linear IC's are equivalents of discrete transistor networks, such as amplifiers, filters, frequency multipliers, and modulators that often require additional external components for satisfactory operation

1.1.2. Based on fabrication

a. Monolithic IC's
b. Hybrid IC's

a. **Monolithic IC's** : In monolithic ICs all components (active and passive) are forme simultaneously by a diffusion process. Then a metallization process is used i interconnecting these components to form the desired circuit.
b. **Hybrid IC's:** .In hybrid ICs, passive components (such as resistors and capacitors) and tl interconnections between them are formed on an insulating substrate. The substrate is use as a chassis for the integrated components. Active components such as transistors and diode as wellas monolithic integrated circuits, are then connected to form a complete circuit.

1.1.3. Based on number of components integrated on IC's

a. SSI <10 components
b. MSI <100 components
c. LSI >100 components
d. VLSI >1000 components

1.2. CHIP SIZE AND CIRCUIT COMPLEXITY:

Invention of transistor	1948
Development of silicon transistor	1955-1959
Silicon planar technology	1959
First IC,Small Scale Integration(SSI),3 to 30 gates/chip	1960
Medium Scale Integration (MSI),30 to 300 gates/chip	1965-1970
Large Scale Integration(LSI),300 to 3000 gates/chip	1970-1975
Very Large Scale Integration(VLSI) more than 3000 gates/chip	1975

An integrated circuit or monolithic integrated circuit (also referred to as IC, chip, or microchip) is an electronic circuit. Integrated circuits are used in virtually all electronic equipment today and have revolutionized the world of electronics. Computers, cell phones, and other digital appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of production of integrated circuits. There are two main advantages of ICs over discrete circuits: cost and performance. Cost is low because the chips, with all their components, are printed as a unit by photolithography rather than being constructed one transistor at a time. Furthermore, much less material is used to construct a packaged IC die than to construct a discrete circuit.

Performance is high because the components switch quickly and consume little power (compared to their discrete counterparts) as a result of the small size and close proximity of the components.

6.2 CLASSIFICATION OF INTEGRATED CIRCUITS

Classification of ICs based on complexity:

- Small Scale Integration or (SSI) - Contain up to 10 transistors or a few gates within a single package such as AND, OR, NOT gates.
- Medium Scale Integration or (MSI) - between 10 and 100 transistors or tens of gates within a single package and perform digital operations such as adders, decoders, counters, flip-flops and multiplexers.
- Large Scale Integration or (LSI) - between 100 and 1,000 transistors or hundreds of gates and perform specific digital operations such as I/O chips, memory, arithmetic and logic units.
- Very-Large Scale Integration or (VLSI) - between 1,000 and 10,000 transistors or thousands of gates and perform computational operations such as processors, large memory arrays and programmable logic devices.
- Super-Large Scale Integration or (SLSI) - between 10,000 and 100,000 transistors within a single package and perform computational operations such as microprocessor chips, micro-controllers, basic PICs and calculators.
- Ultra-Large Scale Integration or (ULSI) - more than 1 million transistors - the big boys that are used in computers CPUs, GPUs, video processors, micro-controllers, FPGAs and complex PICs.

While the "ultra large scale" ULSI classification is less well used, another level of integration which represents the complexity of the Integrated Circuit is known as the **System-on-Chip** or (**SOC**) for short. Here the individual components such as the microprocessor, memory, peripherals, I/O logic etc, are all produced on a single piece of silicon and which represents a whole electronic system within one single chip, literally putting the word "integrated" into integrated circuit. These chips are generally used in mobile phones, digital cameras, micro-controllers, PICs and robotic applications, and which can contain up to 100 million individual silicon-CMOS transistor gates within one single package.

Classification of integrated circuits based on the signal processed:

- DIGITAL INTEGRATED CIRCUITS

Digital integrated circuits, primarily used to build computer systems, also occur in cellular phones, stereos and televisions. Digital integrated circuits include microprocessors, microcontrollers and logic circuits. They perform mathematical calculations, direct the flow of data and make decisions based on Boolean logic principles.The Boolean system used centers on on two numbers: 0 and 1.

- ANALOG INTEGRATED CIRCUITS

Analog integrated circuits most commonly make up a part of power supplies, instruments and communications. In these applications, analog integrated circuits amplify, filter and modify electrical signals. In cellular phones, they amplify and filter the incoming signal from the phone's antenna. The sound encoded into that signal has a low amplitude level; after the circuit filters the sound signal from the incoming signal, the circuit amplifies the sound signal and sends it to the speaker in your cell phone, allowing you to hear the voice on the other end.

- MIXED-SIGNAL INTEGRATED CIRCUITS

Mixed-signal circuits occur in cellular phones, instrumentation, motor and industrial control applications. These circuits convert digital signals to analog signals, which in turn set the speed of motors, the brightness of lights and the temperature of heaters, for example. They also convert digital signals to sound waveforms, allowing for the design of digital musical instruments such as electronic organs and computer keyboards capable of playing music.

Mixed-signal integrated circuits also convert analog signals to digital signals. They will convert analog voltage levels to digital number representations of the voltage level of the signals. Digital integrated circuits then perform mathematical calculations on these numbers.

- MEMORY-INTEGRATED CIRCUITS

Though primarily used in computer systems, memory-integrated circuits also occur in cellular phones, stereos and televisions. A computer system may include 20 to 40 memory chips, while other types of electronic systems may contain just a few.

Memory circuits store information, or data, as two numbers: 0 and 1. Digital integrated circuits will often retrieve these numbers from memory and perform calculations with them, then save the calculation result a memory chip's data storage locations. The more data it accesses---pictures, sound and text---the more memory an electronic system will require.

Combinational Logic ICs – Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs

7400 Series TTL: The 7400 series TTL logic integrated circuits provided the basis for most of the logic circuits of the time and they are still available today.

The 7400 series of TTL logic integrated circuits was introduced in October 1966. The 7400 series logic TTL chips spawned a series of other derivative logic families offering slightly different characteristics: high speed, low power, etc. However the standard parameters remained the same: logic function (a 7416 and a 74LS16 had the same function; they were pin compatible, etc.

The 7400 series TTL chips remained in use for many years. They have long been superseded by other 74xx00 logic families, but they have been so successful that the basic concept has remained the same.

7400 series main features

Some of the main or highlight features and specifications for the 7400 series logic family are detailed below:

Summary of 7400 Series TTL Key Parameters

Parameter	Specification
Supply voltage	Nominal 5V (4.75 - 5.25)
Max toggle speed	25 MHz
Propagation delay per gate	Typically 10 ns
Power consumption per gate	10 mW

7400 series output stages

There are three types of output stage that 7400 series logic may possess.

- ***Totem pole:*** This output is the standard output format for 7400 series logic chips. It comprises two transistors and enables very fast switching times to be achieved.

The advantages of using the totem-pole output are threefold:

- Low power consumption
- Fast switching
- Low output impedance

The **4000 series** is a range of **CMOS ICs** introduced as a lower-power and more versatile alternative to the 7400 **series** in common use. There are many **ICs** in the **4000 series**, from simple logic gates to counters and many more.

General characteristics of 4000 series CMOS ICs

- **Supply:** 3 to 15V, small fluctuations are tolerated.
- **Inputs** have very high impedance (resistance), this is good because it means they will not affect the part of the circuit where they are connected. However, it also means that unconnected inputs can easily pick up electrical noise and rapidly change between high and low states in an unpredictable way. This is likely to make the IC behave erratically and it will significantly increase the supply current. To prevent problems **all unused inputs MUST be connected to the supply (either +Vs or 0V)**, this applies even if that part of the IC is not being used in the circuit!
- **Outputs** can sink and source only about 1mA if you wish to maintain the correct output voltage to drive CMOS inputs. If there is no need to drive any inputs the maximum current is about 5mA with a 6V supply, or 10mA with a 9V supply (just enough to light an LED). To switch larger currents you can connect a transistor.
- **Fan-out:** one output can drive up to 50 inputs.
- **Gate propagation time**: typically 30ns for a signal to travel through a gate with a 9V supply, it takes a longer time at lower supply voltages.
- **Frequency**: up to 1MHz, above that the 74 series is a better choice.
- **Power consumption** (of the IC itself) is very low, a few µW. It is much greater at high frequencies, a few mW at 1MHz for example.

Quad 2-input gates

- 4001 quad 2-input NOR
- 4011 quad 2-input NAND
- 4030 quad 2-input EX-OR (now obsolete)
- 4070 quad 2-input EX-OR
- 4071 quad 2-input OR
- 4077 quad 2-input EX-NOR
- 4081 quad 2-input AND
- 4093 quad 2-input NAND with Schmitt trigger inputs

The 4093 has Schmitt trigger inputs to provide good noise immunity. They are ideal for slowly changing or noisy signals. The hysteresis is about 0.5V with a 4.5V supply and almost 2V with a 9V supply.

Code Converters:

The Gray Code is unweighted and is not an arithmetic code: that is, there are no specific weights asssigned to the bit positions. The important feature of the Gray Code is that it exhibits only a single bit change from one code word to the next in sequence. This property is important in many applications, such as shaft position encoders, where error susceptibility increases with the number of bit changes between adjacent numbers in a sequence.

To convert a binary number to a Gray Code number, the following rules apply.

1. The most significant digit (Left Most Bit) in the Gray Code is the same as the corresponding digit in the binary number.

2. Going from left to right, add each adjacent pair of binary digits to get the next Gray code digit, regradless carries.

For instance - Let us convert the binary number 1010 to Gray Code.

Step 1 - The left most Gray digit is the same as the left most binary

```
1    0    1    0    Binary
↓
1                   Gray
```

Step 2 - Add the left most binary digit to the adjacent one.

```
1 + 0    1    0    Binary
    ↓
1   1              Gray
```

Step 3 - Add the next adjacent pair

```
1    0  + 1    0    Binary
        ↓
1    1    1         Gray
```

Step 4 -Add the last adjacent pair

```
1    0    1  + 0    Binary
             ↓
1    1    1    1    Gray
```

The conversion is now complete and the Gray Code is 1111.

Steps to design the converter

1. Design a converter by the following procedures:

a. Write down the truth table of both input and output bits of the converter.

b. Apply Karnaugh Map to look for the minimized logic expression for the output bits.

c. Implement the logic gates by using Circuit Maker.

Example:

For Binary to Gray Code Converter, binary bits are input and gray code bits are output. So first write the truth table for binary bits and gray code. Then k-map for the all bits of gray code, find the simplified expression for each bit of gray code. Then design the logical circuit.

Truth Table

Decimal	Binary				Gray			
	A	B	C	D	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

K-Map for each bit of Gray code

For practical consideration code conversions are made for each bit.

(a) For Y_3, the Karnaugh map can draw as follow.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	0	0
$\bar{A}B$	0	0	0	0
AB	1	1	1	1
$A\bar{B}$	1	1	1	1

(a)

By minimization, $Y_3 = A$

(b) For Y_2, the Karnaugh map can draw as f

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	0	0
$\bar{A}B$	1	1	1	1
AB	0	0	0	0
$A\bar{B}$	1	1	1	1

(b)

By minimization, $Y_2 = A \oplus B$

(c) For Y_1, the Karnaugh map can draw as follow.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	1	1
$\bar{A}B$	1	1	0	0
AB	1	1	0	0
$A\bar{B}$	0	0	1	1

(a)

By minimization, $Y_1 = B \oplus C$

(d) For Y_0, the Karnaugh map can draw as follow.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	0	1
$\bar{A}B$	0	1	0	1
AB	0	1	0	1
$A\bar{B}$	0	1	0	1

(b)

By minimization, $Y_0 = C \oplus D$

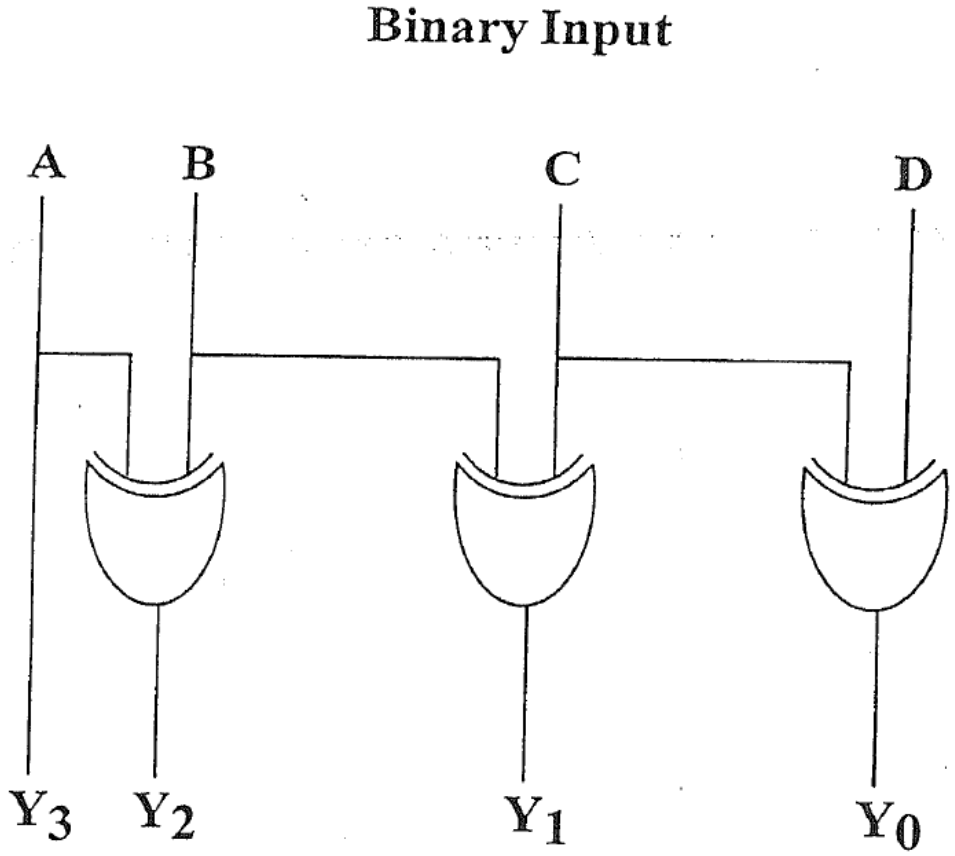
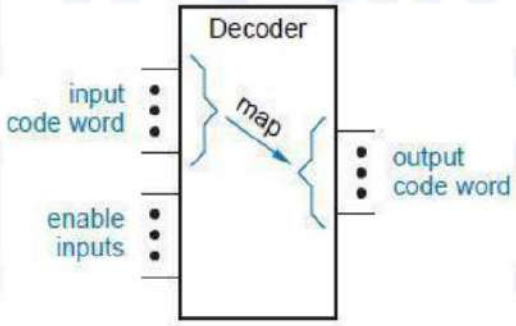


Figure 3.1 Binary-to-Gray Code

Decoders & Encoders

Decoders

A *decoder* is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. The input code generally has fewer bits than the output code, and there is a one-to one mapping from input code words into output code words. In a *one-to-one mapping*, each input code word produces a different output code word.



The general structure of a decoder circuit is shown in Figure 1. The enable inputs, if present, must be asserted for the decoder to perform its normal mapping function. Otherwise, the decoder maps all input code words into a single, "disabled," output code word.

The most commonly used output code is a 1-out-of-m code, which contains m bits, where one bit is asserted at any time. Thus, in a 1-out-of-4 code with active-high outputs, the code words are 0001, 0010, 0100, and 1000. With active-low outputs, the code words are 1110, 1101, 1011, and 0111.

Binary Decoders

The most common decoder circuit is an n-to-$2n$ decoder or *binary decoder*. Such a decoder has an n-bit binary input code and a 1-out-of-$2n$ output code. A binary decoder is used when you need to activate exactly one of $2n$ outputs based on an n-bit input value.

Inputs			*Outputs*			
EN	I1	I0	Y3	Y2	Y1	Y0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Table 1: 2 to 4 decoder

Table 1 is the truth table of a 2-to-4 decoder. The input code word 1,I0 represents an integer in the range 0–3. The output code word Y3,Y2,Y1,Y0 has Y*i* equal to 1 if and only if the input code word is the binary representation of *i* and the *enable input* EN is 1. If EN is 0, then all of the outputs are 0. A gate-level circuit for the 2-to-4 decoder is shown in Figure 2 Each AND gate *decodes* one combination of the input code word I1,I0.

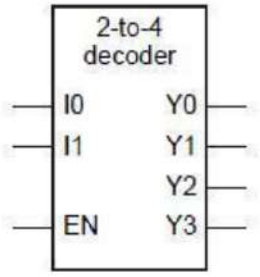


Fig 3: 2 to 4 decoder logic symbol

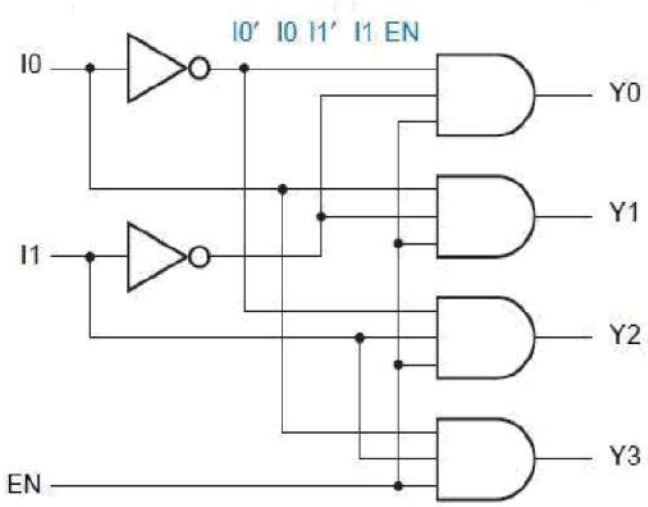


Fig 4: logic diagram of 2 to 4 decoder

The 74x139 Dual 2-to-4 Decoder

Two independent and identical 2-to-4 decoders are contained in a single MSI part, the *74x139*. The gate-level circuit diagram for this IC is shown in Figure 5.

1. The outputs and the enable input of the '139 are active-low.
2. Most MSI decoders were originally designed with active-low outputs, since TTL inverting gates are generally faster than non inverting ones.

3. '139 has extra inverters on its select inputs. Without these inverters, each select input would present three AC or DC loads instead of one, consuming much more of the fanout budget of the device that drives it.

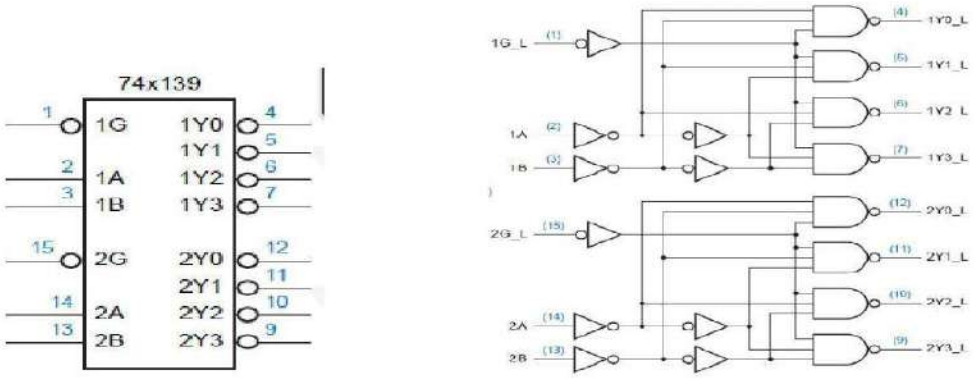


Figure 6 The 74x139 dual 2-to-4 decoder: (a) traditional logic symbol (b) logic diagram, including pin numbers for a standard 16-pin dual in-line package;

In this case, the assignment of the generic function to one half or the other of a particular '139 package can be deferred until the schematic is completed Table 5-6 is the truth table for a 74x139-type decoder.

The 74x138 3-to-8 Decoder

The *74x138* is a commercially available MSI 3-to-8 decoder whose gate-level circuit diagram and symbol are shown in Figure 7; its truth table is given in Table 5-7. Like the 74x139, the 74x138 has active-low outputs, and it has three enable inputs (G1, /G2A, /G2B), all of which must be asserted for the selected output to be asserted.

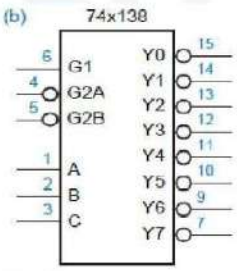


Figure 7: logic symbol of 74X138

Inputs						Outputs							
G1	G2A_L	G2B_L	C	B	A	Y7_L	Y6_L	Y5_L	Y4_L	Y3_L	Y2_L	Y1_L	Y0_L
0	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

The logic function of the '138 is straightforward—an output is asserted if and only if the decoder is enabled and the output is selected. Thus, we can easily write logic equations for an internal output signal such as Y5 in terms of the internal input signals:

$$Y5 = \underbrace{G1 \cdot G2A \cdot G2B}_{\text{enable}} \cdot \underbrace{C \cdot B' \cdot A}_{\text{select}}$$

However, because of the inversion bubbles, we have the following relations between internal and external signals:

$$G2A = G2A\_L'$$
$$G2B = G2B\_L'$$
$$Y5 = Y5\_L'$$

Therefore, if we're interested, we can write the following equation for the external output signal Y5_L in terms of external input signals:

$$\begin{aligned} Y5\_L = Y5' &= (G1 \cdot G2A\_L' \cdot G2B\_L' \cdot C \cdot B' \cdot A)' \\ &= G1' + G2A\_L + G2B\_L + C' + B + A' \end{aligned}$$

On the surface, this equation doesn't resemble what you might expect for a decoder, since it is a logical sum rather than a product. However, if you practice bubble-to-bubble logic design, you don't have to worry about this; you just give the output signal an active-low name and remember that it's active low when you connect it to other inputs.

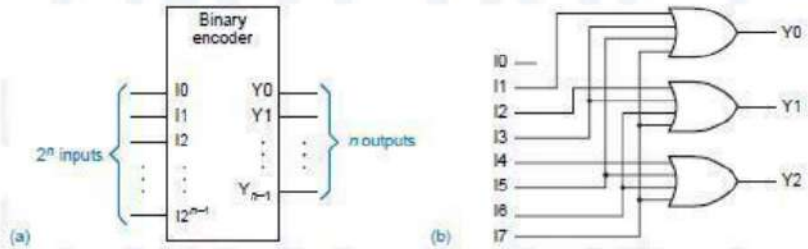
5.5 Encoders

A decoder's output code normally has more bits than its input code. If the device's output code has *fewer* bits than the input code, the device is usually called an *encoder*.

Probably the simplest encoder to build is a $2n$-to-n or *binary encoder*. As shown in Figure 5-45(a), it has just the opposite function as a binary *de*coder— its input code is the 1-out-of-$2n$ code and its output code is n-bit binary. The equations for an 8-to-3 encoder with inputs I0–I7 and outputs Y0–Y2 are given below:

$$Y0 = I1 + I3 + I5 + I7$$
$$Y1 = I2 + I3 + I6 + I7$$
$$Y2 = I4 + I5 + I6 + I7$$

The corresponding logic circuit is shown in (b). In general, a $2n$-to-n encoder can be built from n $2n$ -input1 OR gates. Bit i of the input code is connected to OR gate j if bit j in the binary representation of i is 1.



Priority Encoder:

The 1-out-of-2*n* coded outputs of an *n*-bit binary decoder are generally used to control a set of 2*n* devices, where at most one device is supposed to be active at any time. Conversely, consider a system with 2*n inputs*, each of which indicates a request for service. This structure is often found in microprocessor input/output subsystems, where the inputs might be interrupt requests.

In this situation, it may seem natural to use a binary encoder. to observe the inputs and indicate which one is requesting service at any time. However, this encoder works properly only if the inputs are guaranteed to be asserted at most one at a time. If multiple requests can be made simultaneously, the encoder gives undesirable results. For example, suppose that inputs I2 and I4 of the 8-to-3 encoder are both 1; then the output is 110, the binary encoding of 6.

Y0 = I1 + I3 + I5 + I7
Y1 = I2 + I3 + I6 + I7
Y2 = I4 + I5 + I6 + I7

Either 2 or 4, not 6, would be a useful output in the preceding example, but how can the encoding device decide which? The solution is to assign *priority* to the input lines, so that when multiple requests are asserted, the encoding device produces the number of the highest-priority requestor. Such a device is called a *priority encoder*.

Input I7 has the highest priority. Outputs A2–A0 contain the number of the highest-priority asserted input, if any. The IDLE output is asserted if no inputs are asserted.

In order to write logic equations for the priority encoder's outputs, we first define eight intermediate variables H0–H7, such that Hi is 1 if and only if Ii is the highest priority 1 input: Using these signals, the equations for the A2–A0 outputs are similar to the ones for a simple binary encoder:

H7=I7 (Highest Priority) H6=I6.I7'

H5=I5.I6'.I7'
H4=I4.I5'.I6'.I7'
H3=I3.I4'.I5'.I6'.I7'
H2=I2.I3'.I4'.I5'.I6'.I7'
H1=I1. I2'.I3'.I4'.I5'.I6'.I7'
H0=I0.I1'. I2'.I3'.I4'.I5'.I6'.I7'
IDLE= I0'.I1'. I2'.I3'.I4'.I5'.I6'.I7'

Encoder

A0=Y0 = H1 + H3 + H5 + H7
A1=Y1 = H2 + H3 + H6 + H7
A2=Y2 = H4 + H5 + H6 + H7

Multiplexers:

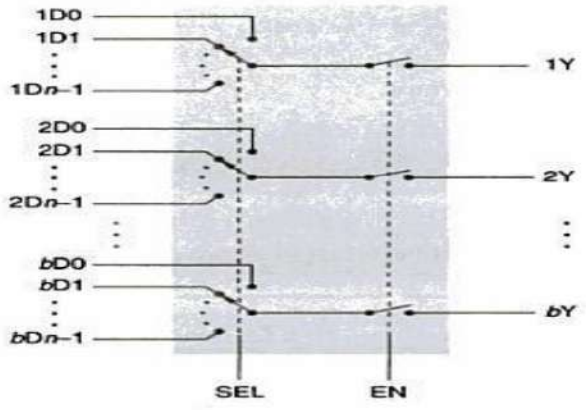
A *multiplexer* is a digital switch—it connects data from one of n sources to its output. Figure 5-61(a) shows the inputs and outputs of an n-input, b-bit multiplexer. There are n sources of data, each of which is b bits wide. A multiplexer is often called a *mux* for short.

A multiplexer can use addressing bits to select one of several input bits to be the output. A selector chooses a single data input and passes it to the MUX output.It has one output selected at a time.

Figure shows a switch circuit that is roughly equivalent to the multiplexer. However, unlike a mechanical switch, a multiplexer is a unidirectional device: information flows only from inputs (on the left) to outputs (on the right. Multiplexers are obviously useful devices in any application in which data must be switched from multiple sources to a destination. A common application

in computers is the multiplexer between the processor's registers and its arithmetic logic unit (ALU). For example, consider a 16-bit processor in which each instruction has a 3-bit field that specifies one of eight registers to use. This 3-bit field is connected to the select inputs of an 8-input, 16-bit multiplexer. The multiplexer's data inputs are connected to the eight registers, and its data outputs

are connected to the ALU to execute the instruction using the selected register.



The sizes of commercially available MSI multiplexers are limited by the number of pins available in an inexpensive IC package. Commonly used muxes come in 16-pin packages. Shown in fig which selects among eight 1-bit inputs. The select inputs are named C, B, and A, where C is most significant numerically. The enable input EN_L is active low; both active-high (Y) and active-low (Y_L) versions of the output are provided.

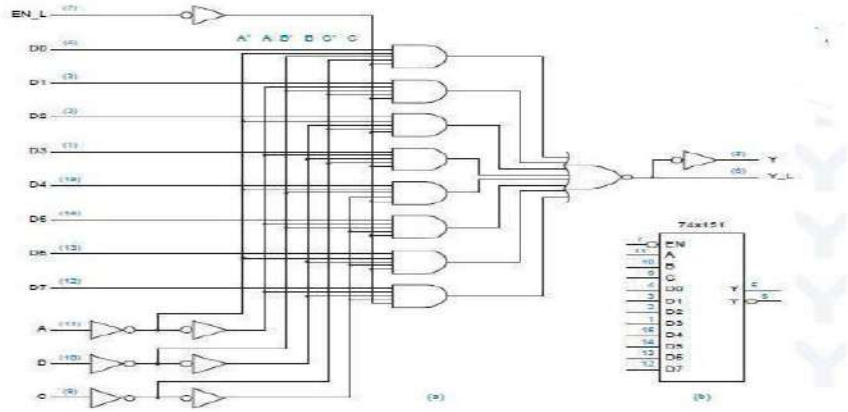
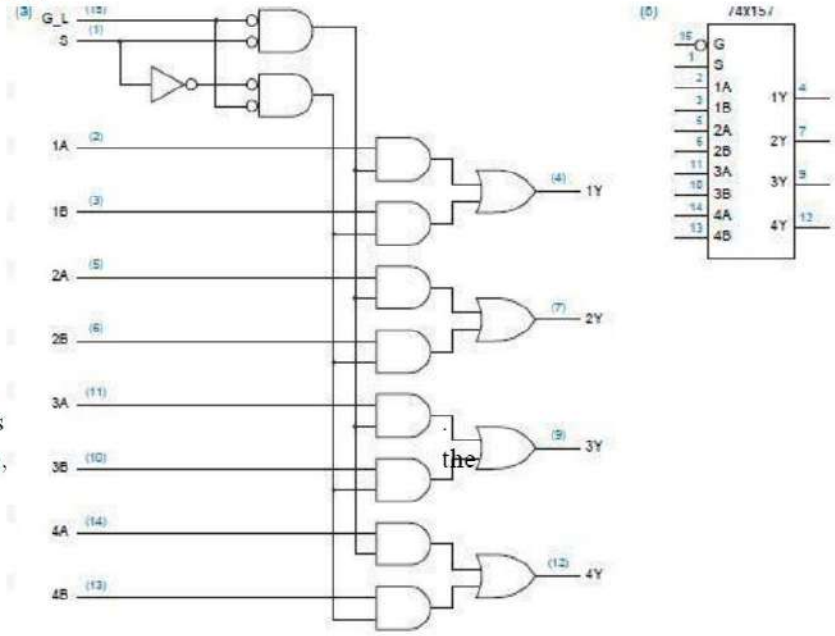


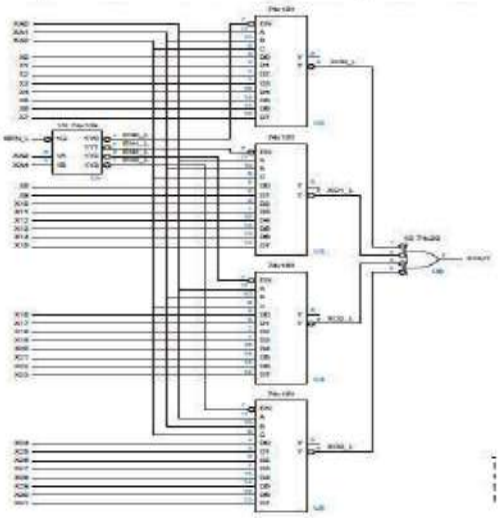
Figure The 74x151 8-input, 1-bit multiplexer: (a) logic diagram, including pin numbers for a standard 16-pin dual in-line
package; (b) traditional logic symbol.

At the other extreme of muxes in 16-pin packages, we have the *74x157*, shown in Figure, which selects between two 4-bit inputs. Just to confuse things, the manufacturer has named the select input S and the active-low enable input G_L. Also note that the data sources are named A and B .



Expanding
Seldom does
For example,
the

design of a computer processor. This function could be performed by 16 74x151 8-input, 1-bit multiplexers or equivalent ASIC cells, each handling one bit of all the inputs and the output. The processor's 3-bit register-select field would be connected to the A, B, and C inputs of all 16 muxes, so they would all select the same register source at any given time.



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Another dimension in which multiplexers can be expanded is the number of data sources. For example, suppose we needed a 32-input, 1-bit multiplexer. Figure shows one way to build it. Five select bits are required. A 2-to-4 decoder (one-half of a 74x139) decodes the two high-order select bits to enable one of four 74x151 8-input multiplexers. Since only one

'151 is enabled at a time, the '151 outputs can simply be ORed to obtain the final output.

The 32-to-1 multiplexer can also be built using 74x251s. The circuit is

identical to Figure 5-65, except that the output NAND gate is eliminated. Instead, the Y (and, if desired, Y_L) outputs of the four '251s are simply tied together. The '139 decoder ensures that at most one of the '251s has its threestate outputs enabled at any time. If the '139 is disabled (XEN_L is negated), then all of the '251s are disabled, and the XOUT and XOUT_L outputs are

undefined. However, if desired, resistors may be connected from each of these signals to 5 volts to pull the output HIGH in this case.

Multiplexers, Demultiplexers, and Buses

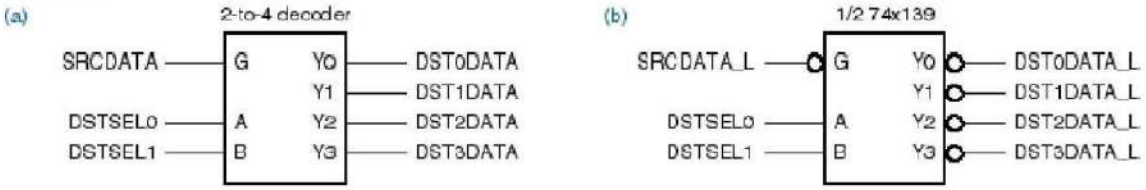
A multiplexer can be used to select one of *n* sources of data to transmit on a bus. At the far end of the bus, a *demultiplexer* can be used to route the bus data to one of *m* destinations. Such an application, using a 1-bit bus. In fact, block diagrams for logic circuits often depict multiplexers and demultiplexers , to suggest visually how a selected one of multiple data sources gets directed onto a bus and routed to a selected one of multiple destinations.

The function of a demultiplexer is just the inverse of a multiplexer's. For example, a 1-bit, *n*-output demultiplexer has one data input and *s* inputs to select one of *n s* 2data outputs. In normal operation, all outputs except the selected one are 0; the selected output equals the data input. This definition may be generalized for a *b*-bit, *n*-output demultiplexer; such a device has *b* data inputs, and its *s* select inputs choose one of *n s* 2sets of *b* data outputs.

A binary decoder with an enable input can be used as a demultiplexer, as shown in Figure 5-67. The decoder's enable input is connected to the data line, and its select inputs determine which of its output lines is driven with the data bit. The remaining output lines are negated.

Thus, the 74x139 can be used as a 2-bit, 4-output demultiplexer with active-low data inputs and outputs, and the
74x138 can be used as a 1-bit, 8-output demultiplexer. In fact, the manufacturer's catalog typically lists these ICs as "decoders/demultiplexers."

A Mux is used to select one of n sources of data to transmit on a bus. A demultiplexer can be used to route the bus data to one of m destinations. Just the inverse of a mux. A binary decoder with an enable input can be used as a Demux. E.g. 74x139 can be used as a 2-bit, 4-output Demux.



Parity Generators/Checkers:

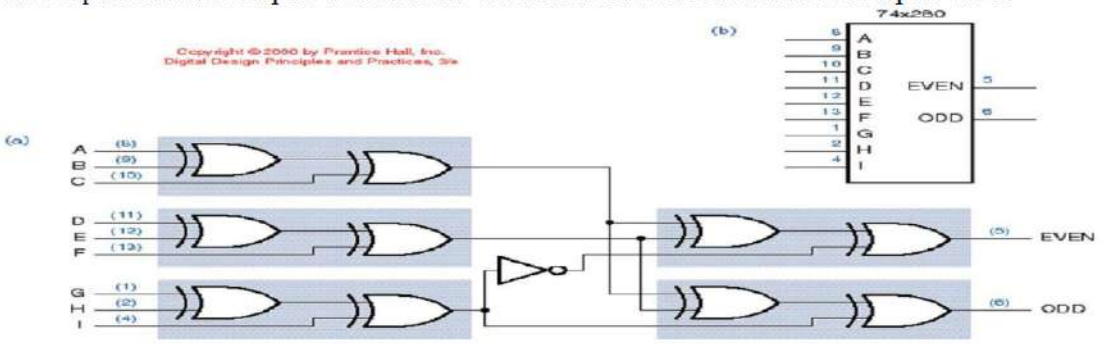
Parity Circuits

N XOR gates may be cascaded to form a circuit with *n* 1 inputs and a single output. This is called an *odd-parity circuit*, because its output is 1 if an odd number of its inputs are 1.

If the output of either circuit is inverted, we get an *even-parity circuit*, whose output is 1 if an even number of its inputs are 1.

The 74x280 9-Bit Parity Generator

Rather than build a multibit parity circuit with discrete XOR gates, it is more economical to put all of the XORs in a single MSI package with just the primary inputs and outputs available at the external pins. The *74x280* 9-bit parity generator, shown in Figure is such a device. It has nine inputs and two outputs that indicate whether an even or odd number of inputs are 1.



Parity-Checking Applications

described error-detecting codes that use an extra bit, called a parity bit, to detect errors in the transmission and storage of data. In an evenparity code, the parity bit is chosen so that the total number of 1 bits in a code word is even. Parity circuits like the 74x280 are used both to generate the correct value of the parity bit when a code word is stored or transmitted, and to check the parity bit when a code word is retrieved or received.

Figure shows how a parity circuit might be used to detect errors in the memory of a microprocessor system. The memory stores 8-bit bytes, plus a parity bit for each byte. The microprocessor uses a bidirectional bus D[0:7] to transfer data to and from the memory. Two control lines, RD and WR, are used to indicate whether a read or write operation is desired, and an ERROR signal is asserted to indicate parity errors during read operations. Complete details of the memory chips, such as addressing inputs, are not shown; memory chips are described in detail in \chapref{MEMORY}.

Parallel Binary Adder/ Subtractor

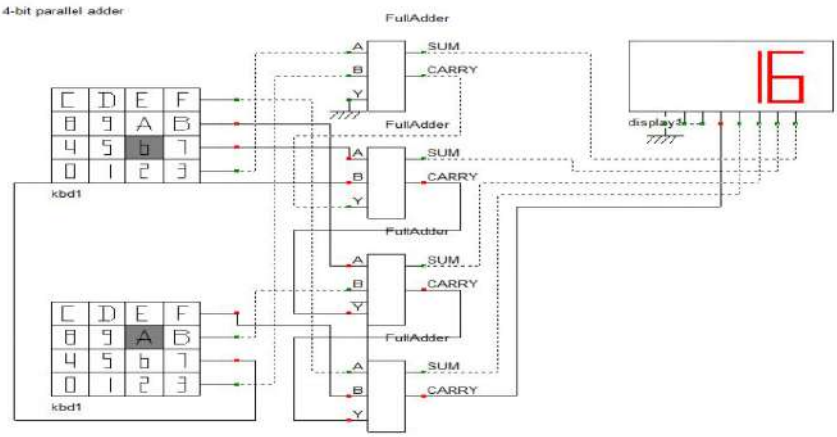
A parallel adder is an arithmetic combinational logic circuit that is used to add more than one bit of data simultaneously. A full adder adds two bits and a carry to give an output. However, to add more than one bit of data in length a parallel adder is used. A parallel adder adds corresponding bits simultaneously using full adders and keeps generating a carry and pushing it towards the next most significant bit to be added. An n-bit parallel adder uses n full adders connected in cascade with each full adder adding the two corresponding bits of both the numbers.

For example, for a binary number D3D2D1D0 and B3B2B1B0, a full adder connected in cascade would add D0 and B0 and send the result to be displayed (LSB). If a carry is generated, it will be passed on to the input of the next full adder.

How to design a 4-bit parallel adder?

To add two Hex codes we need four full adders connected in cascade. This is because a hex code can be represented by four binary bits. The four full adders will connect to each other via their CARRY outputs. And depending on the position of the bits the full adders add, the SUM outputs of the full adders will be connected to the display. The least significant bit will be connected to the LSB of the display. The most significant bit will be connected to the pin one bit before the MSB of the display. The carry output of the final full adder will be connected to the MSB pin of the display.

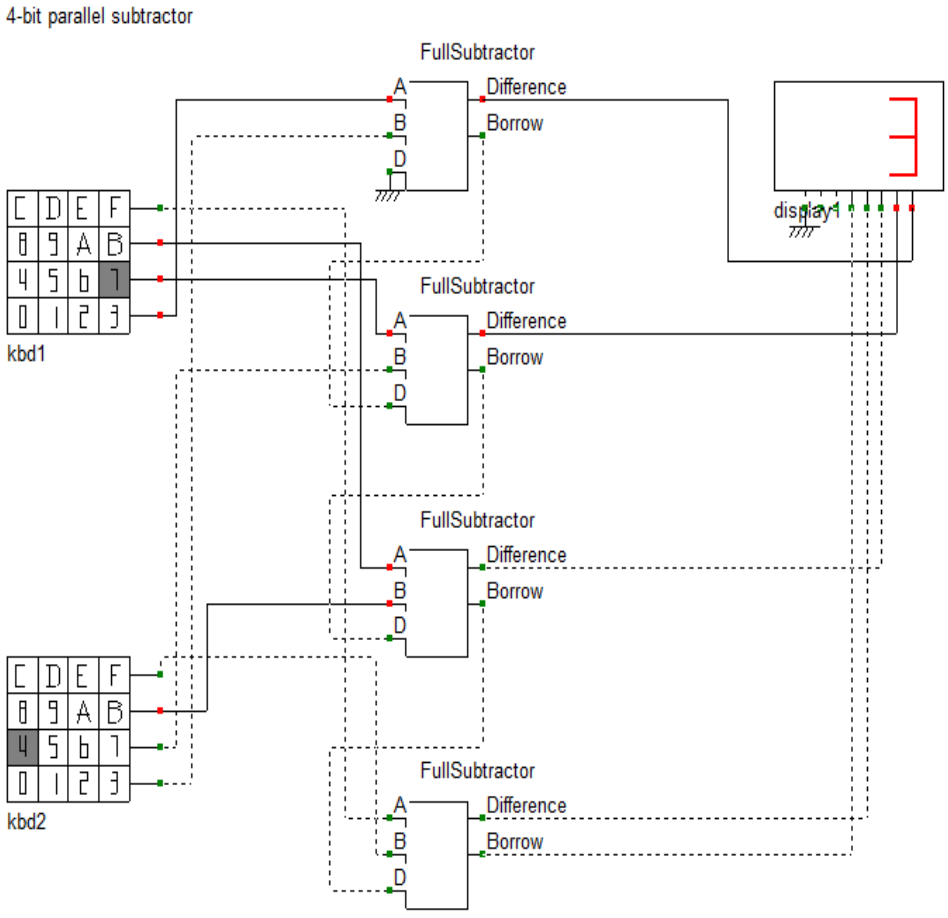
We can use two hex 4×4 keypads to generate the input bits or we can just add the bits manually. If you want a circuit diagram without the hex keypads as inputs let us know in the comments. Each row of the keypad is connected to a full adder depending on its significance. The first full adder receives inputs from the first row of the hex keypad, the second receives inputs from the second row of the hex keypad and the carry from the first and so on. The resultant combinational logic circuit is shown below.



How to design a 4-bit parallel subtractor?

A 4-bit parallel subtractor is used to subtract a number consisting of 4 bits. This is done by cascading a series of full subtractors. For an n-bit parallel subtractor, n full subtractors can be cascaded to achieve the desired output. The connections are exactly the same as that of the 4-bit parallel adder which we saw earlier in this post. Each of the bit is subtracted from its corresponding bit of equal significance from the other number. A borrow if generated, propagates through the cascade of full subtractors.

We use the same 4×4 hex keypads to input data in a full subtractor. The first rows (having the least significance compared to the other rows) of the hex keypads are connected to the first full subtractor. The second rows to the second full subtractor's inputs along with the borrow from the first full subtractor and so on. The output of each full adder is connected to the display on the basis of their positional significance in the answer. i.e the output of the first full subtractor is connected to the LSB of the display. The final borrow output of the final full subtractor is connected to the MSB pin of the display



Magnitude Comparators:

Comparators

Comparing two binary words for equality is a commonly used operation in computer systems and device interfaces. we showed a system structure in which devices are enabled by comparing a "device select" word with a predetermined "device ID." A circuit that compares two binary words and indicates whether they are equal is called a *comparator*. Some comparators interpret their input words as signed or unsigned numbers and also indicate an arithmetic relationship (greater or less than) between the words. These devices are often called *magnitude comparators*.

Inputs				Outputs		
A_1	A_0	B_1	B_0	A > B	A = B	A< B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

A > B

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

$$A>B = A_0\overline{B}_1\overline{B}_0 + A_1\overline{B}_1 + A_1A_0\overline{B}_0$$

A = B

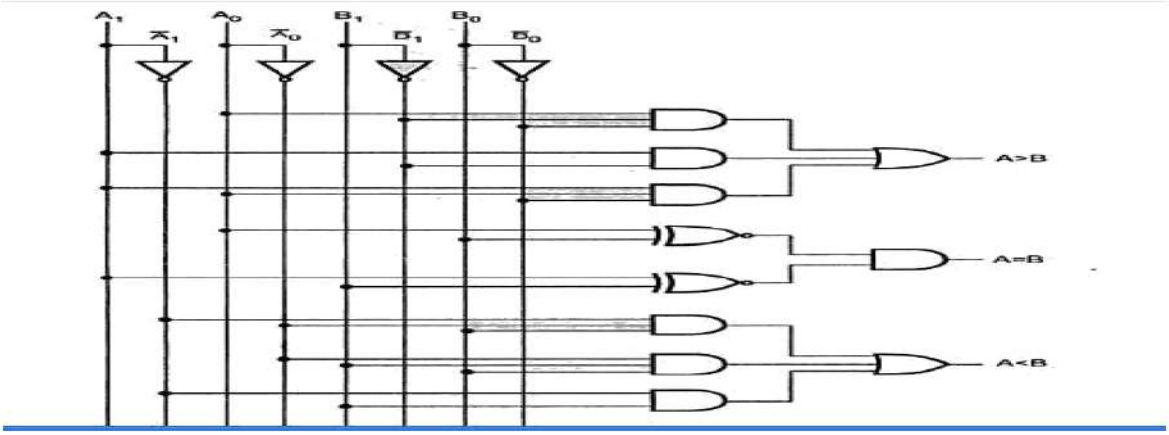
A_1A_0 \ B_1B_0	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

A < B

A_1A_0 \ B_1B_0	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

Fig. 4.93

$$\begin{aligned}(A = B) &= \overline{A}_1\overline{A}_0\overline{B}_1\overline{B}_0 + \overline{A}_1A_0\overline{B}_1B_0 \\ &\quad + A_1A_0B_1B_0 + A_1\overline{A}_0B_1\overline{B}_0 \\ &= \overline{A}_1\overline{B}_1(\overline{A}_0\overline{B}_0 + A_0B_0) \\ &\quad + A_1B_1(A_0B_0 + \overline{A}_0\overline{B}_0) \\ &= (A_0 \odot B_0)(A_1 \odot B_1) \\ (A < B) &= \overline{A}_1\overline{A}_0B_0 + \overline{A}_0B_1B_0 + \overline{A}_1B_1\end{aligned}$$


A1
A0
B1
B0
A>B
A=B
A<B

UNIT-V

SEQUENTIAL LOGIC IC'S AND MEMORIES

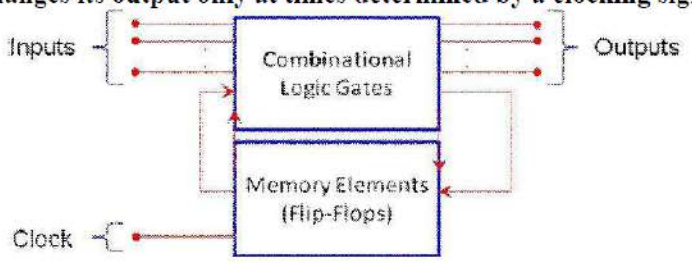
All Types of Flip-flops:

A *bistable memory device* is the generic term for the elements we are studying.

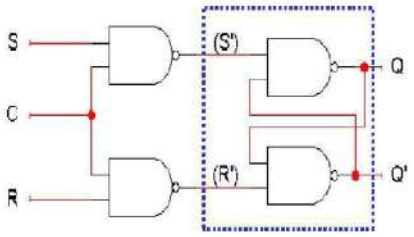
Latches and Flip flops

***Latches and flip-flops* (FFs) are the basic building blocks of sequential circuits.**

latch: bistable memory device with level sensitive triggering (no clock), watches all of its inputs continuously and changes its outputs at any time, independent of a clocking signal.
flip-flop: bistable memory device with edge-triggering (with clock), samples its inputs, and changes its output only at times determined by a clocking signal.



- Here is an SR latch with a control input C.
- Notice the hierarchical design!
  - The dotted blue box is the S'R' latch.
  - The additional NAND gates are simply used to generate the correct inputs for the S'R' latch.
- The control input acts just like an enable.



C	S	R	S'	R'	Q
0	x	x	1	1	No change
1	0	0	1	1	No change
1	0	1	1	0	0 (reset)
1	1	0	0	1	1 (set)
1	1	1	0	0	Avoid!

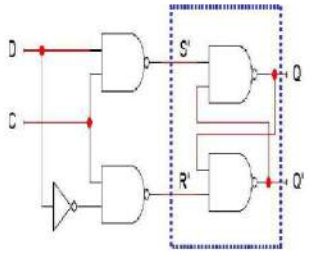
D latch

- Finally, a D latch is based on an S'R' latch. The additional gates generate the S' and R' signals, based on inputs D ("data") and C ("control").

– When C = 0, S' and R' are both 1, so the state Q does not change.

– When C = 1, the latch output Q will equal the input D.

- No more messing with one input for set and another input for reset!

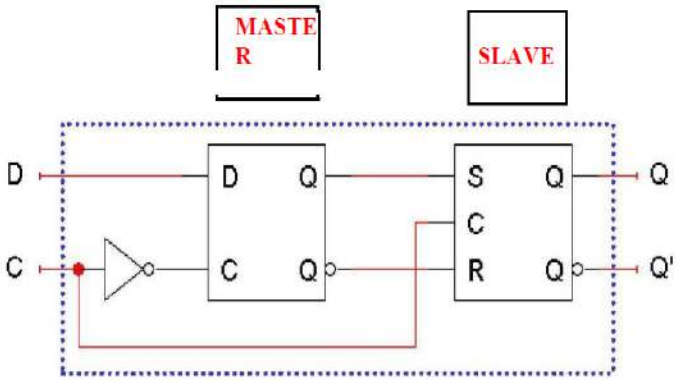


C	D	Q
0	x	No change
1	0	0
1	1	1

- Also, this latch has no "bad" input combinations to avoid. Any of the four possible assignments to C and D are valid.

Flip-flops

- Here is the internal structure of a D flip-flop.
  - The flip-flop inputs are C and D, and the outputs are Q and Q'.
  - The D latch on the left is the master, while the SR latch on the right is called the slave.
- Note the layout here.
  - The flip-flop input D is connected directly to the master latch.
  - The master latch output goes to the slave.
  - The flip-flop outputs come directly from the slave latch.



D flip-flops when C=0

- The D flip-flop's control input C enables *either* the D latch or the SR latch, but not both.
- When C = 0:
  - The master latch is enabled, and it monitors the flip-flop input D. Whenever D changes, the master's output changes too.
  - The slave is disabled, so the D latch output has no effect on it. Thus, the slave just maintains the flip-flop's current state.

D flip-flops when C=1

- *As soon as C becomes 1,*
  - The master is disabled. Its output will be the *last* D input value seen just before C became 1.
  - Any subsequent changes to the D input while C = 1 have no effect on the master latch, which is now disabled.
  - The slave latch is enabled. Its state changes to reflect the master's output, which again is the D input value from right when C became 1.

Positive edge triggering

- This is called a positive edge-triggered flip-flop.
  - The flip-flop output Q changes *only* after the positive edge of C.
  - The change is based on the flip-flop input values that were present right at the positive edge of the clock signal.

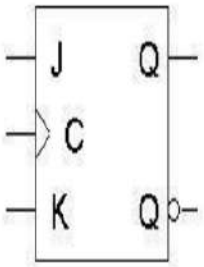
The D flip-flop's behavior is similar to that of a D latch except for the positive edge-triggered nature, which is not explicit in this table

C	D	Q
0	x	No change
1	0	0 (reset)
1	1	1 (set)

Flip-flop variations

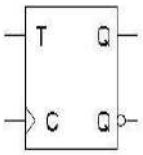
- We can make different versions of flip-flops based on the D flip-flop, just like we made different latches based on the S'R' latch.

- A JK flip-flop has inputs that act like S and R, but the inputs JK=11 are used to *complement* the flip-flop's current state.



C	J	K	Qnext
0	x	x	No change
1	0	0	No change
1	0	1	0 (reset)
1	1	0	1 (set)
1	1	1	Q'current

A T flip-flop can only maintain or complement its current state



C	T	Qnext
0	x	No change
1	0	No change
1	1	Q'current

Characteristic equations

- We can also write characteristic equations, where the next state Q(t+1) is defined in terms of the current state Q(t) and inputs.

D	Q(t+1)	Operation
0	0	Reset
1	1	Set

Q(t+1) = D

J	K	Q(t+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

Q(t+1) = K'Q(t) + JQ'(t)

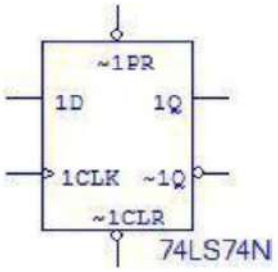
T	Q(t+1)	Operation
0	Q(t)	No change
1	Q'(t)	Complement

Q(t+1) = T'Q(t) + TQ'(t) = T Q(t)

Flip-Flop Vs. Latch

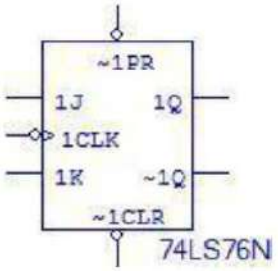
- The primary difference between a D flip-flop and D latch is the EN/CLOCK input.
- The flip-flop's CLOCK input is edge sensitive, meaning the flip-flop's output changes on the edge (rising or falling) of the CLOCK input.
- The latch's EN input is level sensitive, meaning the latch's output changes on the level (high or low) of the EN input.

Flip-Flops & Latches



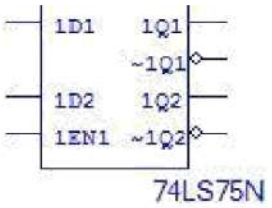
74LS74

Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs



74LS76

Dual Negative-Edge-Triggered J-K Flip-Flops with Preset, Clear, and Complementary Outputs



74LS75 Quad Latch

74LS74: D Flip-Flop

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

74LS76: J/K Flip-Flop

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	⎍	L	L	Q_o	$\overline{Q}_o$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transfered to the outputs on the falling edge of the clock pulse.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.
Note 1: This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Conversion of Flip flops

For the conversion of one flip flop to another, a combinational circuit has to be designed first. If a JK Flip Flop is required, the inputs are given to the combinational circuit and the output of the combinational circuit is connected to the inputs of the actual flip flop. Thus, the output of the actual flip flop is the output of the required flip flop. In this post, the following flip flop conversions will be explained.

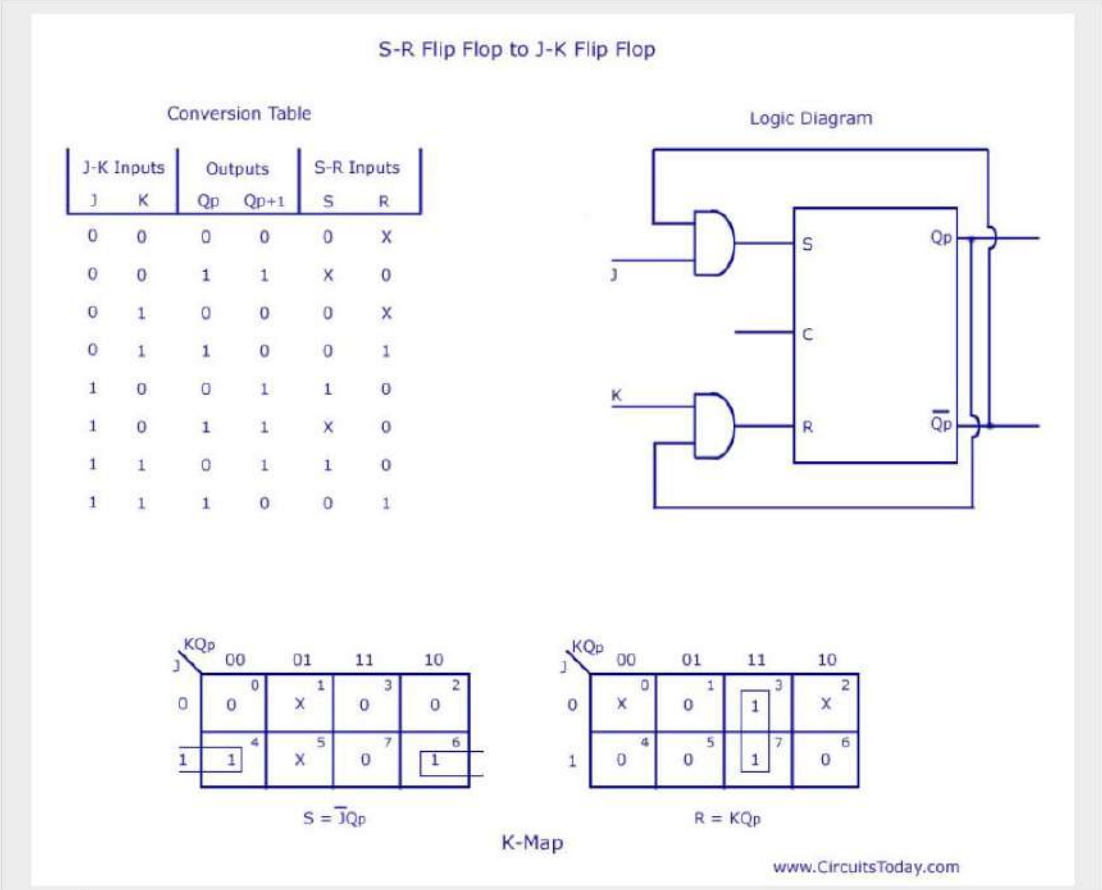
- SR Flip Flop to JK Flip Flop
- JK Flip Flop to SR Flip Flop
- SR Flip Flop to D Flip Flop
- D Flip Flop to SR Flip Flop
- JK Flip Flop to T Flip Flop
- JK Flip Flop to D Flip Flop
- D Flip Flop to JK Flip Flop

SR Flip Flop to JK Flip Flop

As told earlier, J and K will be given as external inputs to S and R. As shown in the logic diagram below, S and R will be the outputs of the combinational circuit.

The truth tables for the flip flop conversion are given below. The present state is represented by Qp and Qp+1 is the next state to be obtained when the J and K inputs are applied.

For two inputs J and K, there will be eight possible combinations. For each combination of J, K and Qp, the corresponding Qp+1 states are found. Qp+1 simply suggests the future values to be obtained by the JK flip flop after the value of Qp. The table is then completed by writing the values of S and R required to get each Qp+1 from the corresponding Qp. That is, the values of S and R that are required to change the state of the flip flop from Qp to Qp+1 are written.

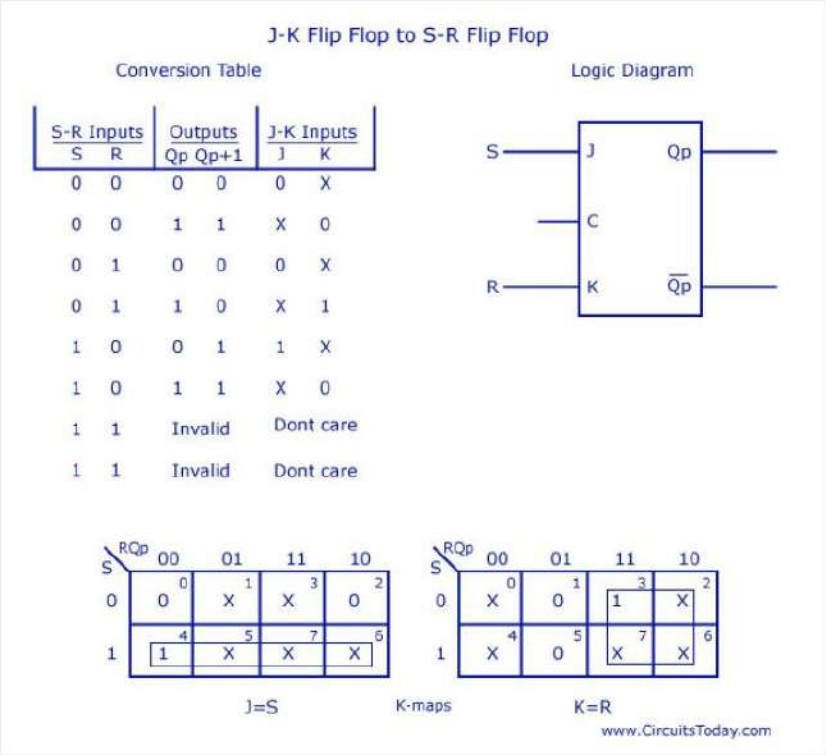


SR Flip Flop to JK Flip Flop

⊡ **JK Flip Flop to SR Flip Flop**

This will be the reverse process of the above explained conversion. S and R will be the external inputs to J and K. As shown in the logic diagram below, J and K will be the outputs of the combinational circuit. Thus, the values of J and K have to be obtained in terms of S, R and Qp. The logic diagram is shown below.

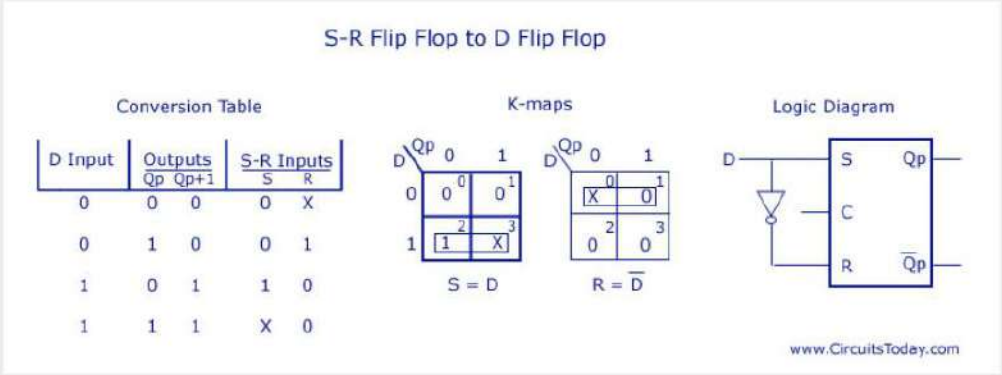
A conversion table is to be written using S, R, Qp, Qp+1, J and K. For two inputs, S and R, eight combinations are made. For each combination, the corresponding Qp+1 outputs are found ut. The outputs for the combinations of S=1 and R=1 are not permitted for an SR flip flop. Thus the outputs are considered invalid and the J and K values are taken as "don't cares".



JK Flip Flop to SR Flip Flop

⊡ SR Flip Flop to D Flip Flop

As shown in the figure, S and R are the actual inputs of the flip flop and D is the external input of the flip flop. The four combinations, the logic diagram, conversion table, and the K-map for S and R in terms of D and Qp are shown below.

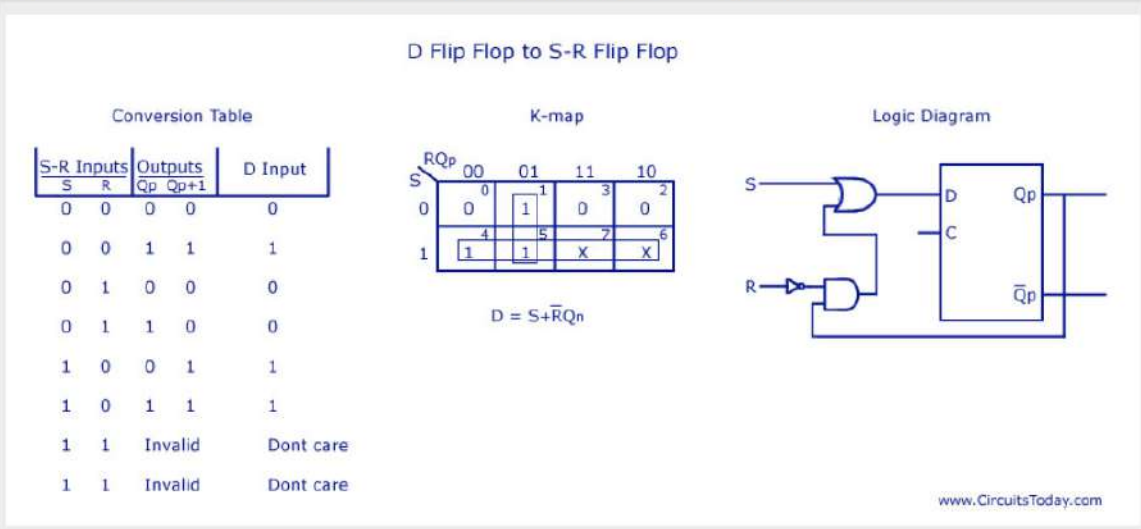


SR Flip Flop to D Flip Flop

⊡ D Flip Flop to SR Flip Flop

D is the actual input of the flip flop and S and R are the external inputs. Eight possible combinations are achieved from the external inputs S, R and Qp. But, since the combination of S=1 and R=1 are

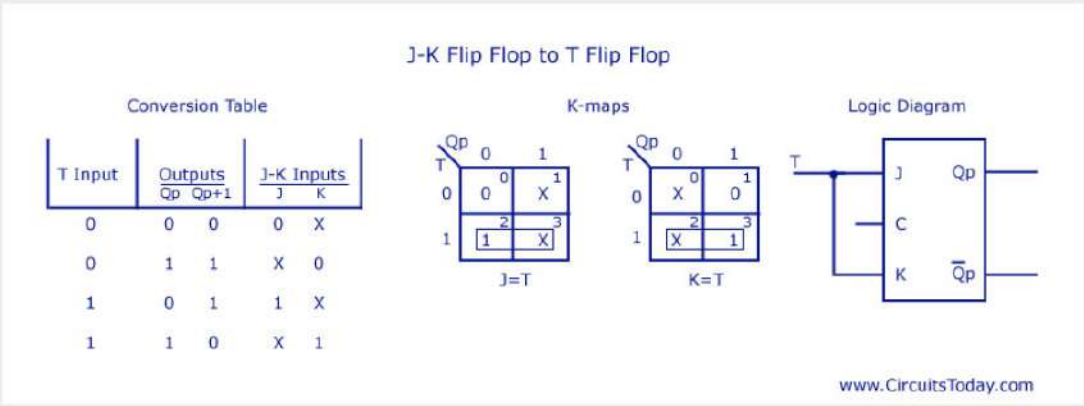
invalid, the values of Qp+1 and D are considered as "don't cares". The logic diagram showing the conversion from D to SR, and the K-map for D in terms of S, R and Qp are shown below.



D Flip Flop to SR Flip Flop

⊡ JK Flip Flop to T Flip Flop

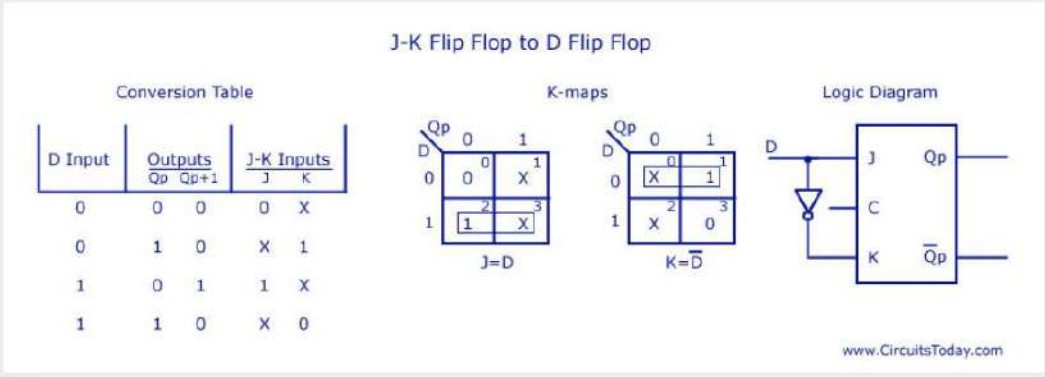
J and K are the actual inputs of the flip flop and T is taken as the external input for conversion. Four combinations are produced with T and Qp. J and K are expressed in terms of T and Qp. The conversion table, K-maps, and the logic diagram are given below.



JK Flip Flop to T Flip Flop

⊡ JK Flip Flop to D Flip Flop

D is the external input and J and K are the actual inputs of the flip flop. D and Qp make four combinations. J and K are expressed in terms of D and Qp. The four combination conversion table, the K-maps for J and K in terms of D and Qp, and the logic diagram showing the conversion from JK to D are given below.

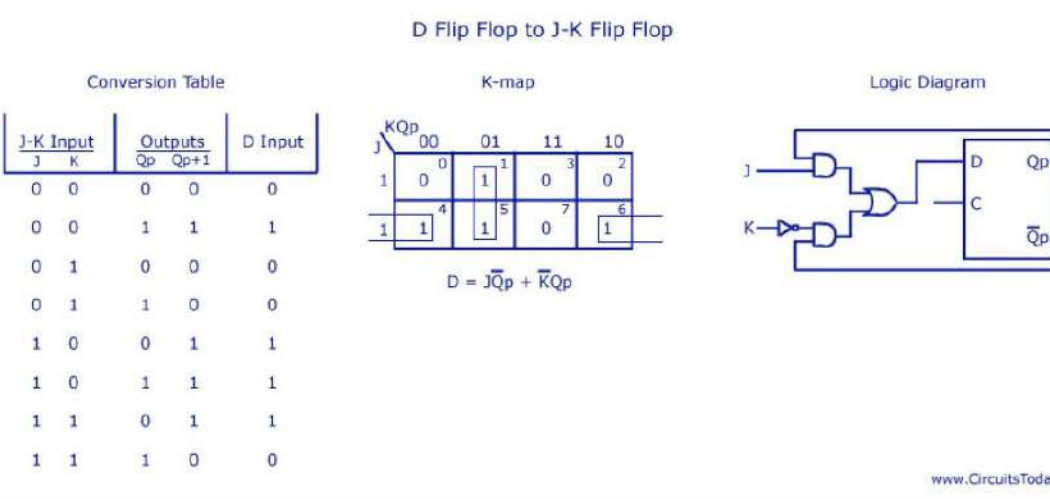


JK Flip Flop to D Flip Flop

⊡ D Flip Flop to JK Flip Flop

In this conversion, D is the actual input to the flip flop and J and K are the external inputs. J, K and Qp make eight possible combinations, as shown in the conversion table below. D is expressed in terms of J, K and Qp.

The conversion table, the K-map for D in terms of J, K and Qp and the logic diagram showing the conversion from D to JK are given in the figure below.



D Flip Flop to JK Flip Flop

Synchronous Counters

Counters are classified into two broad categories according to the way they are clocked; asynchronous and synchronous.

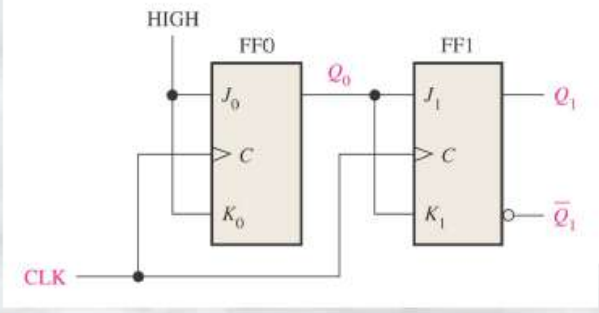
In asynchronous counters, commonly called ripple counters, the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the precedingflip-flop.

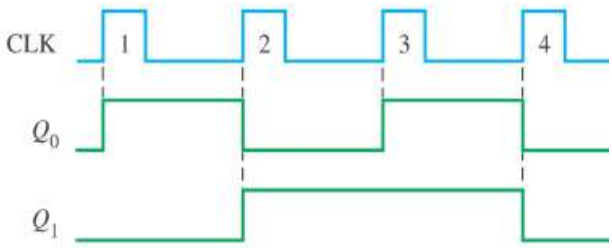
In synchronous counters, the clock input is connected to all of the flip-flops so that they are clocked simultaneously.

With in each of these two categories, counters are classified primarily by the type of sequence, the number of states, or the number of flip-flops in the counter.

Synchronous Counter Operation

- Synchronous counters have a common clock pulse applied simultaneously to all flip-flops.
- A 2-Bit Synchronous Binary Counter





Inputs			Outputs		Comments
J	K	CLK	Q	$\overline{Q}$	
0	0	↑	Q_0	$\overline{Q_0}$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	Q_0	Q_0	Toggle

Note that both the J and K inputs are connected together. The flip-flop will toggle when both are a 1 (FF0)

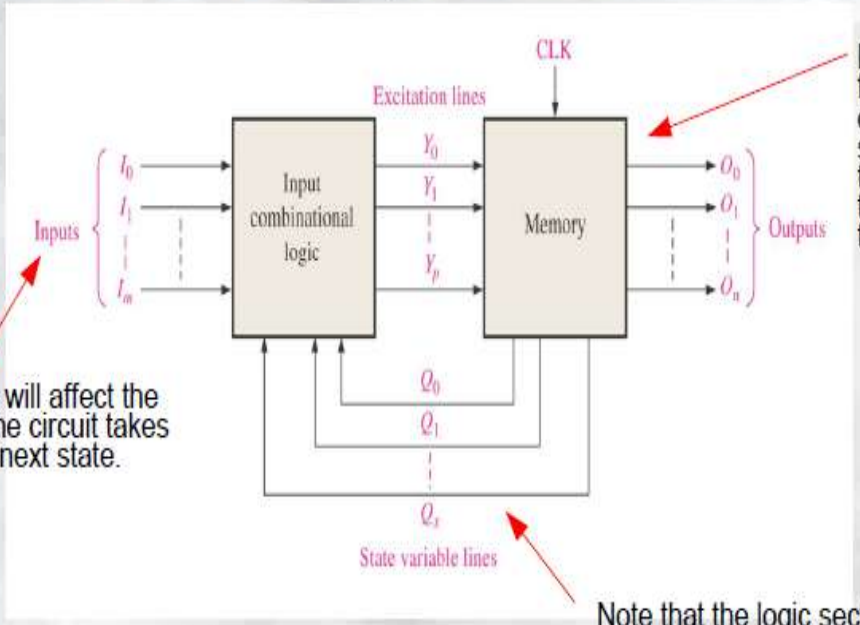
Also the transition at clock pulse 2 works because of propagation delay effects. Q0 is still high on the input of Q1 at the instant clock 2 hits so FF1 changes state. A short time later clock 2 has propagated through FF0 and it goes low.

Design of Synchronous Counters

- We can use synchronous counting circuits to implement state machines.
- State machines are useful in many control and digital applications as they provide the means for taking specific action based upon what state the machine is in and, perhaps, some external event.
- Two types of state machines
  - Moore Circuits – the outputs depend only on the present internal state
  - Mealy Circuits – the output depends on the present state and one or more inputs.

State machines are sequential in that they follow prescribed paths. But the path may vary depending on events.

- General Model of a Sequential Circuit



Memory circuits are flip-flops. They are always in one state or another. The state they are in is called the *present state*. When they change, they go to the *next state*.

Inputs will affect the path the circuit takes to the next state.

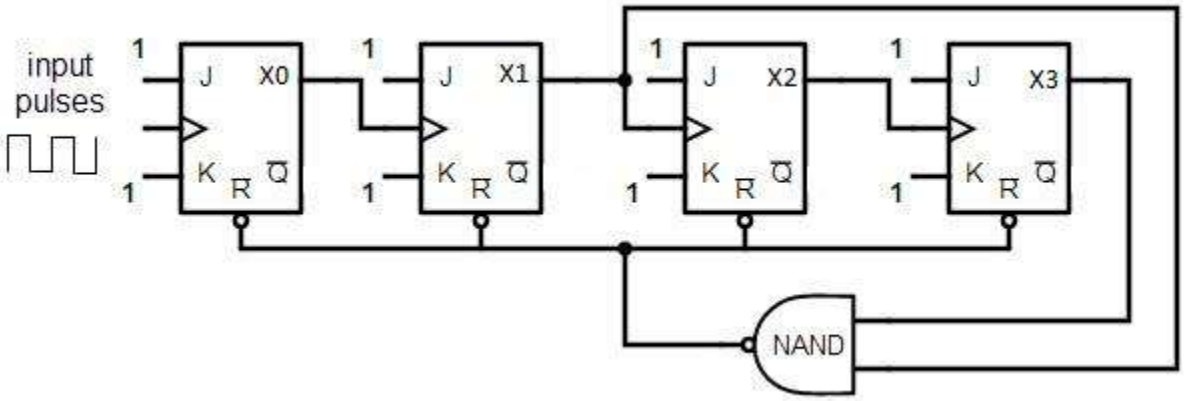
The present state of the output variables Q0 through Qn define the value of the state they are in.

Note that the logic section also looks at the output as well as the input.

Decade Counters

A binary coded decimal (BCD) is a serial digital counter that counts ten digits .And it resets for every new clock input. As it can go through 10 unique combinations of output, it is also called as "Decade counter". A BCD counter can count 0000, 0001, 0010, 1000, 1001, 1010, 1011, 1110, 1111, 0000, and 0001 and so on.

A 4 bit binary counter will act as decade counter by skipping any six outputs out of the 16 (24) outputs. There are some available ICs for decade counters which we can readily use in our circuit, like 74LS90. It is an asynchronous decade counter.

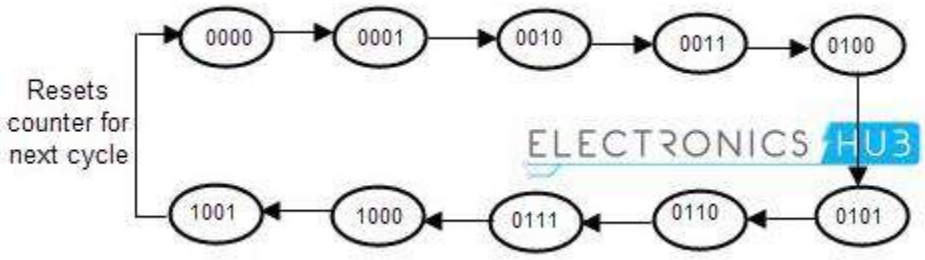


The above figure shows a decade counter constructed with JK flip flop. The J output and K outputs are connected to logic 1. The clock input of every flip flop is connected to the output of next flip flop, except the last one.

The output of the NAND gate is connected in parallel to the clear input 'CLR' to all the flip flops. This ripple counter can count up to 16 i.e. 24.

State Diagram of Decade Counter

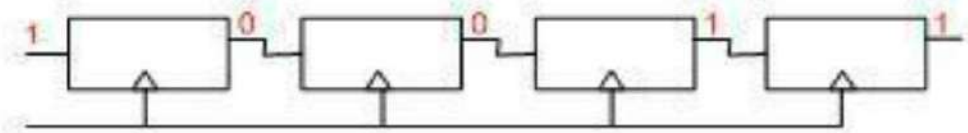
The state diagram of Decade counter is given below. State diagram of Decade counter

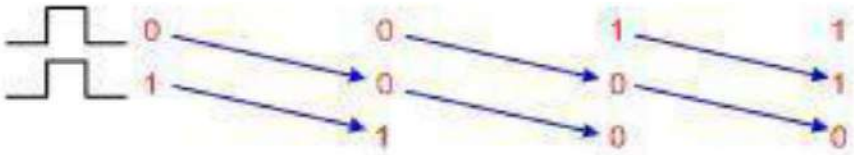


Shift Registers

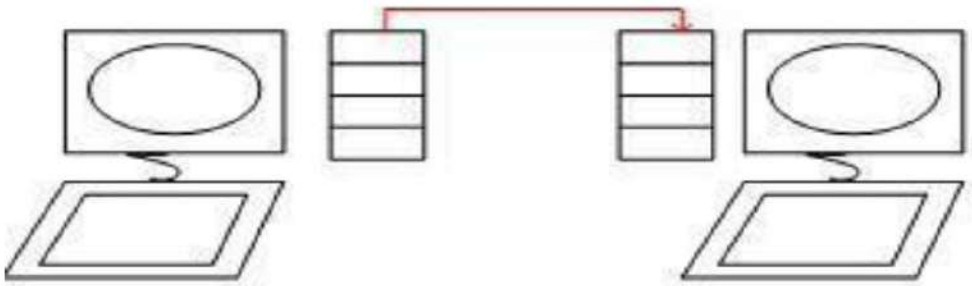
Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All the flip-flops are driven by a common clock, and all are set or reset simultaneously. In this chapter, the basic types of shift registers are studied, such as Serial In - Serial Out, Serial In - Parallel Out, Parallel In - Serial Out, Parallel In - Parallel Out, and bidirectional shift registers. A special form of counter - the shift register counter, is also introduced.

Let's observe the values of the flip flops in this shift register for the next couple of clock pulse:



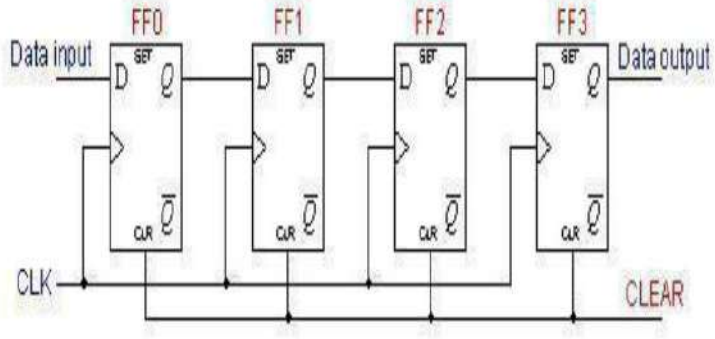


We are actually shifting our data to the right on every clock pulse.Shift registers are widely used in parallel to serial converters which find applications in computer communications.



Serial In - Serial Out Shift Registers

A basic four-bit shift register can be constructed using four D flip-flops, as shown below. The operation of the circuit is as follows. The register is first cleared, forcing all four outputs to zero. The input data is then applied sequentially to the D input of the first flip-flop on the left (FF0). During each clock pulse, one bit is transmitted from left to right. Assume a data word to be 1001. The least significant bit of the data has to be shifted through the register from FF0 to FF3.

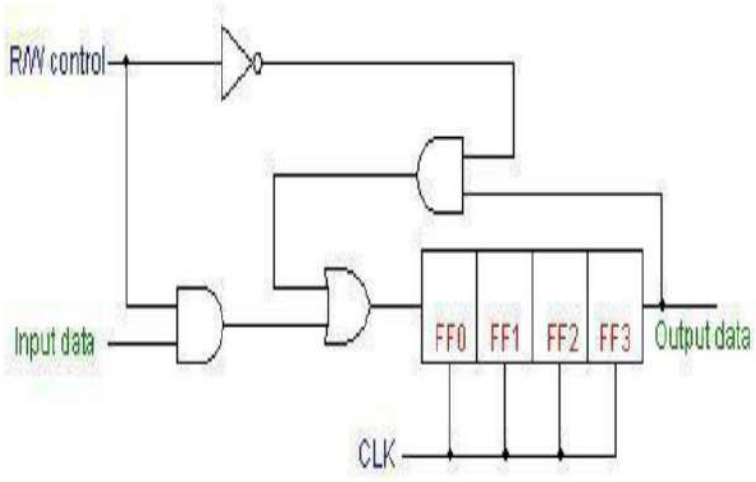


	FF0	FF1	FF2	FF3
CLEAR	0	0	0	0

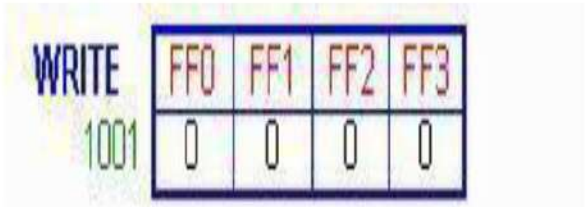
In order to get the data out of the register, they must be shifted out serially. This can be done destructively or non-destructively. For destructive readout, the original data is lost and at the end of the read cycle, all flip-flops are reset to zero.

	FF0	FF1	FF2	FF3
CLEAR	0	0	0	0

To avoid the loss of data, an arrangement for a non-destructive reading can be done by adding two AND gates, an OR gate and an inverter to the system. The construction of this circuit is shown below

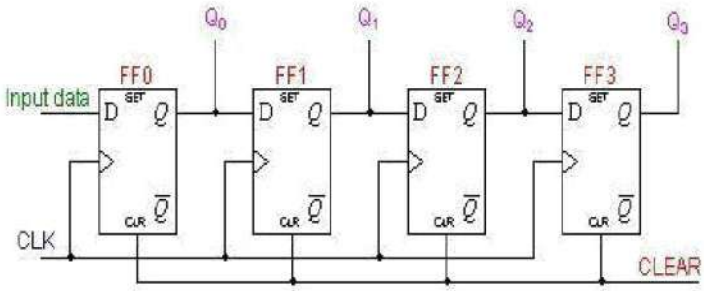


The data is loaded to the register when the control line is HIGH (ie WRITE). The data can be shifted out of the register when the control line is LOW (ie READ). This is shown in the animation below

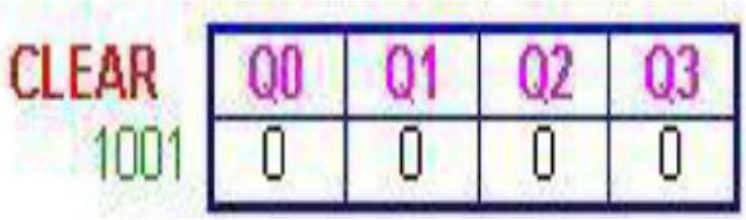


Serial In - Parallel Out Shift Registers

For this kind of register, data bits are entered serially in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. A construction of a four-bit serial in - parallel out register is shown below.

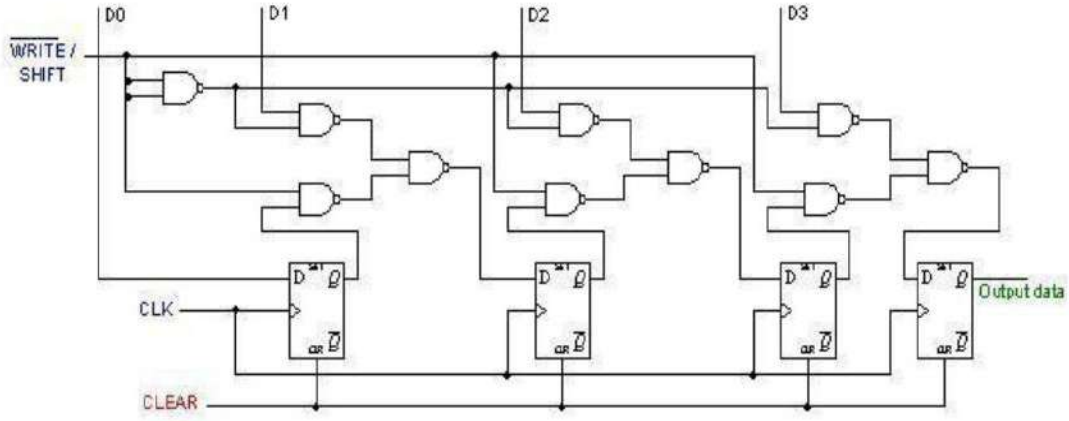


In the animation below, we can see how the four-bit binary number 1001 is shifted to the Q outputs of the register.



Parallel In - Serial Out Shift Registers

A four-bit parallel in - serial out shift register is shown below. The circuit uses D flip-flops and NAND gates for entering data (ie writing) to the register.

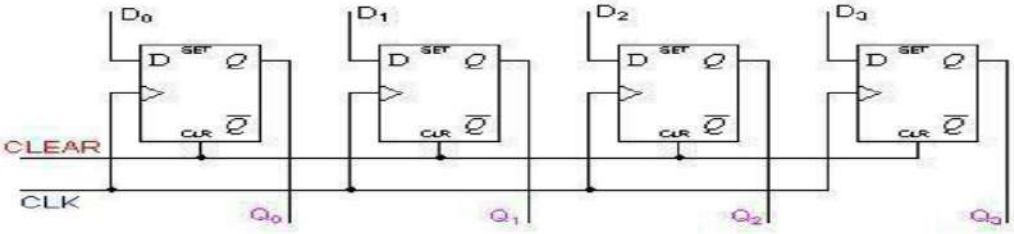


D0, D1, D2 and D3 are the parallel inputs, where D0 is the most significant bit and D3 is the least significant bit. To write data in, the mode control line is taken to LOW and the data is clocked in. The data can be shifted when the mode control line is HIGH as SHIFT is active high. The register performs right shift operation on the application of a clock pulse, as shown in the animation below.

	Q0	Q1	Q2	Q3
CLEAR	0	0	0	0

Parallel In - Parallel Out Shift Register

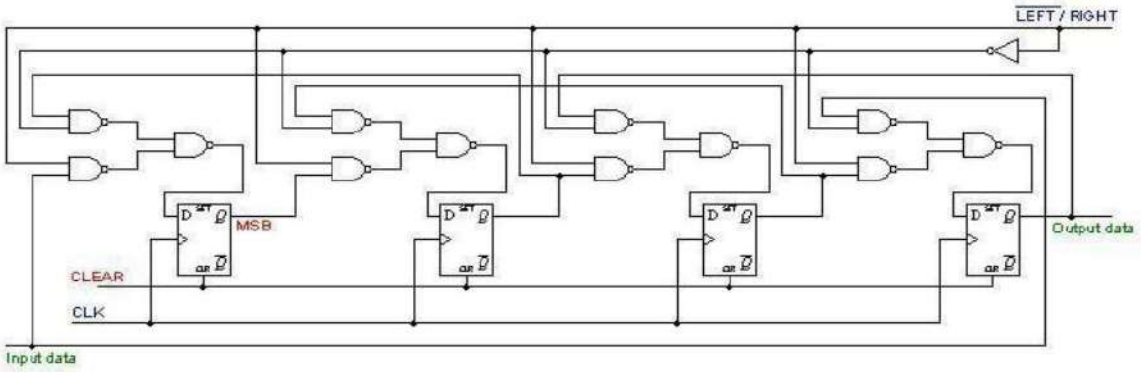
For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by D flip-flops.



The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously.

Bidirectional Shift Registers

The registers discussed so far involved only right shift operations. Each right shift operation has the effect of successively dividing the binary number by two. If the operation is reversed (left shift), this has the effect of multiplying the number by two. With suitable gating arrangement a serial shift register can perform both operations. A *bidirectional*, or *reversible*, shift register is one in which the data can be shift either left or right. A four-bit bidirectional shift register using D flip-flops is shown below.


LEFT / RIGHT
MSB
Output data
CLEAR
CLK
Input data

MEMORIES - ROM Architecture, Types of ROMS & Applications

A ROM is essentially a memory device in which permanent binary information is stored. The binary information must be specified by the designer and is then embedded in the unit to form the required interconnection pattern. Once the pattern is established it stays within the unit even when power is turned off and on again.

A block diagram of ROM is shown in the Figure 1. It consists of k inputs and n outputs. The inputs provide the address for the memory and the outputs give the data bits of the stored word which is selected by the address. The number of words in a ROM is determined from the fact that k address input lines are needed to specify 2^k words.

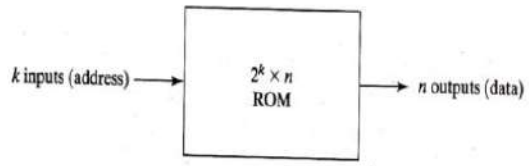


Fig 1 ROM Block Diagram

ROM does not have data inputs because it does not have a write operation.

Consider for example a 32 x 8 ROM. The unit consists of 32 words of 8 bits each. There are five input lines that form the binary numbers from 0 through 31 for the address. The Figure 2 shows the internal logic construction of the ROM. The five inputs are decoded into 32 distinct outputs by means of a 5 x 32 decoder. Each output of the decoder represents a memory address. The 32 outputs of the decoder are connected to each of the eight OR gates.

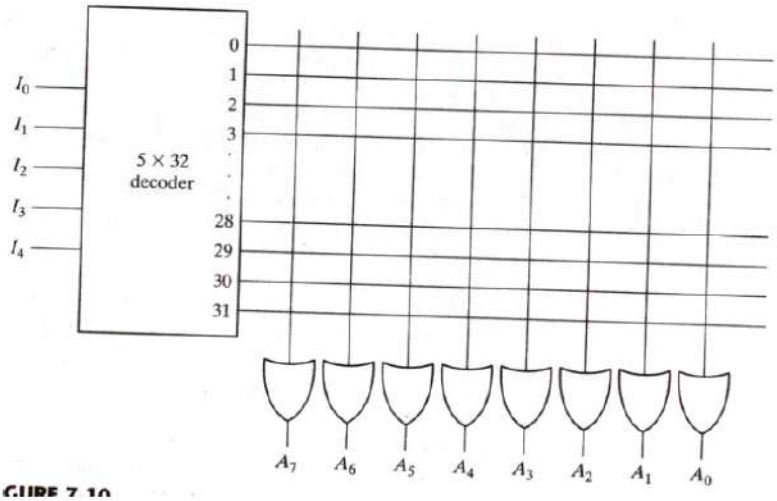


Fig 2 Internal Logic of a 32 X 8 ROM

The diagram shows the array logic convention used in complex circuits . Each OR gate must be considered as having 32 inputs. Each output of the decoder is connected to one of the inputs of each OR gate. Since each OR gate has 32 input connections and there are 8 OR gates, the ROM contains 32 x 8 = 256 internal connections.

In general, a 2^k x n ROM will have an internal k x 2^k decoder and n OR gates. Each OR gate has 2^k inputs, which are connected to each of the outputs of the decoder.

The 256 intersections of the above figure are programmable. A programmable connection

Inputs					Outputs				
I4	I3	I2	I1	I0	A7	A6	A5	A4	A3
0	0	0	0	0	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1
0	0	0	1	0	1	1	0	0	0
0	0	0	1	1	1	0	1	1	0
		⋮					⋮		
1	1	1	0	0	0	0	0	0	1
1	1	1	0	1	1	1	1	0	0
1	1	1	1	0	0	1	0	0	1
1	1	1	1	1	0	0	1	1	0

Table 1 ROM Truth Table

Between the lines is logically equivalent to a switch that can be altered to either be close or open .The programmable intersection between two lines is sometimes called cross point.

The internal binary storage of a ROM is specified by a truth table that shows the word content in each address. The Table 1 shows the five inputs under which are listed all 32 addresses. At each address, there is stored a word of 8 bits, which is listed under the outputs columns .The table shows only the first four and the last four words in the ROM. The complete table must include the list of all 32 words.

The hardware procedure that programs the ROM results in blowing fuse links according to a given truth table. The programming of ROM according to the truth table is given in Table 1 , results in the configuration shown in Figure 2.

Every 0 listed in the truth table specifies a no connection and every 1 listed specifies a path that is obtained by a connection. The four 0's in the word are programmed by blowing the fuse links between output 3 of the decoder and the inputs of the OR gates associated with outputs A_6 , A_3, A_2 and A_0. The four 1's in the word are marked in the diagram with a X to denote a connection in place of a dot used for permanent connection in logic diagrams.

When the input of the ROM is 00011, all the outputs of the decoder are 0 except for output 3, which is at logic 1. The signal equivalent to logic 1 at decoder output 3 propagates through the connections to the OR gate outputs of A_7 , A_5, A_4 and A_1.The other four outputs remain at 0. The result is that the stored word 10110010 is applied to the eight data outputs.

COMBINATIONAL PLDs

The PROM is a combinational programmable logic device (PLD). A combinational PLD is an integrated circuit with programmable gates divided into an AND array and an OR array to provide an AND-OR sum of product implementation.

There are three major types of combinational PLDs and they differ in the placement of the programmable connections in the AND-OR array. The Figure 3 shows the configuration of three PLDs.

The PROM has a fixed AND array constructed as a decoder and programmable OR array. The programmable OR gates implement the Boolean functions in sum of minterms.

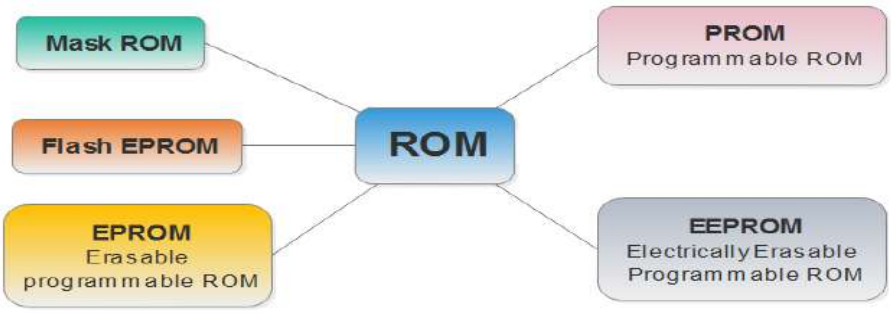
Types of ROM:

Although all ROM basically serves the same purpose, there are a few different types commonly in use today.

Understanding the different types of ROMs will also help you understand how they're used for different applications, and which type may apply to your application.

Some of them are:

1. PROM (Programmable ROM)
2. EPROM (Erasable Programmable ROM)
3. EEPROM (electrically erasable programmable ROM)
4. Flash EPROM
5. Mask ROM



1. PROM (programmable ROM) and OTP

PROM refers to the kind of ROM that the user can burn information into. In other words, PROM is a user-programmable memory.

For every bit of the PROM, there exists a fuse. PROM is programmed by blowing the fuses. If the information burned into PROM is wrong, that PROM must be discarded since its internal fuses are blown permanently. For this reason, PROM is also referred to as OTP (One Time Programmable).

Programming ROM, also called burning ROM, requires special equipment called a ROM burner or ROM programmer.

2. EPROM (erasable programmable ROM) and UV-EPROM

EPROM was invented to allow making changes in the contents of PROM after it is burned.

In EPROM, one can program the memory chip and erase it thousands of times. This is especially necessary during the development of the prototype of a microprocessor-based project.

A widely used EPROM is called UV-EPROM, where UV stands for ultraviolet. The only problem with UV-EPROM is that erasing its contents can take up to 20 minutes.

All UV-EPROM chips have a window through which the programmer can shine ultraviolet (UV) radiation to erase the chip's contents. For this reason, EPROM is also referred to as UV-erasable EPROM or simply UV-EPROM.

Programming a UV-EPROM

To program a UV-EPROM chip, the following steps must be taken:

1. Its contents must be erased. To erase a chip, remove it from its socket on the system board and place it in EPROM erasure equipment to expose it to UV radiation for 5—20 minutes.
2. Program the chip. To program a UV-EPROM chip, place it in the ROM burner (programmer). To burn code or data into EPROM, the ROM burner uses 12.5 volts or higher, depending on the EPROM type. This voltage is referred to as V_{pp} in the UV-EPROM data sheet.
3. Place the chip back into its socket on the system board.

As can be seen from the above steps, not only is there an EPROM programmer (burner), but there is also separate EPROM erasure equipment.

The main problem, and indeed the major disadvantage of UV-EPROM, is that it cannot be erased and programmed while it is in the system board. To provide a solution to this problem, EEPROM was invented. '

3. EEPROM (electrically erasable programmable ROM)

EEPROM has several advantages over EPROM, such as the fact that its method of erasure is electrical and therefore instant. as opposed to the 20-minute erasure time required for UV-EPROM.

In addition, in EEPROM one can select which byte to be erased, in contrast to UV-EPROM, in which the entire contents of ROM are erased.

However, the main advantage of EEPROM is that one can program and erase its contents while it is still in the system board. it does not require physical removal of the

memory chip from its socket. In other words, unlike UV-EPROM, EEPROM does not require an external erasure and programming device.

To utilize EEPROM fully, the designer must incorporate the circuitry to program the EEPROM into the system board. In general, the cost per bit for EEPROM is much higher than for UV-EPROM.

4. Flash memory EPROM

Since the early 1990s, Flash EPROM has become a popular user-programmable memory chip. and for good reasons.

1. First, the erasure of the entire contents takes less than a second, or one might say in a flash, hence its name, Flash memory.
2. In addition, the erasure method is electrical, and for this reason, it is sometimes referred to as Flash EEPROM. To avoid confusion, it is commonly called Flash memory.

The major difference between EEPROM and Flash memory is that when Flash memory's contents are erased, the entire device is erased, in contrast to EEPROM, where one can erase a desired byte.

Although in many Flash memories recently made available the contents are divided into blocks and the erasure can be done block by block, unlike EEPROM, Flash memory has no byte erasure option.

Because Flash memory can be programmed while it is in its socket on the system board, it is widely used to upgrade the BIOS ROM of the PC. Some designers believe that Flash memory will replace the hard disk as a mass storage medium.

This would increase the performance of the computer tremendously since Flash memory is semiconductor memory with access time in the range of 100 ns compared with disk access time in the range of tens of milliseconds. For this to happen, Flash memory's program/erase cycles must become infinite, just like hard disks.

Program/erase cycle refers to the number of times that a chip can be erased and reprogrammed before it becomes unusable. At this time, the program/erase cycle is 100,000 for Flash and EEPROM, 1000 for UV-EPROM, and infinite for RAM and disks.

5. Mask ROM

Mask ROM refers to a kind of ROM in which the contents are programmed by the IC manufacturer. In other words, it is not a user-programmable ROM.

The term mask is used in IC fabrication. Since the process is costly, mask ROM is used when the needed volume is high (hundreds of thousands) and it is absolutely certain that the contents will not change.

It is common practice to use UV-EPROM or Flash for the development phase of a project, and only afier the code/data have been finalized is the mask version of the product ordered.

The main advantage of mask ROM is its cost, since it is significantly cheaper than other kinds of ROM, but if an error is found in the data/code, the entire batch must be thrown away. It must be noted that all ROM memories have 8 bits for data pins; therefore, the organization is x8.

Applications of Mask Read Only Memory (MROM)

The Mask Read-Only Memory (MROM) are used for:

- Network Operating Systems.
- Server Operating Systems.
- Storing fonts for laser printers.
- Storing sound data in electronic musical instruments.

Applications of Programmable Read Only Memory (PROM)

The Programmable ROM (PROM) are used in:

- Mobile Phones for providing User Specific Selections.
- Video game consoles
- Implantable Medical devices.
- Radio-Frequency Identification (RFID)tags.
- High definition Multimedia Interfaces(HDMI)

Applications of Erasable Programmable Read Only Memory (EPROM)

The applications of Erasable Programmable ROM (EPROM) includes:

- As program storage chip in Micro controllers.
- For debugging.
- For program development.
- As BIOS chip in computers.
- As program storage chip in modem, video card and many electronic gadgets.

Applications of Electrically Erasable Programmable Read Only Memory (EEPROM)

The applications of Electrically Erasable Programmable ROM (EPROM) includes:

- As BIOS chip in computers
- As storage for re-programmable calibration information in test-equipment.

- As storage for in-built self learning functionality in remote operated transmitters.

Applications of Flash Read Only Memory (Flash ROM)

The applications of Flash Read-Only Memory (Flash ROM) are:

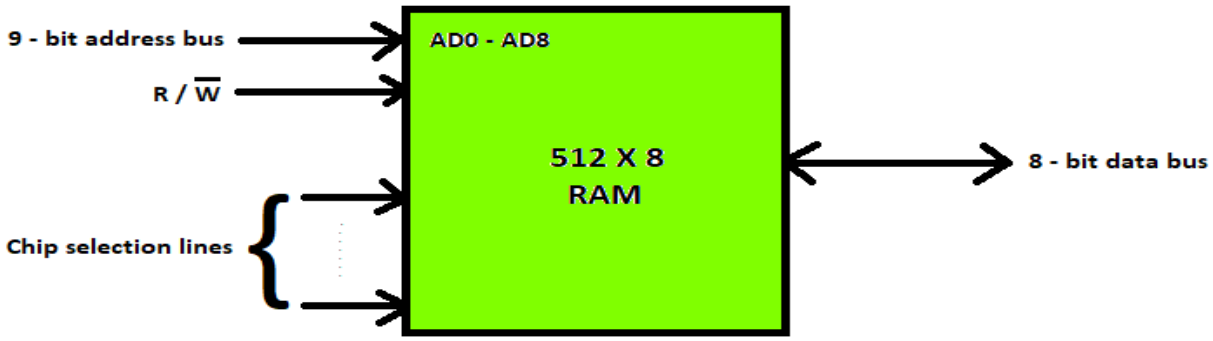
- The latest technology computers use BIOS stored on a flash memory chip, called as flash BIOS.
- Modems, pen drives, small cards use flash ROM.

RAM Architecture:

RAM(Random Access Memory) is a part of computer's Main Memory which is directly accessible by CPU. RAM is used to Read and Write data into it which is accessed by CPU randomly. RAM is volatile in nature, it means if the power goes off, the stored information is lost. RAM is used to store the data that is currently processed by the CPU. Most of the programs and data that are modifiable are stored in RAM.

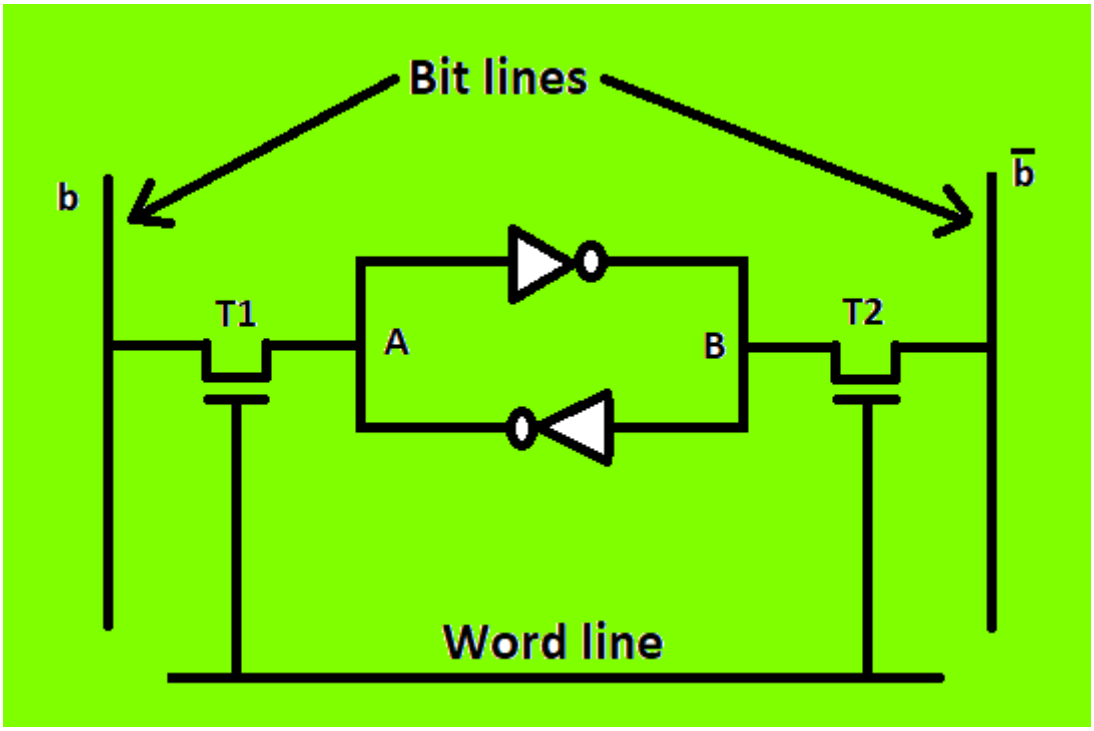
Integrated RAM chips are available in two form:

1. SRAM(Static RAM)
2. DRAM(Dynamic RAM)



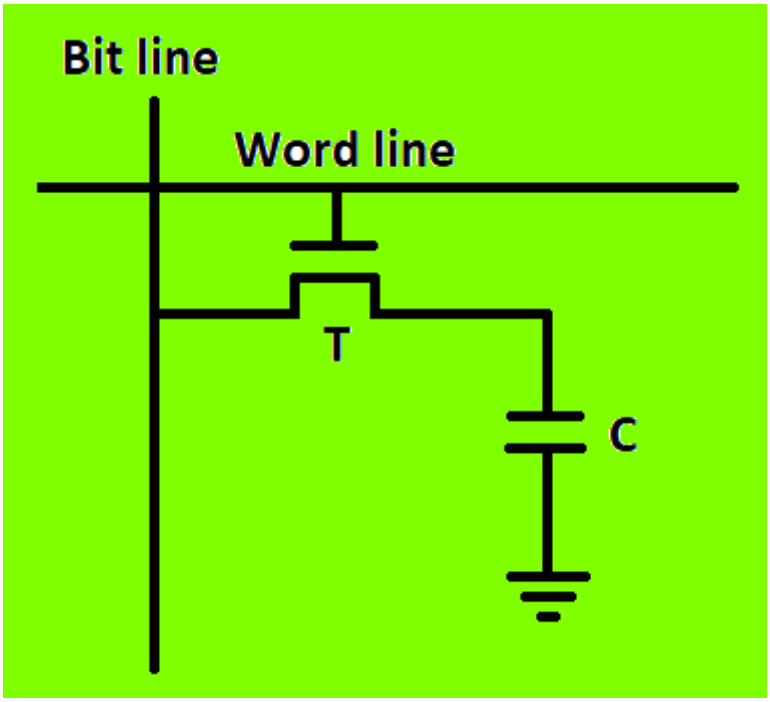
SRAM Memory Cell: Static memories(SRAM) are memories that consist of circuits capable of retaining their state as long as power is on. Thus this type of memories is called volatile memories. The below figure shows a cell diagram of SRAM. A latch is formed by two inverters connected as shown in the figure. Two transistors T1 and T2 are used for connecting the latch with two bit lines. The purpose of these transistors is to act as switches that can be opened or closed under the control of the word line, which is controlled by the address decoder. When the word line is at 0-level, the transistors are turned off and the latch remains its information. For

example, the cell is at state 1 if the logic value at point A is 1 and at point B is 0. This state is retained as long as the word line is not activated.



For **Read operation**, the word line is activated by the address input to the address decoder. The activated word line closes both the transistors (switches) T1 and T2. Then the bit values at points A and B can transmit to their respective bit lines. The sense/write circuit at the end of the bit lines sends the output to the processor.
For **Write operation**, the address provided to the decoder activates the word line to close both the switches. Then the bit value that to be written into the cell is provided through the sense/write circuit and the signals in bit lines are then stored in the cell.

DRAM Memory Cell: Though SRAM is very fast, but it is expensive because of its every cell requires several transistors. Relatively less expensive RAM is DRAM, due to the use of one transistor and one capacitor in each cell, as shown in the below figure., where C is the capacitor and T is the transistor. Information is stored in a DRAM cell in the form of a charge on a capacitor and this charge needs to be periodically recharged.
For storing information in this cell, transistor T is turned on and an appropriate voltage is applied to the bit line. This causes a known amount of charge to be stored in the capacitor. After the transistor is turned off, due to the property of the capacitor, it starts to discharge. Hence, the information stored in the cell can be read correctly only if it is read before the charge on the capacitors drops below some threshold value.



Difference between SRAM and DRAM

Below table lists some of the differences between SRAM and DRAM:

SRAM	DRAM
1. SRAM has lower access time, so it is faster compared to DRAM.	1. DRAM has higher access time, so it is slower than SRAM.
2. SRAM is costlier than DRAM.	2. DRAM costs less compared to SRAM.
3. SRAM requires constant power supply, which means this type of memory consumes more power.	3. DRAM offers reduced power consumption, due to the fact that the information is stored in the capacitor.
4. Due to complex internal circuitry, less storage capacity is available compared to the same physical size of DRAM memory chip.	4. Due to the small internal circuitry in the one-bit memory cell of DRAM, the large storage capacity is available.
5. SRAM has low packaging density.	5. DRAM has high packaging density.