# M.TECH (VLSI &ES)

## R20 HANDBOOK
## (2020-2022)

### Department of Electronics and Communication Engineering


**MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY**

**(Autonomous Institution – UGC, Govt. of India)**

Recognized under 2(f) and 12 (B) of UGC ACT 1956

(Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2015 Certified)

Maisammaguda, Dhulapally (Post Via. Kompally), Secunderabad – 500100, Telangana State, India


**MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY**
**(Autonomous Institution – UGC, Govt. of India)**
**Sponsored by CMR Educational Society**
(Affiliated to JNTU, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2015 Certified)
Maisammaguda, Dhulapally, Kompally, Secunderabad – 500100, Telangana State, India.
Contact Number: 7207034237/9133555162, E-Mail ID: mrcet2004@gmail.com, website: www.mrcet.ac.in

# MASTER OF TECHNOLOGY
# POSTGRADUATE PROGRAM

# ACADEMIC REGULATIONS
## (Batch admitted from the Academic Year 2020-2021)

*Note: The regulations hereunder are subject to amendments as may be made by the Academic Council of the College from time to time. Any or all such amendments will be effective from such date and to such batches of candidates (including those already pursuing the program) as may be decided by the Academic Council.*

## PRELIMINARY DEFINITIONS AND NOMENCLATURES

*"Autonomous Institution /College" means an institution/college designated as autonomous institute / college by University Grants Commission (UGC), as per the UGC Autonomous College Statutes.

*"Academic Autonomy" means freedom to a College in all aspects of conducting its academic programs, granted by the University for promoting excellence.

*"Commission" means University Grants Commission.

*"AICTE" means All India Council for Technical Education.

*"University" the Jawaharlal Nehru Technological University, Hyderabad.

*"College" means Malla Reddy College of Engineering & Technology, Secunderabad unless indicated otherwise by the context.

*"Program" means:

Master of Technology (M.Tech) degree program

PG Degree Program: M.Tech

*"Branch" means specialization in a program like M.Tech degree program in Electronics and Communication Engineering, M.Tech degree program in Computer Science and Engineering etc.

*"Course" or "Subject" means a theory or practical subject, identified by its course – number and course-title, which is normally studied in a semester.

*T–Tutorial, P–Practical, D–Drawing, L-Theory, C-Credits

**FOREWORD**

The autonomy is conferred on Malla Reddy College of Engineering & Technology (MRCET) by UGC based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies like UGC and AICTE. It reflects the confidence of the UGC in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards degrees on behalf of the college. Thus, an autonomous institution is given the freedom to have its own curriculum, examination system and monitoring mechanism, independent of the affiliating University but under its observance.

Malla Reddy College of Engineering & Technology (MRCET) is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, and also improving upon the values and beliefs for which it has been striving for more than a decade in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Boards of Studies are constituted with the guidance of the Governing Body of the College and recommendations of the JNTU Hyderabad to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after prolonged and detailed interaction with several experts drawn from academics, industry and research, in accordance with the vision and mission of the college which reflects the mindset of the institution in order to produce quality engineering graduates to the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications, if needed, are to be sought at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The Cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the institution and brighter prospects of engineering graduates.

***"A thought beyond the horizons of success committed for educational excellence"***

**PRINCIPAL**


# MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

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**VISION**

- To establish a pedestal for the integral innovation, team spirit, originality and competence in the students, expose them to face the global challenges and become technology leaders of Indian vision of modern society.

**MISSION**

- To become a model institution in the fields of Engineering, Technology and Management.
- To impart holistic education to the students to render them as industry ready engineers.
- To ensure synchronization of MRCET ideologies with challenging demands of International Pioneering Organizations.

**QUALITY POLICY**

- To implement best practices in Teaching and Learning process for both UG and PG courses meticulously.
- To provide state of art infrastructure and expertise to impart quality education.
- To groom the students to become intellectually creative and professionally competitive.
- To channelize the activities and tune them in heights of commitment and sincerity, the requisites to claim the never ending ladder of SUCCESS year after year.

**For more information: www.mrcet.ac.in**

## ACADEMIC REGULATIONS R-20 FOR M. TECH. (REGULAR) DEGREE COURSE

Academic Regulations of R-20 are applicable for the students of M. Tech. (Regular) Course from the Academic Year 2020-2021 and onwards. The M.Tech Degree of Malla Reddy College of Engineering & Technology (MRCET), Secunderabad shall be conferred on candidates who are admitted to the program and who fulfill all the requirements for the award of the Degree.

### 1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University (or) State Government (or) on the basis of any other order of merit as approved by the University, subject to norms as laid down by the State Govt. from time to time.

### 2.0 AWARD OF M. TECH. DEGREE

2.1. A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years.

2.2. A student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his admission, shall forfeit his seat in M. Tech. course.

2.3. The student shall register for all 66 credits and secure all the 66 credits.

2.4. The minimum instruction days in each semester are 90.

### 3.0 A. COURSE OF STUDY

The following specializations are offered at present for the M. Tech. course of study.

1. Aerospace Engineering
2. Computer Science and Engineering
3. Machine Design
4. VLSI and Embedded Systems
5. Thermal Engineering

and any other course as approved by the MRCET from time to time.

### 3.0 B. Departments offering M. Tech. Programmes with specializations are noted below:

| | |
|---|---|
| Aeronautical Engineering | Aerospace Engineering |
| Computer Science Engineering | Computer Science Engineering |
| Electronics & Communication Engineering | VLSI and Embedded Systems |
| Mechanical Engineering | Machine Design |
| Mechanical Engineering | Thermal Engineering |

**4.0 ATTENDANCE**

The programs are offered on a unit basis with each subject being considered a unit.

**4.1** A student shall be eligible to write University examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

**4.2** Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee.

**4.3** Shortage of Attendance below 65% in aggregate shall not be condoned.

**4.4** Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of that class and their registration shall stand cancelled.

**4.5** A prescribed fee as determined by the examination branch shall be payable towards condonation of shortage of attendance.

**4.6** A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

**4.7** In order to qualify for the award of the M. Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

**4.8** A student shall not be promoted to the next semester unless he satisfies the minimum academic requirements of the previous semester.

**5.0 EVALUATION**

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

For the theory subjects 70 marks shall be awarded based on the performance in the End Semester Examination and 30 marks shall be awarded based on the Internal Examination Evaluation. The internal evaluation consists of two mid-term examinations each covering descriptive paper 24 marks which consists of six questions and answers any four questions, each carrying 6 marks a total duration of 2 hours. Average of the two mid-term examinations shall be taken as the final marks secured by each candidate. Six (6) marks are allocated for Assignments (as specified by the subject teacher concerned). The total marks secured by the student in mid-term examination and assignment are evaluated for 30 marks.

However, any student scoring internal marks less than 40% will be given a chance to write the internal exam once again after he/she re-registering for the concerned subject and paying stipulated fees as per the norms.

**5.1** The end semesters examination will be conducted for 70 marks with 5 questions consisting of two questions each (a) and (b), out of which the student has to answer either (a) or (b), not both and each question carries 14 marks.

**5.2** For practical subjects, 70 marks shall be awarded based on the performance in the End Semester Examinations and 3 0 marks shall be awarded based on the day-to-day performance as Internal Marks.

**5.3** There shall be two seminar presentations during II year I semester and II semester respectively. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

**5.4** A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Examination taken together.

**5.5** In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.4) he has to reappear for the End semester Examination in that subject.

**5.6** A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and so has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the eventof the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled.

**5.7** In case the candidate secures less than the required attendance in any subject, he shall not be permitted to write the End Examination in that subject. He shall re-register the subject when next offered.

**5.8** Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher and the second examiner shall be another Laboratory Teacher.

**5.9 EVALUATION OF MAJOR PROJECT/DISSERTATION WORK**

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee for Mini Project and Major Project.

**5.10** A Project Review Committee (PRC) shall be constituted with Principal as Chairperson, Heads of all the Departments offering the M. Tech. programs and twoother senior faculty members.

**5.11** Registration of Project Work: A candidate is permitted to register for the Mini Project and Major Project after satisfying the attendance requirement of all the subjects, both theory and practical.

**5.12** After satisfying 5.11, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his Mini Project and Major Project work to the Departmental Academic Committee for approval. Only after obtaining the approval of the Departmental Academic Committee can the student initiate the Mini Project and Major Project.

**5.13** If a candidate wishes to change his supervisor or topic of the project, he can doso with the approval of the Departmental Academic Committee. However, the Departmental Academic Committee shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

**5.14** A candidate shall submit his status report in a bound-form in two stages at least with a gap of 3 months.

**5.15** The work on the Mini Project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 1 month from the date of registration of the Mini Project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal through Head of the Department and make an oral presentation before the PRC.

**5.16** The work on the Major Project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Major Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the Major Project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal through Head of the Department and make an oral presentation before the PRC.

**5.17** Three copies of the Mini Project report and Major Project Thesis certified by the supervisor shall be submitted to the College/Institute.

**5.18** The Mini Project report and Major Project thesis shall be adjudicated by one examiner selected by the University. For this, the Principal of the College shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned and head of the department.

**5.19** If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

**5.20** If the report of the examiner is favorable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report the candidate's work for a maximum of 100 marks for Mini Project and maximum 100 marks for Major Project:

The Head of the Department shall coordinate and make arrangements for the conduct of Viva- Voce examination. 50% marks are to be scored in both Mini Project and Major Project. If the candidate fails to score minimum marks, the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva- Voce examination, he will not be eligible for the award of the degree.

## 6.0 AWARD OF DEGREE AND CLASS

In assessing the performance of the students in examinations, the usual approach is to award marks based on the examinations conducted at various stages (sessional, mid-term, end-semester etc.,) in a semester. As per UGC Autonomous guidelines, the following system is implemented in awarding the grades and CGPA under the Credit Based Semester System (CBCS).

## 7.0 Letter Grades and Grade Points:

The UGC recommends a 10-point grading system with the following letter grades as given below:

| Letter Grade | Points | % of Marks secured in a subject or course (Class Intervals) |
|---|---|---|
| O (Outstanding) | 10 | Greater than or equal to 85 |
| A+(Excellent) | 9 | 75 and less than 85 |
| A(Very Good) | 8 | 65 and less than 75 |
| B+(Good) | 7 | 60 and less than 65 |
| B(Average) | 6 | 55 and less than 60 |
| C (Pass) | 5 | 50 and less than 55 |
| F(Fail) | 0 | Below 50 |
| Ab (Absent) | 0 | - |

A student obtaining Grade F shall be considered failed and will be required to reappear in the examination.

Students with final CGPA (at the end of the programme) ≥ 7.50, and shall be placed in **'first class with distinction'**.

Students with final CGPA (at the end of the programme) ≥ 6.50 but < 7.50, shall be placed in **'first class'**.

Students with final CGPA (at the end of the programme) ≥ 5.50 but < 6.50, shall be placed in **'Second class'.**

All other students who qualify for the award of the degree, with final CGPA (at the end of the programme) ≥ 5.00 but < 5.50, shall be placed in **'pass class'.**

**% of Marks = (final CGPA) x 10**

**7.1 Computation of SGPA and CGPA**

The UGC recommends the following procedure to compute the Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

**Credit points (CP) = grade point (GP) x credits …. For a course**

i. The SGPA is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e

**SGPA (Si) = Σ(Ci x Gi) / ΣCi**

where Ci is the number of credits of the ith course and Gi is the grade point scored by the student in the ith course.

ii. The CGPA is also calculated in the same manner taking into account all the courses undergone by a student over all the semesters of a programme, i.e.

**CGPA = Σ(Ci x Si) / Σ Ci**

where Si is the SGPA of the ith semester and Ci is the total number of credits in that semester.

iii. The SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

**7.2** A student obtaining 'F' grade in any subject shall be deemed to have 'failed' and is required to reappear as a 'supplementary student' in the semester end examination, as and when offered. In such cases, internal marks in those subjects will remain the same as those obtained earlier.

**7.3** A student who has not appeared for examination in any subject '**Ab'** grade will be allocated in that subject, and student shall be considered **'failed'**. Student will be required to reappear as a 'supplementary student' in the semester end examination, as and when offered.

**7.4** A letter grade does not indicate any specific percentage of marks secured by the student, but it indicates only the range of percentage of marks.

**7.5** A student earns grade point (GP) in each subject/ course, on the basis of the letter grade secured in that subject/ course. The corresponding 'credit points' (CP) are computed by multiplying the grade point with credits for that particular subject/ course.

**Credit points (CP) = grade point (GP) x credits …. For a course**

**7.6** The student passes the subject/ course only when **GP ≥ 5 ('C' grade or above)**

**Illustration of calculation of SGPA**

| Course/Subject | Credits | Letter Grade | Grade Points | Credit Points |
|---|---|---|---|---|
| Course 1 | 4 | A | 8 | 4 x 8 = 32 |
| Course 2 | 4 | O | 10 | 4 x 10 = 40 |
| Course 3 | 4 | C | 5 | 4 x 5 = 20 |
| Course 4 | 3 | B | 6 | 3 x 6 = 18 |
| Course 5 | 3 | A+ | 9 | 3 x 9 = 27 |
| Course 6 | 3 | C | 5 | 3 x 5 = 15 |
| | 21 | | | 152 |

**SGPA = 152/21 = 7.24**

**Illustration of calculation of CGPA:**

| Course/Subject | Credits | Letter Grade | Grade Points | Credit Points |
|---|---|---|---|---|
| **I Year I Semester** | | | | |
| Course 1 | 4 | A | 8 | 4 x 8 = 32 |
| Course 2 | 4 | A+ | 9 | 4 x 9 = 36 |
| Course 3 | 4 | B | 6 | 4 x 6 = 24 |
| Course 4 | 3 | O | 10 | 3 x 10 = 30 |
| Course 5 | 3 | B+ | 7 | 3 x 7 = 21 |
| Course 6 | 3 | A | 8 | 3 x 8 = 24 |

| | | | | |
|---|---|---|---|---|
| **I Year II Semester** | | | | |
| Course 7 | 4 | B+ | 7 | 4 x 7 = 28 |
| Course 8 | 4 | O | 10 | 4 x 10 = 40 |
| Course 9 | 4 | A | 8 | 4 x 8 = 32 |
| Course 10 | 3 | B | 6 | 3 x 6 = 18 |
| Course 11 | 3 | C | 5 | 3 x 5 = 15 |
| Course 12 | 3 | A+ | 9 | 3 x 9 = 27 |
| | Total Credits = 42 | | | Total Credits Points = 327 |
| | | | | |

**CGPA = 327/42 = 7.79**

**7.7** For merit ranking or comparison purposes or any other listing, **only** the **'rounded off'** values of the CGPAs will be used.

**7.8** For calculations listed in regulations 7.2 to 7.7, performance in failed subjects/ courses (securing **F** grade) will also be taken into account, and the credits of such subjects/courses will also be included in the multiplications and summations. After passing the failed subject(s) newly secured letter grades will be taken into account for calculation of SGPA and CGPA. However, mandatory courses will not be taken into consideration.

**8.0 Passing standards**

In assessing the performance of the students in examinations, the usual approach is to award marks based on the examinations conducted at various stages (sessional, mid-term, end-semester etc.,) in a semester. As per UGC Autonomous guidelines, the following system is implemented in awarding the grades and CGPA under the **Choice Based Credit System (CBCS).**

**8.1** student shall be declared successful or 'passed' in a semester, if student secures a GP $\geq 5$ ('C' grade or above) in every subject/course in that semester (i.e. when student gets an SGPA $\geq 5.00$ at the end of that particular semester); and a student shall be declared successful or 'passed' in the entire under graduate programme, only when gets a CGPA $\geq 5.00$ for the award of the degree as required.

**8.2** After the completion of each semester, a grade card or grade sheet (or transcript) shall be issued to all the registered students of that semester, indicating the letter grades and credits earned. It will show the details of the courses registered (course code, title, no. of credits, and grade earned etc.), credits earned, SGPA, andCGPA.

A student who registers for all the specified subjects/ courses as listed in the course structure and secures the required number of 88 credits (with CGPA $\geq 5.0$), within 8 academic years from the date of commencement of the first academic year, shall be declared to have 'qualified' for the award of the M.Tech. degree in the chosen branch of Engineering as selected at the time of admission.

A student who qualifies for the award of the degree as listed above shall be placed in the following classes.

Students with final CGPA (at the end of the post graduate programme) $\geq 7.50$, shall be placed in 'first class with distinction'.

Students with final CGPA (at the end of the post graduate programme) $\geq 6.50$ but $< 7.50$, shall be placed in'first class'.

Students with final CGPA (at the end of the post graduate programme) $\geq 5.50$ but $< 6.50$, shall be placed in 'Second class'.

All other students who qualify for the award of the degree (listed above), with final CGPA (at the end of the post graduate programme) $\geq 5.00$ but $< 5.50$, shall be placed in 'pass class'.

A student with final CGPA (at the end of the post graduate programme) $< 5.00$ will not be eligible for the award of the degree.

Students fulfilling the conditions listed above alone will be eligible for award of 'university rank' and 'gold medal'.

**9.0 Declaration of results**

**9.1** Computation of SGPA a**n**d CGPA are done using the procedure listed in 7.2 to 7.7.

**9.2** For final percentage of formula marks equivalent to the computed final CGPA, the following formula maybe used.

**% of Marks = (final CGPA – 0.5) x 10**

**10.0 WITHHOLDING OF RESULTS**

If the student has not paid the dues, if any, to the Institute or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be withheld in such cases.

**11.0 TRANSITORY REGULATIONS**

**11.1** Discontinued, detained, or failed candidates are eligible for admission to two earlier or equivalent subjects at a time as and when offered.

**12. GENERAL**

12.1 Wherever the words he, him, his, occur in the regulations, they include she, her, hers.

12.2 The academic regulation should be read as a whole for the purpose of any interpretation.

12.3 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council of the College is final.

12.4 The College may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Academic Council of the College/Affiliating University.

## MALPRACTICES RULES

**DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS**

| S.No | Nature of Malpractices/Improper conduct | Punishment |
|---|---|---|
| | ***If the candidate:*** | |
| 1. (a) | Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination) | Expulsion from the examination hall and cancellation of the performance in that subject only. |
| (b) | Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter. | Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him. |
| 2. | Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing. | Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University. |
| 3. | Impersonates any other candidate in connection with the examination. | The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The |

| | | |
|---|---|---|
| | | performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him. |
| 4. | Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination. | Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. |
| 5. | Using objectionable, abusive or offensive | Cancellation of the performance |

| | | |
|---|---|---|
| | language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks. | in that subject. |
| 6. | Refuses to obey the orders of the Chief Superintendent/Assistant Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-incharge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination. | In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them. |
| 7. | Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall. | Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic |

| | | |
|---|---|---|
| | | regulations in connection with forfeiture of seat. |
| 8. | Possess any lethal weapon or firearm in the examination hall. | Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. |
| 9. | If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8. | Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate hasalready appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them. |
| 10. | Comes in a drunken condition to the examination hall. | Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the |

| | | |
|---|---|---|
| | | subjects of that semester/year. |
| 11. | Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny. | Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations. |
| 12. | If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment. | |

**Malpractices identified by squad or special invigilators**

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)

i. A show cause notice shall be issued to the college.
ii. Impose a suitable fine on the college.
iii. Shifting the examination centre from the college to another college for a specific period of not less than one year.

* * * * *

# MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
## (AUTONOMOUS)
### M. Tech –(VLSI & Embedded Systems)

## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
## M.TECH – VLSI & EMBEDDED SYSTEMS
## R20 COURSE STRUCTURE

**I Year I Semester**

| S.NO. | SUBJECT CODE | SUBJECT | L | T/P/D | C | MAX MARKS | |
|---|---|---|---|---|---|---|---|
| | | | | | | INT | EXT |
| 1 | R20D6801 | RTL Simulation and Synthesis with PLDs | 3 | - | 3 | 30 | 70 |
| 2 | R20D6802 | Embedded System Design | 3 | - | 3 | 30 | 70 |
| 3 | R20D6803<br>R20D6804<br>R20D6805 | ELECTIVE-I<br>1.CMOS Analog IC DesignR20<br>2.Programming Languages for Embedded S/W<br>3.VLSI Signal Processing | 3 | - | 3 | 30 | 70 |
| 4 | R20D6806<br>R20D6807<br>R20D6808 | ELECTIVE-II<br>1.CMOS Digital IC Design<br>2.CAD of Digital System<br>3.System Design with Embedded Linux | 3 | - | 3 | 30 | 70 |
| 5 | R20DHS53 | Research Methodology | 3 | - | 3 | 30 | 70 |
| 6 | R20D6809 | Lab 1: RTL Simulation and Synthesis with PLDs | - | 3 | 2 | 30 | 70 |
| 7 | R20D6810 | Lab 2: ES Lab | - | 3 | 2 | 30 | 70 |
| 8 | R20DHS54 | Audit Course I - Value Education | 2 | - | - | 50 | - |
| Total | | | 17 | 6 | 19 | 260 | 490 |

*Audit course: Non-credit course, 50% of scoring is required for the award of the degree

**I Year II Semester**

| S.NO. | SUBJECT CODE | SUBJECT | L | T/P/D | C | MAX MARKS | |
|---|---|---|---|---|---|---|---|
| | | | | | | INT | EXT |
| 1 | R20D6811 | CMOS Mixed Signal Circuit Design | 3 | - | 3 | 30 | 70 |
| 2 | R20D6812 | Embedded RTOS | 3 | - | 3 | 30 | 70 |
| 3 | R20D6813<br>R20D6814<br>R20D6815 | ELECTIVE – III<br>1.Low Power VLSI Design<br>2.SOC Design<br>3.Memory Technologies | 3 | - | 3 | 30 | 70 |
| 4 | R20D6816<br>R20D6817<br>R20D6818 | ELECTIVE- IV<br>1.Physical Design Automation<br>2.Communication Buses and Interfaces<br>3. Multimedia Signal Coding | 3 | - | 3 | 30 | 70 |
| 5 | R20D6819 | Mini Project | 3 | - | 3 | 30 | 70 |
| 6 | R20D6820 | Lab 1: CMOS Mixed Signal Circuit Design Lab | - | 3 | 2 | 30 | 70 |
| 7 | R20D6821 | Lab 2: Embedded RTOS Lab | - | 3 | 2 | 30 | 70 |
| 8 | R20DHS55 | Audit Course II - English for Research Paper Writing | 2 | - | - | 50 | |
| Total | | | 17 | 6 | 19 | 260 | 490 |

*Audit course: Non-credit course, 50% of scoring is required for the award of the degree

# MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
## (AUTONOMOUS)
### M. Tech –(VLSI & Embedded Systems)

**II Year I Semester**

| S.NO. | SUBJECT CODE | SUBJECT | L | T/P/D | C | MAX MARKS | |
|---|---|---|---|---|---|---|---|
| | | | | | | INT | EXT |
| 1 | R20D6822<br>R20D6823<br>R20D6824 | (1)Communication Network<br>(2)Selected Topics in Mathematics<br>(3)Nano materials and Nanotechnology | 3 | - | 3 | 30 | 70 |
| 2 | OE | OE | 3 | - | 3 | 30 | 70 |
| 3 | R20D6825 | Dissertation Phase 1 | - | - | 8 | 100 | - |
| Total | | | 6 | - | 14 | 160 | 140 |

**II Year II Semester**

| S.NO. | SUBJECT CODE | SUBJECT | L | T/P/D | C | MAX MARKS | |
|---|---|---|---|---|---|---|---|
| | | | | | | INT | EXT |
| 1 | R20D6826 | Dissertation Phase 2 | - | - | 14 | 100 | 200 |
| Total | | | - | - | 14 | 100 | 200 |

| OPEN ELECTIVE | |
|---|---|
| Subject Code | Subject Name |
| R20DME51 | Non-Conventional Energy Sources |
| R20DME52 | Industrial Safety |
| R20DME53 | Operations Research |
| R20DHS51 | Business Analytics |
| R20DCS51 | Scripting Languages |
| R20DAE51 | Mathematical Modeling Techniques |
| R20DEC51 | Embedded Systems Programming |

# RTL SIMULATION AND SYNTHESIS WITH PLDS

**Course Objectives:**

- To learn High-Level Design Methodology and overview of design flow
- To learn the coding skills relevant to synthesis of logic circuits.
- To understand importance of libraries in synthesis flow
- To design logic to meet specifications and optimization
- To understand the design constrains related to FSM

**Unit I**

**High-Level Design Methodology Overview:** ASIC Design Flow Using Synthesis, HDL Coding, RTL Behavioral and Gate-Level Simulation, Logic Synthesis, Design for Testability, Design Re-Use, Behavioral Synthesis & Concepts. Design Analyzer and Design compiler, Target Library, Link Library, and Symbol Library, Cell names, Instance names, and VHDL Libraries in the Synthesis Environment, Synthesis, Optimization and Compile, Classic Scenarios

**Unit II**

**VHDL/Verilog Coding for Synthesis:** General HDL Coding Issues, VHDL vs. Verilog: The Language Issue, Finite State Machines, HDL Coding Examples, Classic Scenarios.

**Unit III**

**Links to Layout,** Motivation for Links to Layout Floor planning, Link to Layout Flow Using Floorplan Manager, Creating Wire Load Models After Back-Annotation Re-Optimizing Designs After P&R. Design for Testability: Introduction to Test Synthesis, Test Synthesis Using Test Compiler

**Unit IV**

**Constraining and Optimizing Designs:** Synthesis Background, Clock Specification for Synthesis, Design Compiler Timing Reports, Commonly Used Design, Compiler Commands, Strategies for Compiling Designs, Typical Scenarios When Optimizing Designs, Guidelines for Logic Synthesis, Classic Scenarios.

**Unit V**

**Constraining and Optimizing Designs for FSM:** Finite State Machine (FSM) Synthesis, Fixing Min Delay Violations Technology Translation, Translating Designs with Black-Box Cells, Pad Synthesis, Classic Scenarios

**Text Book**

1. Kurup Pran, Taher Abbasi, Logic Synthesis using Synopsys, 2/e, Pearson Education, 2007.

**References**

1. VHDL for Logic Synthesis, Third Edition. Andrew Rushton. © 2011 John Wiley & Sons, Ltd. Published 2011 by John Wiley & Sons, Ltd.

2. Weng Fook Lee, VHDL Coding and Logic Synthesis with Synopsys, Academic Press, 2000
3. Morris Mano, Michael D. Ciletti, Digital Design , 4/e, Prentice Hall of India, 2008
4. Himanshu Bhatnagar, Advanced ASIC Chip Synthesis, Springer Science, 2013

**Course Outcomes:**

After successful completion of the course, the student will be able to

- Understand Synthesis Flow and Optimization
- Understand Synthesizable Coding Concepts
- Analyze Physical Design Concepts
- Understand Efficient Way of Giving Constrains
- Analyze Constraining and Optimizing Designs For FSM

# EMBEDDED SYSTEM DESIGN

**Course Objectives:**

- Discuss the basic principles of ARM system design.
- Identify the major hardware components ARM data path architecture.
- Identify the design issues ARM based embedded system with the basic knowledge of firmware, embedded OS & ARM architectures.
- Analyze the execution of instructions/program knowing the basic principles of ARM architecture and assembly language.
- Compare programs written in C & assembly to execute on ARM platform.

**UNIT –I:**

**ARM Architecture:**

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and

Vector Table, Architecture Revision, ARM Processor Families.

**UNIT –II:**

**ARM Programming Model – I:**

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions,

PSR Instructions, Conditional Instructions.

**UNIT –III:**

**ARM Programming Model – II:**

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions,

Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

**UNIT –IV:**

**ARM Programming:**

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

**UNIT –V:**

**Memory Management:**

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access

Permissions, Context Switch.

**TEXT BOOKS:**

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N.

Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

2. Professional Embedded ARM development-James A Langbridge, Wiley/Wrox

**REFERENCE BOOKS:**

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes

/ Cole, 1999, Thomas Learning.

2.ARM System on Chip Architecture, Steve Furber, 2nd Edition, Pearson

**Course Outcomes:**

- Become aware of the ARM Processor, Architecture, Registers, Instruction pipeline, Interrupts and Instructions, Addressing modes and conditional instructions.
- Apply and analyze the applications in various processors and domains of embedded system.
- Ability to use advanced controllers using thumb instruction for embedded system design.
- Analyze and develop embedded hardware and software development cycles and tools.
- Understanding the concept of Memory management unit, integration methods and hardware and software design concepts associated with processor in Embedded Systems.

# ELECTIVE-I

# CMOS ANALOG IC DESIGN

**Course Objectives:**

- To provide in-depth understanding of different types of MOS devices and modeling techniques
- To understand and design the operation of current mirror circuits
- To demonstrate the analysis and design of amplifiers using CMOS
- To design a various stages of Operational amplifiers using CMOS devices.
- Design and construct the open loop and discrete time comparators using op-amp.

**UNIT -I**

**MOS Devices and Modeling:**

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOSDevice Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model forthe MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

**UNIT -II**

**Analog CMOS Sub-Circuits:**

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Currentmirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current andVoltage References, Band gap Reference.

**UNIT –III**

**CMOS Amplifiers**

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

**UNIT –IV**

**CMOS Operational Amplifiers**

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAmp.

**UNIT –V**

**Comparators**

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

**TEXT BOOKS:**

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University

Press, International Second Edition/Indian Edition, 2010.

2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and

R. G. Meyer, Wiley India, Fifth Edition, 2010.

**REFERENCE BOOKS:**

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.

2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

3. CMOS: Circuit Design, Layout and Simulation- Baker, Li

**Course Outcomes:**

- Model various components in CMOS process to estimate their performance in circuits.
- Analyze and design of MOS and different current mirror circuits including Wilson, cascode current mirror.
- Design of CMOS Amplifiers including Differential, Cascode and high gain amplifier architectures.
- Design of CMOS Operational amplifiers and to measure the characteristics of cascode operational-amplifier.
- Apply and analyze the performance of open loop and discrete time capacitor circuits

# ELECTIVE-I

# PROGRAMMING LANGUAGES FOR EMBEDDED S/W

**UNIT I:Embedded 'C' Programming:** Bitwise operations, Dynamic memory allocation, OS services, Linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code optimization issues, Writing LCD drives, LED drivers, Drivers for serial port communication, Embedded Software Development Cycle and Methods (Waterfall, Agile)

**UNIT II: Object Oriented Programming:** Introduction to procedural, modular, object-oriented and generic programming techniques,

Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

**UNIT III: CPP Programming:** 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

**UNIT IV: Overloading, Inheritance & Templates:** Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions

**Templates**

Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.

**UNIT V: Scripting Languages:** Overview of Scripting Languages – PERL, CGI, VB Script, Java Script, PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

**TEXT BOOKS:**

1. Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008

2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011

3. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002

4. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999

5. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey

& Sons, 2005

**Course Outcomes:**

At the end of this course, students will be able to

- Write an embedded C application of moderate complexity.
- Develop and analyze algorithms in C++.

Differentiate interpreted languages from compiled languages.

# ELECTIVE-I

# VLSI SIGNAL PROCESSING

**UNIT I:**

**Introduction to DSP Systems, Pipelining And Parallel Processing Of FIR Filters**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

**UNIT II:**

**Retiming, Algorithmic Strength Reduction**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

**UNIT III:**

**Fast Convolution, Pipelining and Parallel Processing Of IIR Filters**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

**UNIT IV:**

**Bit-Level Arithmetic Architectures**

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

**UNIT V:**

**Numerical Strength Reduction, Synchronous, Wave and Asynchronous Pipelining**

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

**References:**


- Keshab K. Parthi[A1] , VLSI Digital signal processing systems, design and implementation[A2] , Wiley, Inter Science, 1999.
- Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
- S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985


**Course Outcomes:**

At the end of this course, students will be able to

- Acquired knowledge about DSP algorithms, its DFG representation, pipelining and parallel processing approaches.

  Ability to acquire knowledge about retiming techniques, folding and register minimization path problems.

- Ability to have knowledge about algorithmic strength reduction techniques and parallel processing of FIR and IIR digital filters.

Acquired knowledge about finite word-length effects and round off noise computation in DSP systems.

# ELECTIVE-II

# CMOS DIGITAL IC DESIGN

## Course Objectives:

- To discuss basic CMOS logic gates, implementation of AOI and OAI gates
- Design MOS logic circuits using Transmission gates
- To analyze different delays and power dissipation in number of stages.
- To understand the design of combinational circuits using ratioed, cascade and dynamic logic.
- To design different types of Semiconductor Memories

**UNIT –I:**

**MOS Design:**

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage,Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates,Transistor equivalency, CMOS Inverter logic.

**UNIT –II:**

**Combinational MOS Logic Circuits:**

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

**UNIT –III:**

**Sequential MOS Logic Circuits:**

Behavior of Bi-stable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered Flip-flop.

**UNIT –IV:**

**Dynamic Logic Circuits:**

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOST Transmission gate logic, High performance Dynamic CMOS circuits.

**UNIT –V:**

**Semiconductor Memories:**

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell andrefresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash andNAND flash.

**TEXT BOOKS:**

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.

2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,

TMH, 3 rd Ed., 2011.

**REFERENCE BOOKS:**

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC

Press, 2011

2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan,

Borivoje Nikolic, 2 nd Ed., PHI.

**Course Outcomes:**

- Able to apply mathematical methods and transistor physics in the analysis of CMOS circuits and design CMOS inverter with different loads for given levels noise margin's and propagation delay's.
- Can execute moderately sized digital logic designs with OAI, AOI, and transmission gates.
- Able to design static and dynamic CMOS circuits (both Combinational and sequential) at transistor level and layout level.
- Able to design memory architectures that aids the growth of VLSI designs with reduced access time and reduced power consumption.

# ELECTIVE-II

# CAD OF DIGITAL SYSTEM

**UNIT I**

**VLSI Design Methodologies**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

**UNIT II**

**Design Rules**

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

**UNIT III**

**Floor Planning**

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

**UNIT IV:**

**Simulation**

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

**UNIT V:**

**Modelling And Synthesis**

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

**TEXT BOOKS:**

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002. 2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002

# ELECTIVE-II

# SYSTEM DESIGN WITH EMBEDDED LINUX

**UNIT I: Embedded OS (Linux) Internals :**Linux internals: Process Management, File Management, Memory Management, I/O Management. Overview of POSIX APIs, Threads – Creation, Cancellation, POSIX Threads Inter Process Communication - Semaphore, Pipes, FIFO, Shared Memory Kernel: Structure, Kernel Module Programming Schedulers and types of scheduling.

Interfacing: Serial, Parallel Interrupt Handling Linux Device Drivers: Character, USB, Block & Network

**UNIT II: Open source RTOS:** Basics of RTOS: Real-time concepts, Hard Real time and Soft Real-time, Differences between General Purpose OS & RTOS, Basic architecture of an RTOS, Scheduling Systems, Inter-process communication, Performance Metric in scheduling models, Interrupt management in RTOS environment, Memory management, File systems, I/O Systems, Advantage and disadvantage of RTOS.

**UNIT III: Open Source RTOS Issues:** POSIX standards, RTOS Issues - Selecting a Real Time Operating System, RTOS comparative study. Converting a normal Linux kernel to real time kernel, Xenomai basics, Overview of Open source RTOS for Embedded systems (Free RTOS/ Chibios-RT) and application development.

**UNIT IV: VxWorks / Free RTOS:** VxWorks/ Free RTOS Scheduling and Task Management - Realtime scheduling, Task Creation, Intertask Communication, Pipes, Semaphore, Message Queue, Signals, Sockets, Interrupts I/O Systems - General Architecture, Device Driver Studies, Driver Module explanation, Implementation of Device Driver for a peripheral

**UNIT V: Case study:** Cross compilers, debugging Techniques, Creation of binaries & porting stages for Embedded Development board (Beagle Bone Black, Rpi or similar), Porting an Embedded OS/ RTOS to a target board ().Testing a real time application on the board

**TEXT BOOKS:**

1. Essential Linux Device Drivers, Venkateswaran Sreekrishnan

2. Writing Linux Device Drivers: A Guide with Exercises, J. Cooperstein

3. Real Time Concepts for Embedded Systems – Qing Li, Elsevier

**Reference Books:**

1. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill

2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK

3. Software Design for Real-Time Systems: Cooling, J E Proceedings of 17the IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society

4. Real-time Systems – Jane Liu, PH 2000

5. Real-Time Systems Design and Analysis : An Engineer's Handbook: Laplante, Phillip A

6. Structured Development for Real - Time Systems V1 : Introduction and Tools: Ward, Paul T & Mellor, Stephen J

7. Structured Development for Real - Time Systems V2 : Essential Modeling Techniques: Ward, Paul T & Mellor, Stephen J

8. Structured Development for Real - Time Systems V3 : Implementation Modeling Techniques: Ward, Paul T & Mellor, Stephen J

9. Monitoring and Debugging of Distributed Real-Time Systems: TSAI, Jeffrey J P & Yang, J H

10. Embedded Software Primer: Simon, David E.

11. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw

Hill

# RESEARCH METHODOLOGY

**Course Objectives:**

- To familiarize the meaning, objectives and sources of research
- To acquaint the student with the importance and methods of literature review/research ethics
- To impart the knowledge of data collection and analysis of data
- To understand the procedure for Hypothesis testing and writing Research proposals

**UNIT - I**

Introduction: Research objective and motivation, Types of research, Research approaches, Significance, Research method vs. methodology, Research process.

**UNIT - II**

Formulating a research problem: Literature review, Formulation of objectives, Establishing Operational definitions, Identifying variables, constructing hypotheses.

**UNIT - III**

Research design and Data Collection: Need and Characteristics, Types of research design, Principles of Experimental research design, Method of data collection, Ethical issues in collecting data.

**UNIT - IV**

Sampling and Analysis of data: Need of Sampling, Sampling distributions, Central limit theorem, Estimation: mean and variance, Selection of sample size Statistics in research, Measures of Central tendency, Dispersion, asymmetry and relationships, Correlation and Regression analysis, Displaying data

**UNIT - V**

Hypothesis Testing: Procedure, Hypothesis testing for difference in mean, variance limitations, Chi-square test, Analysis of variance (ANOVA), Basic principles and techniques of writing a Research Proposal

**Text Books:**

1. R. C. Kothari, Research Methodology: Methods and Techniques, 2nd edition, New Age International Publisher, 2009
2. Ranjit Kumar, Research Methodology: A Step-by-Step Guide for Beginners, 2nd Edition, SAGE, 2005

References:

1. Trochim, William M. The Research Methods Knowledge Base, 2nd Edition. Internet WWW

page, at URL: <http://www.socialresearchmethods.net/kb/>
2. (Electronic Version): StatSoft, Inc. (2012). Electronic Statistics Textbook. Tulsa, OK: StatSoft. WEB: http://www.statsoft.com/textbook/.(Printed Version): Hill, T. & Lewicki, P. (2007). STATISTICS: Methods and Applications. StatSoft, Tulsa, OK.

**Course Outcomes:**

- Develop understanding on various kinds of research, objectives of doing research, research process, research designs and sampling.
- Identify appropriate research topics.
- Select and define appropriate research problem and parameters.
- Analyze the data collected and conduct research in a more appropriate manner.
- Have basic awareness of data analysis-and hypothesis testing procedures.

# LAB 1

## RTL SIMULATION AND SYNTHESIS WITH PLDS

**List of Experiments:**

1) Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2) Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3) Vending machines - Traffic Light controller, ATM, elevator control.
4) PCI Bus & arbiter and downloading on FPGA.
5) UART/ USART implementation in Verilog.
6) Realization of single port SRAM in Verilog.
7) Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.

   Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

**Course Outcomes:**

At the end of the laboratory work, students will be able to:

- Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.

  Use EDA tools like Cadence, Mentor Graphics and Xilinx.

# LAB 2: ES LAB

**Note:**
The following programs are to be implemented on ARM based Processors/Equivalent.
Minimum of 10 programs are to be conducted.

**The following Programs are to be implemented on ARM Processor**
1. Simple Assembly Program for a. Addition | Subtraction | Multiplication | Division
b. Operating Modes, System Calls and Interrupts
c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

**Course Outcomes:**

- To gain the working knowledge of various embedded tools.
- To develop sample programs to be implemented on ARM based Processors or equivalent.
- Create applications for using the ARM Processor on IDE Environment using RAM Tool chain & Library.
- Develop applications using the concept of Interfacing.
- Design advanced embedded applications using ARM Processor.

# AUDIT COURSE I

# VALUE EDUCATION

**Course Objectives:**

- To expose the student to need for values, ethics, self-development and standards
- To make the student understand the meaning of different values including duty, devotion, self-reliance etc.
- To imbibe the different behavioral competencies in students for leading an ethical and happy life
- To expose the student to different characteristic attributes and competencies for leading a successful, ethical and happy profession life

**UNIT I:**

**Values and self-development**

Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non-moral valuation. Standards and principles, Value judgements

**UNIT II:**

**Importance of cultivation of values**

Sense of duty, Devotion, Self-reliance, Confidence, Concentration, Truthfulness, Cleanliness, Honesty, Humanity. Power of faith, National Unity, Patriotism, Love for nature, Discipline

**UNIT III:**

**Personality and Behavior Development**

Soul and Scientific attitude, Positive Thinking, Integrity and discipline, Punctuality, Love and Kindness ,Avoid fault Thinking, Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship, Happiness Vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature

**UNIT IV:**

**Character and Competence**

Holy books vs Blind faith, Self-management and Good health, Science of reincarnation, Equality, Nonviolence ,Humility, Role of Women, All religions and same message, Mind your Mind, Self-control, Honesty, Studying effectively

**TEXT BOOKS:**

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

**Course Outcomes:**

- Appreciate the need for human values and methods for self-development
- Elaborate the different traits and benefits of a self-developed individual
- List the different attributes of self-developed individual
- Elaborate the role and scope of books/faith/health/religions in character building and competence development

# CMOS MIXED SIGNAL CIRCUIT DESIGN

**Course Objectives:**

- To study the fundamentals of switched capacitor circuits and filters
- To know the basics of PLL and jitter circuits
- To understand the design and performance measures of data converter fundamentals
- To describe and demonstrate the various techniques for Nyquist Rate A/D Converters
- To design the performance of different over sampling converters

**UNIT -I:**
**Switched Capacitor Circuits:**
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing,biquad filters.

**UNIT -II:**
**Phased Lock Loop (PLL):**
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency
detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities,Jitter in PLLs, Delay locked loops, applications

**UNIT -III:**
**Data Converter Fundamentals:**
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

**UNIT -IV:**
**Nyquist Rate A/D Converters:**
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

**UNIT -V:**
**Oversampling Converters:**
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

**TEXT BOOKS:**

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press,International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

**REFERENCE BOOKS:**
1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche,Kluwer Academic Publishers, 2003

2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

**Course Outcomes:**

- Understand the fundamentals of switched capacitor and biquad filter circuits.
- Design of Phase Locked Loop including charge pump, jitter and delay locked loop circuits.
- Design, Apply and analyze the performance of D/A converters including Binary-Scaled,Thermometer and Hybrid converters.
- Analyze the performance of noise shaping, Decimating, interpolating filters and higher order modulators
- Design of Successive approximation, Folding, Pipelined A/D, Time-interleaved and nyquist rate A/D Converters.

# EMBEDDED REAL TIME OPERATING SYSTEMS

**Course Objectives**:

- Understand issues in Real Time Operating Systems
- Analyze the importance of deadlines and concept of task scheduling.
- To understand and design Real Time Operating Systems which are backbone of embedded industry.

**UNIT – I:**
**Introduction**
Introduction to UNIX/LINUX, Overview of Commands, File I/O,( open, create, close, lseek, read,write), Process Control ( fork, vfork, exit, wait, waitpid, exec.

**UNIT - II:**
**Real Time Operating Systems**
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS,Defining a Task asks States and Scheduling, Task Operations, Structure, Synchronization,
**Communication and Concurrency.**
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage,
Operations and Use

**UNIT - III:**
**Objects, Services and I/O**
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

**UNIT - IV:**
**Exceptions, Interrupts and Timers**
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

**UNIT - V:**
**Case Studies of RTOS**
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

**TEXT BOOKS:**
1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011
**REFERENCE BOOKS:**
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

**Course Outcomes:**

- Explain fundamental principles for programming of real time systems with time and resource limitations.
- Exposing the major differentials of RISC and CISC architectural characteristics.
- Account for how real time operating systems are designed and functions.
- Use real time system programming languages and real time operating systems for real time applications.
- The students can implement the RTOS development tools in building real time embedded systems.

# ELECTIVE – III

# LOW POWER VLSI DESIGN

**Course Objectives:**

- To understand the sources of Power dissipation
- Analyze the Low power design approaches
- Understand the System Level, Circuit Level, Mask level Measures.
- Interpret and understand the design of various Low power circuits

**UNIT –I:**
**Fundamentals:**
Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation ,Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.
**UNIT –II:**
**Low-Power Design Approaches:**
Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.
**Switched Capacitance Minimization Approaches:**
System Level Measures, Circuit Level Measures, Mask level Measures.
**UNIT –III:**
**Low-Voltage Low-Power Adders:**
Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques–Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.
**UNIT –IV:**
**Low-Voltage Low-Power Multipliers:**
Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.
**UNIT –V:**
**Low-Voltage Low-Power Memories:**
Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.
**TEXT BOOKS:**
1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

**REFERENCE BOOKS:**

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons,2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

**Course Outcomes:**

- Able to spot and estimate the sources of power dissipation in a given circuit.
- Analyze and Design low power circuits with various circuit techniques and architectural approaches.
- Design and put forward the Architectures of adders and multipliers for low power design.
- Choose different types of memory elements for low power applications.

# ELECTIVE – III

# SOC DESIGN

**UNIT I:**

**ASIC**

Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

**UNIT 2:**

**NISC**

NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

**UNIT III:**

**Simulation**

Different simulation modes, behavioural, functional, static timing, gate level, switch level,transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

**UNIT IV:**

**Low power SoC design / Digital system**

Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS),building block optimization, building block memory, power down techniques, power consumption verification.

**UNIT V:**

**Synthesis**

Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph,Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis, Single core and Multi core systems, dark silicon issues,HDL coding techniques for minimization of power consumption, Fault tolerant designs.Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

**TEXT BOOKS:**

1.Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006
3. RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000
4. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
5. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley,2011

# ELECTIVE – III

# MEMORY TECHNOLOGIES

**UNIT I:**

**Random Access Memory Technologies**

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures,Application Specific SRAMs.

**Unit II:**

**DRAM DESIGN**

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs.SRAM and DRAM Memory controllers.

**Unit III:**

**Non-Volatile Memories**

Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

**Unit IV:**

**Semiconductor Memory Reliability and Radiation Effects**

General Reliability Issues,RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation

**Unit V:**

**Advanced Memory Technologies and High-density Memory Packing Technologies**

Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices, Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards,High Density Memory Packaging

**TEXT BOOKS:**

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience
2. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition
3. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability , PHI

# ELECTIVE- IV
# PHYSICAL DESIGN AUTOMATION

**UNIT I:**

**Introduction to VLSI Design Methodologies**

Design and Fabrication of VLSI Devices, Fabrication Process and its impact on Design.

**UNIT II:**

**VLSI design automation tools**

Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

**UNIT III:**

**General purpose methods for combinational optimization**

Partitioning, floor planning and pin assignment, placement, routing. Concepts and Algorithms Modeling: Gate Level Modeling and Simulation, Switch level modeling and simulation, Basic issues and Terminology, Binary – Decision diagram, Two – Level Logic Synthesis.

Hardware Models: Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High – level Transformations.

**Unit 4:**

Simulation

Logic synthesis, verification, high level Synthesis. FPGA technologies: Physical Design cycle for FPGA's partitioning and routing for segmented and staggered models

**UNIT V:**

**MCM technologies**

MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing –Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, routing and programmable MCM's.

TEXT BOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", John Wiley 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation" 3rd edition, Springer International Edition. REFERENCES 1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI" Wiley,1993 2. Wayne Wolf, "Modern VLSI Design: Systems on silicon" Pearson Education Asia, 2nd Edition.

# ELECTIVE- IV
# COMMUNICATION BUSES AND INTERFACES

**Unit 1:**
Serial Buses: Physical interface, Data and Control signals, features

**Unit 2:**
Limitations and applications of RS232, RS485, I2C, SPI

**Unit 3:**
CAN Architecture, Data transmission, Layers, Frame formats, applications

**Unit 4:**
PCIe - Revisions, Configuration space, Hardware protocols, applications

**Unit 5:**
USB - Transfer types, enumeration, Descriptor types and contents, Device driver
Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

TEXT BOOKS:
1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ”, Lakeview Research, 2nd Edition
2.Jan Axelson, “USB Complete”, Penram Publications
3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press
4. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 – 200x

# ELECTIVE- IV
# MULTIMEDIA SIGNAL CODING

**Course Objectives:**

- To provide an introduction to the fundamental principles and techniques in Multimedia signal
  - coding and compression.
  - To give an overview of current multimedia standards and technologies.
  - To provide techniques related to computer and multimedia networks.
  - To provide knowledge related to Multimedia network communications and applications.

**UNIT-I:**

**Introduction to Multimedia**

Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.

**Color in Image and Video:** Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Out-of-Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model.

**UNIT-II:**

**Video Concepts:** Types of Video Signals, Analog Video, Digital Video.

**Audio Concepts:** Digitization of Sound, Quantization and Transmission of Audio.

**UNIT-III:**

**Compression Algorithms**

**Lossless Compression Algorithms:** Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.

**Lossy Image Compression Algorithms:** Transform Coding: KLT And DCT Coding, Wavelet Based Coding.

**Image Compression Standards:** JPEG and JPEG2000.

**UNIT-IV:**

**Video Compression Techniques**

Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and InterFrame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

**UNIT-V:**

Audio, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

**TEXT BOOKS:**

1. Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI, 2010.
2. Multimedia Signals & Systems – Mrinal Kr. Mandal Springer International Edition 1st Edition, 2009.

**REFERENCE BOOKS:**

1. Multimedia Communication Systems – Techniques, Stds & Netwroks K.R. Rao, Zorans. Bojkoric, Dragorad A. Milovanovic, 1st Edition, 2002.
2. Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition, 2009.
3. Multimedia Systems John F. Koegel Bufond Pearson Education (LPE), 1st Edition, 2003.
4. Digital Video Processing – A. Murat Tekalp, PHI, 1996.

Video Processing and Communications – Yaowang, Jorn Ostermann, Ya-QinZhang, Pearson, 2002

## LAB 1: CMOS MIXED SIGNAL CIRCUIT DESIGN LAB

## List of Experiments:

1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
   a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
   b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
   c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
   d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV
      To extract Vth use the following procedure.
      i. Plot gm vs VGS using NGSPICE and obtain peak gm point.
      ii. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice.
      iii. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
   f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.

   Tabulate your result according to technologies and comment on it.

2) Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
   a) Perform the following
      i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
      ii. Plot VTC for CMOS inverter with varying VDD.
      iii. Plot VTC for CMOS inverter with varying device ratio.
   b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF)
   c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k)

3) Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.

4) Perform the following
   a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and

0.13um process.

b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.

i. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2. Calculate input bias voltage if bias current=50uA.

iii. Use Ngspice and obtain the bias current. Compare its value with 50uA.

iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).

v. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW

vi. Use Ngspice to determine input voltage range of the amplifier

5) Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA.

Note: Adjust accuracy options of the simulator (setup->options in GUI).

Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

i. Draw the schematic of op-amp macro model.

ii. Draw the schematic of INA.

iii. Obtain parameters of the op-amp macro model such that

a. low-frequency voltage gain = $5x10^4$,

b. unity gain BW (fu) = 500KHz,

c. input capacitance=0.2pF,

d. output resistance = ,

e. CMRR=120dB

iv. Draw schematic diagram of CMRR simulation setup.

v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.

6) Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Microwind.

a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.

b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.

c) Use extracted netlist and obtain $t_{PHL}$ and $t_{PLH}$ for the middle inverter using Eldo.

d) Use interconnect length obtained and connect the second and third inverter.
Extract the new netlist and obtain $t_{PHL}$ and $t_{PLH}$ of the middle inverter. Compare new values of delay times with corresponding values obtained in part 'c'.

## Course Outcomes:

At the end of the laboratory work, students will be able to:

- Design digital and analog Circuit using CMOS.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like NgSpice

# LAB 2: EMBEDDED RTOS LAB

**Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:**

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

**Interfacing Programs:**

1.. Write an application that creates a two task to Blinking two different LEDs at different timings
2. Write an application that creates a two task displaying two different messages in LCD display in two lines.
3. Sending messages to mailbox by one task and reading the message from mailbox by another task.
4. Sending message to PC through serial port by three different tasks on priority Basis.
5. Basic Audio Processing on IDE environment.

**Course Outcomes:**

- To gain the working knowledge of various embedded tools.
- To develop sample programs to be implemented on ARM based Processors or equivalent.
- Create applications for using the ARM Processor on IDE Environment using RAM Tool chain & Library.
- Develop applications using the concept of Interfacing.
- Design advanced embedded applications using ARM Processor.

# AUDIT COURSE II
# ENGLISH FOR RESEARCH PAPER WRITING

**Course Objectives:**

- To write clearly, concisely and carefully by keeping the structure of the paper in mind.
- To use standard phrases in English and further improve his command over it
- To write with no redundancy, no ambiguity and increase the readability of the paper.
- To plan and organize his paper by following a logical buildup towards a proper conclusion.
- To decide what to include in various parts of the paper.
- To write a suitable title and an abstract in order to attract the attention of the reader
- To identify the correct style and correct tense.
- To retain the scientific value of the paper by using minimum number of words.

UNIT I:

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and vagueness

UNIT II:

Clarifying Who Did What, Highlighting Your Findings, Hedging, and Critics in paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III:
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT IV:
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature

UNIT V:

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions: useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

**TEXT BOOKS:**

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press

3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book .
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

**Course Outcomes:**

- Frame the structure of the paper precisely
- Improve his command over English by using standard phrase
- Avoid repetition and mistakes in the paper and increase its readability
- Organize the paper logically towards a proper conclusion
- Decide on the content to be included in various parts of the paper
- Identify whether to use personal or impersonal style in the paper
- Express the content in a clear and concise way
- Attract the attention of the reader by providing a suitable title and an appropriate abstract

# II YEAR I SEMESTER

# COMMUNICATION NETWORKS

**Unit 1:**Introduction:
- Network Architecture, Performance

**Unit 2:**Connecting nodes:
- Connecting links, Encoding, framing, Reliable transmission, Ethernet and Multiple access networks, Wireless networks

**Unit 3:**Queuing models
- For a) one or more servers b) with infinite and finite queue size c) Infinite population

Internetworking:
- Switching and bridging, IPv4, Addressing, Routing Protocols, Scale issues, Routers - Architecture, IPv6

**Unit 4:**End-to-End Protocols:
- Services, Multiplexing, De-multiplexing, UDP, TCP, RPC, RTP

**Unit 5:**Congestion control and Resource Allocation
- Issues, Queuing disciplines, TCP congestion control, Congestion Avoidance, QoS Applications:
- Domain Name Resolution, File Transfer, Electronic Mail, WWW, Multimedia Applications

**Unit 6:**Network monitoring – Packet sniffing tools such as Wireshark Simulations using NS2/OPNET

**References:**


- Aaron Kershenbaum, "Telecommunication Network Design Algorithms", MGH, International Edition 1993.
- Vijay Ahuja, "Communications Network Design and Analysis of Computer Communication Networks", MGH, International Editions.
- Douglas E. Comer, "Internetworking with TCP/IP", Pearson Education, 6th Edition
- Larry L. Peterson, Bruce S, Devie, "Computer Networks" , MK, 5th Edition


**Course Outcomes:**

At the end of the course, students will be able to:

- Analyze protocols and algorithms, acknowledge tradeoffs and rationale
- Use routing, transport protocols for the given networking scenario and application
- Evaluate and develop small network applications

# SELECTED TOPICS IN MATHEMATICS

**Unit 1: Probability and Statistics:**

Definitions, conditional probability, Bayes Theorem and independence, Random Variables: Discrete, continuous and mixed random variables, probability mass, probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshev inequality.

**Unit 2: Special Distributions:** Discrete uniform, Binomial, Geometric, Poisson, Exponential, Gamma, normal distributions, Pseudo random sequence generation with given distribution, Functions of a Random Variable

**Unit 3: Joint Distributions:** Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution. Stochastic Processes: Definition and classification of stochastic processes, Poisson process

- Norms, Statistical methods for ranking data

**Unit 4:**Multivariate Data Analysis:Linear and non-linear models, Regression, Prediction and Estimation, Design of Experiments – factorial method, Response surface method

**Unit 5:Graphs and Trees:** Graphs: Basic terminology, multi graphs and weighted graphs, paths and circuits, shortest path Problems, Euler and Hamiltonian paths and circuits, factors of a graph, planar graph and Kuratowski's graph and theorem, independent sets, graph colouring

**Trees:** Rooted trees, path length in rooted trees, binary search trees, spanning trees and cut set,theorems on spanning trees, cut sets , circuits, minimal spanning trees, Kruskal's and Prim's algorithms for minimal spanning tree

**References:**


- Henry Stark, John W. Woods, "Probability and Random Process with Applications to Signal Processing", Pearson Education, 3rd Edition
- C. L. Liu, "Elements of Discrete Mathematics", Tata McGraw-Hill, 2nd Edition
- Douglas C. Montgomery, E.A. Peck and G. G. Vining, "Introduction to Linear Regression Analysis", John Wiley and Sons, 2001.
- Douglas C. Montgomery, "Design and Analysis of Experiments", John Wiley and Sons, 2001.
- B. A. Ogunnaike, "Random Phenomena: Fundamentals of Probability and Statistics for Engineers", CRC Press, 2010.

**Course Outcomes:**

At the end of the course, students will be able to:

- Characterize and represent data collected from experiments using statistical methods.
- Model physical process/systems with multiple variables towards parameter estimation and prediction
- Represent systems/architectures using graphs and trees towards optimizing desired objective.

# NANO MATERIALS AND NANOTECHNOLOGY

**Unit 1:** Nanomaterials in one and higher dimensions,

**Unit 2:** Applications of one and higher dimension nano-materials.

**Unit 3:** Nano-lithography, micro electro-mechanical system (MEMS) and nano-phonics.

**Unit 4:** carbon nanotubes – synthesis and applications

**Unit 5:**Interdisciplinary arena of nanotechnology

## References:


- Nanoscale Materials in Chemistry edited by Kenneth J. Klabunde and Ryan M. Richards, 2nd edn, John Wiley and Sons, 2009.
- Nanocrystalline Materials by A I Gusev and A ARempel, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
- Springer Handbook of Nanotechnology by Bharat Bhushan, Springer, 3rdedn, 2010.
- Carbon Nanotubes: Synthesis, Characterization and Applications by Kamal K. Kar, Research Publishing Services; 1stedn, 2011, ISBN-13: 978-9810863975..


## Course Outcomes:

At the end of the course, students will be able to:

- To understand the basic science behind the design and fabrication of nano scale systems.
- To understand and formulate new engineering solutions for current problems and competing technologies for future applications.
- To be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.

# OPEN ELECTIVE

# NON-CONVENTIONAL ENERGY SOURCES

**UNIT-I**

**Introduction**: Energy Scenario, Survey of energy resources. Classification and need for conventional energy resources.

**Solar Energy:** The Sun-sun-Earth relationship, Basic matter to waste heat energy circuit, SolarRadiation, Attention, Radiation measuring instruments.

**Solar Energy Applications:** Solar water heating. Space heating, Active and passive heating, Energystorage, Selective surface, Solar stills and ponds, solar refrigeration, Photovoltaic generation.

**UNIT -II**

**Geothermal Energy:** Structure of earth, Geothermal Regions, Hot springs. Hot Rocks, HotAquifers. Analytical methods to estimate thermal potential. Harnessing techniques, Electricity generating systems.

**UNIT-III**

**Direct Energy Conversion:** Nuclear Fusion, Fusion reaction, P-P cycle, Carbon cycle,Deuterium cycle, Condition for controlled fusion, Fuel cells and photovoltaic, Thermionic and Thermoelectric generation and MHD generator.

**Hydrogen Gas as Fuel:** Production methods, Properties, I.C. Engines applications, Utilization strategy,Performances.

**UNIT-IV**

**Bioenergy:** Biomass energy sources. Plant productivity, Biomass wastes, aerobic and anaerobicbioconversion processes, Raw material and properties of bio-gas, Bio-gas plant technology and status, the energetic and economics of biomass systems, Biomass gasification

**UNIT-V**

**Wind Energy**: Wind, Beaufort number, Characteristics, Wind energy conversion systems, Types,Betz model. Interference factor. Power coefficient, Torque coefficient and Thrust coefficient, Lift machines and Drag machines. Matching Electricity generation.

**Energy from Oceans**: Tidal energy, Tides, Diurnal and semi-diurnal nature, Power from tides, WaveEnergy, Waves, Theoretical energy available. Calculation of period and phase velocity of waves, Wave power systems, submerged devices. Ocean thermal Energy, Principles, Heat exchangers, Pumping requirements, Practical considerations.

**TEXTBOOKS:**

1.Non-conventional Energy Sources / GD Rai/Khanna publications.
2.Non-Conventional Energy Sources and Utilisation (Energy Engineering)/ R KRajput/ S.Chand.
3.Renewable Energy Sources /Twidell& Weir/Taylor and Francis/ 2nd special Indian edition .

**REFERENCE BOOKS:**

1.Renewable Energy Resources- Basic Principles and Applications/ G.N.Tiwari and M.K.GhosalNarosa Publications.
2.Renewable Energy Resources/ John Twidell& Tony Weir/Taylor & Francis/2nd edition.

3.Non Conventional Energy / K.Mittal/ Wheeler.

**Course Outcomes:**

- The concept of solar energy and their applications in different fields.
- The ways to harness energy from nonconventional energy sources like geothermal, wind and ocean.
- Understand Biogas generation and its impact on the Environment.
- Understand the different nonconventional sources and power generation techniques.
- Understand the role of Nonconventional Energy Sources when conventional sources are scarce in nature.

# OPEN ELECTIVE

# INDUSTRIAL SAFETY

**Objectives:**

- To explain the concept of various industrial safety methods.
- To outline division aspects measurements of safety performance .

**UNIT-I** :

Importance of Safety, health and environment. Health safety and environmental policy, fundamentals of safety, classification of accidents, Managements responsibility, objectives of safety management, National safety council, Employees state insurance act 1948, approaches to prevent accidents, principles of safety management, safety organization, safety auditing, maintenance of safety, measurements of safety performance, industrial noise and noise control, Industrial Psychology, Industrial accidents and prevention. Introduction to OSHAS 18001 AND OSHA.

**UNIT II**:

Process safety management (P.S.M) as per OSHA, legal aspects of safety, safety with respect to plant and machinery, the explosive act 1884, Petroleum act 1934, personal protective equipment, classification of hazards, protection of respiratory system, work permit system, hazards in refineries and process plants, safety in process plants, pollution in some typical process industry.

**UNIT III:**

Safe working practices, housekeeping, safe working environment, safety device and tools, precaution in use of ladders, safety instruction during crane operation, safety instruction for welding, burning and cutting and gas welding equipment, electrical safety, case studies, safety in use of electricity, electric shock phenomena, Occurrence of electric shock, medical analysis of electric shock and its effect, safety procedures in electric plants, installation of Earthing system,

**UNIT IV**:

Safety in hazardous area, hazard in industrial zones, classification of industrial Enclosures for gases and vapors. Mechanical, Chemical, Environmental and Radiation hazards, Machine guards and safety devices, slings, load limits, lifting tackles and lifting equipment, hydrostatic test, Chemical hazards, industrial toxicology, toxic chemicals and its harmful effects on humans, factors influencing the effect of toxic materials, Units of concentration, control measure, environmental hazards, devices for

measuring radiation, safety analysis and risk analysis, risk management, First aid, Safety measures to avoid occupational diseases.

**UNIT V**

Factories act – 1948 Stuatutory authorities – inspecting staff, health, safety, provisions relating to hazardous processes,welfare, working hours, employment of young persons – special provisions – penalties and procedures- Indian Boiler Act 1923, static and mobile pressure vessel rules (SMPV), motor vehicle rules, mines act 1952, workman compensation act, rules – electricity act and rules

**Text books :**

1. Industrial safety management By: L.M. Deshmukh Publishers: Tata Megraw Hill ,New Delhi Year: 2006 Edition: First
2. The Factories Act 1948, Madras Book Agency, Chennai, 2000

**References:**

1. Industrial safety health and environment Management system By: R.K. Jain & Sunil S. Rao Publishers: Khanna Publishers Year: 2008 Edition: Second

2. The Indian boilers act 1923, Commercial Law Publishers (India) Pvt.Ltd., Allahabad.

3."Accident prevention manual for industrial operations", N.S.C.,Chicago, 1982.

4. Industrial Safety and Environment by Amit Gupta

5. "Safety in Industry" N.V. Krishnan JaicoPublishery House, 1996.

**Outcome of course**:

- Educate students about how to reduce work place hazards and to encourage the standard of Safety ,Health & Environment programme , so as to aim 0% accidents and 100% safety in different industries in which Industrial Safety plays an important role.
- This has the blending mixture of both Learning and Skills.

# OPEN ELECTIVE

# OPERATIONS RESEARCH

**Objectives:**

- To familiarize the students with the use of practice oriented mathematical applications for optimization functions in an organization.
- To familiarize the students with various tools of optimization, probability, statistics and simulation,
- To applicable in particular scenarios in industry for better management of various resources.

**UNIT–I**

**Introduction:** Development – Definition– Characteristics and Phases – Types of models – operation Research models– applications.

**Allocation:** Linear Programming Problem Formulation – Graphical solution – Simplex method – Artificial variables techniques -Two–phase method, Big-M method.

**UNIT–II**

**Transportation Problem** – Formulation – Optimal solution, unbalanced transportation problem – Degeneracy.Assignment problem – Formulation – Optimal solution - Variants of Assignment Problem-Traveling Salesman problem.

**Sequencing** – Introduction – Flow **–**Shop sequencing – n jobs through two machines – n jobs through three machines – Job shop sequencing – two jobs through 'm' machines.

**UNIT–III**

**Replacement:** Introduction – Replacement of items that deteriorate with time – when money value is not counted and counted – Replacement of items that fail completely, group replacement.

**Theory of Games:** Introduction – Minimax (maximin) – Criterion and optimal strategy – Solution of games with saddle points – Rectangular games without saddle points – 2 X 2 games – dominance principle – m X 2 & 2 X n games -graphical method.

**UNIT–IV**

**Waiting Lines:** Introduction – Single Channel – Poisson arrivals – exponential service times – with infinite population and finite population models– Multichannel – Poisson arrivals – exponential service times with infinite population single channel Poisson arrivals.

**Inventory:** Introduction – Single item – Deterministic models – Purchase inventory models with one price break and multiple price breaks – shortages are not allowed – Stochastic models – demand may be discrete variable or continuous variable – Instantaneous production. Instantaneous demand and continuous demand and no set up cost.

**UNIT–V**

**Dynamic Programming:** Introduction – Bellman's Principle of optimality – Applications of dynamic programming- capital budgeting problem – shortest path problem – linear programming problem.

**Simulation:** Definition – Types of simulation models – phases of simulation– applications of simulation – Inventory and Queuing problems – Advantages and Disadvantages – Simulation Languages.

**TEXT BOOKS :**

1. Operations Research / S.D.Sharma-Kedarnath
2. Introduction to O.R/Hiller &Libermann (TMH).
3. Introduction to O.R /Taha/PHI

**REFERENCE BOOKS:**

1. Operations Research /A.M.Natarajan,P.Balasubramani,A. Tamilarasi/Pearson . Education.
2. Operations Research / R.Pannerselvam,PHI Publications.
3. Operation Research /J.K.Sharma/MacMilan.

**OUTCOMES:**

- Student will be able to Illustrate the need to optimally utilize the resources in various types of industries.
- Apply and analyze mathematical optimization functions to various applications.
- Demonstrate cost effective strategies in various applications in industry.

# OPEN ELECTIVE

# BUSINESS ANALYTICS

**Learning Objective:** To understand the importance of ever-increasing volume, variety and velocity of data in organization and application of data analytical tools for decision making.

**Learning Outcome:** Students will be able to understand a) Importance of Analytics b) Understanding the analytical tools c) Application of Analytical tools to solve business problems.

**Unit-I: Introduction to Business Analytics:** Importance, Scope, Evolution, Classification, and Application; Data Structure-Visualization of Data, Data Architecture, Measurement Scale; Decision Models-Classification, Structure of Decision Models; Data Structure and Data View-Understanding of data, exploring data using pivot tables.

**Unit-II: Descriptive Analytics:** Descriptive Statistical Measures–Population and samples, Measures of location, Measures of Dispersion, Measures of variability, measures of Association. Probability distribution and Data Modeling – Discrete Probability distribution, Continuous Probability distribution, Random sampling from Probability Distribution, Data Modeling and Distribution fitting.

**Unit-III: Predictive Analytics:** Karl Pearson Correlation Techniques -Multiple Correlation-Spearman's Rank correlation-Simple and Multiple regression-Regression by the method of least squares –Building good regression models –Regression with categorical independent variables --Linear Discriminant Analysis-One way and Two Way ANOVA

**Unit-IV: Data Mining:** Scope of Data Mining, Data Exploration and Reduction, Unsupervised learning –cluster analysis, Association rules, Supervised learning-Partition Data, Classification Accuracy, prediction Accuracy, k-nearest neighbors, Classification and regression trees, Logistics Regression.

**Unit-V: Simulation:** Random Number Generation, Monte Carlo Simulation, What if Analysis, Verification and Validation, Advantages and Disadvantages of Simulation, Risk Analysis, Decision Tree Analysis.

**References:**


- James Evans, Business Analytics, 2e, Pearson.
- Camm, Cochran, Fry, Ohlmann, Anderson, Sweeney, Williams Essential of Business Analytics, Cengage Learning.
- Thomas Eri, Wajid Khattack & Paul Buhler: Big Data Fundamentals, Concepts, drivers and Techniques by Prentice Hall of India, New Delhi.
- Akil Maheswari: Big Data, Upskill ahead by Tata McGraw Hill, New Delhi.
- Seema Acharya & Subhashini Chellappan: Big Data and Analytics, Wiley Publications, New Delhi.
- S. Christian Albright, Wayne L. Winston: Business Analytics: Data Analysis & Decision Making, Cengage Learning

# OPEN ELECTIVE

# SCRIPTING LANGUAGES

**Objectives:** The course demonstrates an in depth understanding of the tools and the scripting languages necessary for design and development of applications dealing with Bio-information/ Bio-data. The instructor is advised to discuss examples in the context of Bio-data/ Bio-information application development.

**UNIT I**

Introduction to PERL and Scripting Scripts and Programs, Origin of Scripting , Scripting Today, Characteristics of Scripting Languages, Web Scripting, and the universe of Scripting Languages. PERL-Names and Values, Variables, Scalar Expressions, Control Structures, arrays, list, hashes, strings, pattern and regular expressions, subroutines, advance perl - finer points of looping, pack and unpack, filesystem, eval, data structures, packages, modules, objects, interfacing to the operating system, Creating Internet ware applications, Dirty Hands Internet Programming, security Issues.

**UNIT II**

PHP Basics- Features, Embedding PHP Code in your Web pages, Outputting the data to the browser, Datatypes, Variables, Constants, expressions, string interpolation, control structures, Function, Creating a Function, Function Libraries, Arrays, strings and Regular Expressions.

**UNIT III**

Advanced PHP Programming Php and Web Forms, Files, PHP Authentication and Methodologies -Hard Coded, File Based, Database Based, IP Based, Login Administration, Uploading Files with PHP, Sending Email using PHP, PHP Encryption Functions, the Mcrypt package, Building Web sites for the World – Translating Websites- Updating Web sites Scripts, Creating the Localization Repository, Translating Files, text, Generate Binary Files, Set the desired language within your scripts, Localizing Dates, Numbers and Times.

**UNIT IV**

TCL Structure, syntax, Variables and Data in TCL, Control Flow, Data Structures, input/output, procedures, strings, patterns, files, Advance TCL- eval, source, exec and up level commands, Name spaces, trapping errors, event driven programs, making applications internet aware, Nuts and Bolts

Internet Programming, Security Issues, C Interface. Tk- Visual Tool Kits, Fundamental Concepts of Tk, Tk by example, Events and Binding , Perl-Tk.

**UNIT V**

Python Introduction to Python language, python-syntax, statements, functions, Built-in-functions and Methods, Modules in python, Exception Handling, Integrated Web Applications in Python – Building Small, Efficient Python Web Systems, Web Application Framework.

**TEXT BOOKS:**

1. The World of Scripting Languages, David Barron, Wiley Publications.

2. Python Web Programming, Steve Holden and David Beazley, New Riders Publications.

3. Beginning PHP and MySQL, 3rd Edition, Jason Gilmore, Apress Publications (Dreamtech)

**REFERENCE BOOKS:**

1. Open Source Web Development with LAMP using Linux, Apache, MySQL, Perl and PHP, J.Lee and B.Ware (Addison Wesley) Pearson Education.

2. Programming Python, M.Lutz, SPD.

3. PHP 6 Fast and Easy Web Development, Julie Meloni and Matt Telles, Cengage Learning Publications.

4. PHP 5.1,I.Bayross and S.Shah, The X Team, SPD.

5. Core Python Programming, Chun, Pearson Education.

6. Guide to Programming with Python, M.Dawson, Cengage Learning.

7. Perl by Example, E.Quigley, Pearson Education.

8. Programming Perl, Larry Wall, T.Christiansen and J.Orwant, O'Reilly, SPD.

9. Tcl and the Tk Tool kit, Ousterhout, Pearson Education.

10. PHP and MySQL by Example, E.Quigley, Prentice Hall(Pearson).

11. Perl Power, J.P.Flynt, Cengage Learning.

12. PHP Programming solutions, V.Vaswani, TMH.

# OPEN ELECTIVE

# MATHEMATICAL MODELING TECHNIQUES

**UNIT-I**: **INTRODUCTION TO MODELING AND SINGULAR PERTURBATION METHODS**

Definition of a model, Procedure of modeling: problem identification, model formulation, reduction, analysis, Computation, model validation, Choosing the model, Singular Perturbations: Elementary boundary layer theory, Matched asymptotic expansions, Inner layers, nonlinear oscillations

**UNIT-II**: **VARIATIONAL PRINCIPLES AND RANDOM SYSTEMS**

Variational calculus: Euler's equation, Integrals and missing variables, Constraints and Lagrange multipliers, Variational problems: Optics-Fermat's principle, Analytical mechanics: Hamilton's principle, Symmetry: Noether's theorem, Rigid body motion, Random systems: Random variables, Stochastic processes, Monte Carlo method

**UNIT-III**: **FINITE DIFFERENCES: ORDINARY AND PARTIAL DIFFERENTIAL EQUATIONS**

ODE: Numerical approximations, Runge-Kutta methods, Beyond Runge-Kutta, PDE: Hyperbolic equations-waves, Parabolic equations-diffusion, Elliptic equations-boundary values, **CELLULAR AUTOMATA AND LATTICE GASES:** Lattice gases and fluids, Cellular automata and computing

**UNIT- IV**: **FUNCTION FITTING AND TRANSFORMS**

Function fitting: Model estimation, Least squares, Linear least squares: Singular value decomposition, Non-linear least squares: Levenberg-Marquardt method, Estimation, Fisher information, and Cramer-Rao inequality, Transforms:Orthogonal transforms, Fourier transforms, Wavelets, Principal components

**FUNCTION FITTING ARCHITECTURES:**Polynomials: Pade approximants, Splines, Orthogonal functions, Radial basis functions, Over-fitting, Neural networks: Back propagation, Regularization

**UNIT-V**: **OPTIMIZATION AND SEARCH:** Multidimensional search, Local minima, Simulated annealing, Genetic algorithms **FILTERING AND STATE ESTIMATION:** Matched filters, Wiener filters, Kalman filters, Non-linearity and entrainment, Hidden Markov models

**TEXT BOOK:**

1. *The Nature of Mathematical Modeling*, Neil Gershenfeld, Cambridge University Press, 2006, ISBN 0-521-57095-6

**REFERENCE BOOKS:**

**1.** *Mathematical Models in the Applied Sciences*, A. C. Fowler, Cambridge University Press, 1997, ISBN 0-521-46140-5

2. *A First Course in Mathematical Modeling*, F. R. Giordano, M.D. Weir and W.P. Fox, 2003, Thomson, Brooks/Cole Publishers

3. *Applied Numerical Modeling for Engineers*, Donald De Cogan, Anne De Cogan, Oxford University Press, 1997

# OPEN ELECTIVE

# EMBEDDED SYSTEMS PROGRAMMING

**Unit 1 - Embedded OS (Linux) Internals**

Linux internals: Process Management, File Management, Memory Management, I/O Management. Overview of POSIX APIs, Threads – Creation, Cancellation, POSIX Threads Inter Process Communication - Semaphore, Pipes, FIFO, Shared Memory

Kernel: Structure, Kernel Module Programming Schedulers and types of scheduling.

Interfacing: Serial, Parallel Interrupt Handling Linux Device Drivers: Character, USB, Block & Network

**Unit 2 – Open source RTOS**

Basics of RTOS: Real-time concepts, Hard Real time and Soft Real-time, Differences between General Purpose OS & RTOS, Basic architecture of an RTOS, Scheduling Systems, Inter-process communication, Performance Matric in scheduling models, Interrupt management in RTOS environment, Memory management, File systems, I/O Systems, Advantage and disadvantage of RTOS.

**Unit 3 – Open Source RTOS Issues**

POSIX standards, RTOS Issues - Selecting a Real Time Operating System, RTOS comparative study. Converting a normal Linux kernel to real time kernel, Xenomai basics.

Overview of Open source RTOS for Embedded systems (Free RTOS/ Chibios-RT) and application development.

**Unit 4 – VxWorks / Free RTOS**

VxWorks/ Free RTOS Scheduling and Task Management - Realtime scheduling, Task Creation, Intertask Communication, Pipes, Semaphore, Message Queue, Signals, Sockets, Interrupts I/O Systems - General Architecture, Device Driver Studies, Driver Module explanation, Implementation of Device Driver for a peripheral

**Unit 5 – Case study**

Cross compilers, debugging Techniques, Creation of binaries & porting stages for Embedded Development board (Beagle Bone Black, Rpi or similar), Porting an Embedded OS/ RTOS to a target board ().Testing a real time application on the board

**TEXT BOOKS:**

1. Essential Linux Device Drivers, Venkateswaran Sreekrishnan

2. Writing Linux Device Drivers: A Guide with Exercises, J. Cooperstein

3. Real Time Concepts for Embedded Systems – Qing Li, Elsevier

**REFERENCES:**

1. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill

2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK

3. Software Design for Real-Time Systems: Cooling, J E Proceedings of 17the IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society

4. Real-time Systems – Jane Liu, PH 2000

5. Real-Time Systems Design and Analysis : An Engineer's Handbook: Laplante, Phillip A

6. Structured Development for Real - Time Systems V1 : Introduction and Tools: Ward, Paul T & Mellor, Stephen J

7. Structured Development for Real - Time Systems V2 : Essential Modeling Techniques: Ward, Paul T & Mellor, Stephen J

8. Structured Development for Real - Time Systems V3 : Implementation Modeling Techniques: Ward, Paul T & Mellor, Stephen J

9. Monitoring and Debugging of Distributed Real-Time Systems: TSAI, Jeffrey J P & Yang, J H

10. Embedded Software Primer: Simon, David E.

11. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill

# DISSERTATION PHASE 1

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following

- Relevance to social needs of society
- Relevance to value addition to existing facilities in the institute
- Relevance to industry need
- Problems of national importance
- Research and development in various domain

The student should complete the following:

- Literature survey Problem Definition
- Motivation for study and Objectives
- Preliminary design / feasibility / modular approaches
- Implementation and Verification
- Report and presentation

# II YEAR II SEMESTER

# DISSERTATION PHASE 2

The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:

- Experimental verification / Proof of concept.
- Design, fabrication, testing of Communication System.

The viva-voce examination will be based on the above report and work.

### Guidelines for Dissertation Phase – I and II

- As per the AICTE directives, the dissertation is a year long activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June.
- The dissertation may be carried out preferably in-house i.e. department s laboratories and centers OR in industry allotted through department s T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.
- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
- Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.
- During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.
- Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, A record of continuous progress.
- Phase – II evaluation: Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend for extension or

repeating the work

**Course Outcomes:**

At the end of this course, students will be able to

- Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem.
- Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
- Ability to present the findings of their technical solution in a written report.
- Presenting the work in International/ National conference or reputed journals.