DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

QUESTION BANK

FOR

II B.TECH II SEM (R17)
(2018 – 19)

MALLA REDDY COLLEGE OF ENGINEERING &TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

(Affiliated to JNTU, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade, ISO 9001:2008 Certified)

Maisammaguda, Dhulapally, Secunderabad – 500100.

INDEX

R17

Code No:

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech I Semester Regular Examinations, May 2019

Electronic Circuit Analysis

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1a. With the help of necessary equations, discuss the variation of A_I, A_V ,R_i, and R_o with R_S and R_L in Common Emitter simplified configuration. [7]

b. In a single stage CE amplifier R_S=1 KΩ, R_1=50 KΩ, R_2=2 KΩ, R_C=1 KΩ, R_L=1.2 KΩ, h_{fe}=50 and h_{ie}=1.1KΩ. Find A_I, R_i, R_o and A_V. [7]

(OR)

2a. Draw the circuit diagram of cascode amplifier with and without biasing circuit. What are the advantages of this circuit. [7]

b. Explain three types of coupling methods used in multistage amplifiers. [7]

SECTION-II

3a. Draw Hybrid - π model for a transistor in the CE configuration [5]

b. Derive the expression for the CE short circuit current gain at high frequencies [9]

(OR)

4a. Derive the expression for the CE current gain with resistive load at high frequencies [9]

b. Derive the expressions for higher and lower cut-off frequency of a multistage amplifier [5]

SECTION-III

5a. Draw and the block schematic of amplifier with negative feedback. [5]

b. Draw the circuit diagram of voltage series feedback amplifier and derive expressions for input and output resistances. [9]

(OR)

6a. Explain Barkhausen criterion for oscillation in feedback oscillator. [5]

b. Derive an expression for frequency oscillation of Hartley oscillator using transistor.[9]

SECTION-IV

7 Draw the push-pull class-B power amplifier and explain its operation. Show that the maximum conversion efficiency is 78.5%. [14]

(OR)

8. What is meant by distortion in power amplifiers, explain the given different types of distortions [14]

SECTION-V

9. Draw and explain the circuit diagram of single tuned capacitive coupled amplifier with its operation in detail. [14]

(OR)

10. Differentiate between single tuned and double tuned amplifier [14]

****

R17

Code No:

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech I Semester Regular Examinations, May 2019

Electronic Circuit Analysis

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1a. Discuss the classification of amplifiers based on frequency range, type of coupling, power delivered and signal handled. [7]

b. State and derive equivalent input, output impedance of Miller's theorem. [7]

(OR)

2a. Draw the circuit diagram of Darlington pair circuit derive input impedance (R_i) and current gain (A_I) [10]

b. What are the advantages and disadvantages of cascading of an amplifiers. [4]

SECTION-II

3. Derive the expressions for the following hybrid Π conductances [14]
i) g_m ii)$g_{b'e}$ ii) $g_{b'c}$ iv)g_{ce} v)$g_{bb'}$

(OR)

4a. Determine the hybrid –π parameters of a Transistor operating at Collector Current $I_C(Q)$=2mA,$V_{CE}(Q)$=20V and $I_B(Q)$=20μA.Transistor specifications are β=100,unity gain frequency f_T=50MHz,C_O=3pF,h_{ie}=1.4KΩ,h_{re}=2.5*10-4,h_{oe}=25μmhos.Assume that the Operating temperature is 3000K. [10]

b. Explain Gain bandwidth product [4]

SECTION-III

5a. Show that the bandwidth increases in negative feedback amplifiers. [7]

b. What are the different types of feedback amplifiers? Give their equivalent circuits.[7]

(OR)

6a. Draw the circuit diagram of RC-phase shift oscillator using BJT and derive the expression for frequency of oscillations. [10]

b. Compare positive feedback and negative feedback. [4]

SECTION-IV

7a. Draw the circuit diagram of Direct coupled class-A power amplifier and explain its operation. Show that the maximum conversion efficiency is 25%. [14]

(OR)

8. For a class B power amplifier driven from a 24V power supply and driving a load 8Ω load, compute
i) Input D.C power ii) output power iii) Conversion efficiency, if the peak to peak output voltage across the load resistance is 22V maximum [14]

SECTION-V

9. Derive an expression for bandwidth of an n-stage synchronously tuned amplifier. [14]

(OR)

10. Discuss the necessity of stabilization circuits in tuned amplifiers. [14]

****

R17

Code No:

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech I Semester Regular Examinations, May 2019

Electronic Circuit Analysis

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1a. With the help of necessary equations, discuss the variation of A_I, A_V ,R_i, and R_o with R_S and R_L in Common Base simplified configuration. [7]

b. Draw the equivalent circuits of RC coupled amplifier for Mid-band ,Low frequency range, high frequency range and derive the expressions for current gain, voltage gain.[7]

(OR)

2a. Explain about Boot-strap follower [7]

b. A CE-RC coupled amplifier uses transistor with the following h-parameters hfe=50, hoe=30x10-6 mhos, hre=2.5x10-4.The value of gm at the operating point is 50m mhos. The biasing resistor R1 between Vcc and base is 100KΩ and R2 between base and ground is 10KΩ.The load resistor RC = 5KΩ. let C = 160pF be the total shunt capacitance in the input circuit and the coupling capacitor Cc=6µF,Calculate for one stage of the amplifier (i) mid-band current gain (ii) mid-band voltage gain [7]

SECTION-II

3. Derive the expressions for the following hybrid Π conductances [14]
i) g_m ii)$g_{b'e}$ ii) $g_{b'c}$ iv)g_{ce} v)$g_{bb'}$

(OR)

4a. Derive the expression for the CE current gain with resistive load at high frequencies [9]

b. Derive the expressions for higher and lower cut-off frequency of a multistage amplifier [5]

SECTION-III

5a. With a neat sketch explain a negative feedback amplifier and obtain expression for its closed loop gain [7]

b. An amplifier requires an input signal of 60mV to produce a certain output. with a negative feedback to get the same output the required signal is 0.5V.The voltage gain with feedback is 90.Find the open loop gain and feedback factor. [7]

(OR)

6a. Draw the circuit of Hartley oscillator and explain its working. Derive the expressions for frequency of oscillation and condition for starting of oscillation. [9]

b. In an Hartley oscillator ,if L1=0.2mH,L2=0.3mH and C=0.003 µF, calculate the frequency of its oscillation [5]

SECTION-IV

7 Draw the complimentary-symmetry class-B power amplifier and explain its operation. Show that the maximum conversion efficiency is 78.5%. [14]

(OR)

8. What is Heat-sink. explain the different types of Heat sinks Determine the power dissipation capability of a transistor ,which has been mounted with a heat sink having thermal resistance Θ_{HS-A}=80c/w,T_A=400c,T_J=1600c, Θ_{J-C}=50c/w and Θ=850c/w [14]

SECTION-V

9a.	Define a Q-factor of a resonant circuit	[4]
b.	What is a tuned amplifier, what are the various types of tuned amplifiers	[10]
	(OR)	
10a.	What is a stagger tuned amplifier	[6]
b.	Explain the effect of cascading single tuned amplifiers on Bandwidth	[8]

****

R15

Code No: **R15A0405**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester supplementary Examinations, Nov/Dec 2018

Electronic circuit Analysis

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

******

Part- A (25 Marks)

1. Draw the simplified h parameter model of CE amplifier. [2M]
2. Three amplifiers of gain 20dB, 30dB and 40dB are connected together. Find the overall gain in dB and in normal units [3M]
3. Define frequency response of an amplifier. [2M]
4. What is the relation between f_T, f_β? [3M]
5. What is the difference between negative and positive feedback? [2M]
6. What are the conditions of an Oscillator [3M]
7. Explain various kinds of power amplifier. [2M]
8. Write short note on heat sinks. [3M]
9. What is the relation between Q factor and bandwidth. [2M]
10. What is difference between single and staggered tuned amplifiers [3M].

Part-B (50 Marks)

SECTION- I

2. a) Draw the exact h parameter model of CC amplifier[3M]

b) Derive the expression for current gain,input resistance, voltage gain and output resistance of CB amplifier using simplified h parameter model.[7M]

OR

3.a) For a CE configuration, what is the maximum value of RS for which Ro differs by no more than 10 percent of its value for RS = 0. The h-parameter values are h_{fe} = 50, h_{ie} =1.1KΩ, h_{re} = 2.5x10−4, h_{oe} = 25 μA/V [5M]

b) Explain different types of coupling mechanisms used in multi stage amplifier. [5M]

SECTION -II

4 a) Derive the expressions for hybrid pi conductance of CE transistor at high equencies.[6M]

b) A transistor is operating at $I_C$of 10mA at room temperature. It has h_{fe}= 100, h_{ie}=500Ω h_{re}=10^{-4},h_{oe}=50μ℧℧. Determine hybrid π impedances.[4M]

OR

5. Derive the expression for CE short circuit current gain [10M]

SECTION III

6. Derive the expressions for input and output resistances of a current series feedback amplifier.[10M]

OR

7.Derive the expression for frequency of oscillation of Hartley oscillator using BJT[10M]

SECTION -IV

8. a) Draw the circuit diagram of class A series fed power amplifier and derive an expression for its conversion efficiency. [6M]

b) A single transistor is acting as ideal Class B amplifier with load of 1KΩ, if DC collector current is 15mA, V_{CC}=20V. Determine its efficiency. [4M]

OR

9. a)Derive the expression for conversion efficiency of Class B push pull power amplifier.[6M]

b) Compare Class A, Class Band Class C power amplifiers.[4M]

SECTION- V

10.a) Draw the circuit of single tuned capacitance coupled amplifier and explain its operation. [6M]

b) Explain the classification of tuned amplifier. [4M]

OR

11.a) Write short notes on stability of tuned amplifier [5M]

b) Explain the effect of cascading single tuned amplifiers on bandwidth [5M]

****

R15

Code No: **R15A0405**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester Regular/Supplementary Examinations, April/May 2018

Electronic Circuit Analysis

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

******

Part- A (25 Marks)

1. a. Define Miller's Theorem. [2M]

b. Three amplifiers of gain 10dB, 20dB and 30dB are connected together. Find the overall gain in dB and in normal units. [3M]

c. What is meant by band width? [2M]

d. Draw the hybrid π model of CE transistor at high frequencies. [3M]

e. What are the advantages of negative feedback amplifiers? [2M]

f. What is meant by Barkhausen criterion? [3M]

g. Explain various kinds of distortions in amplifiers. [2M]

h. Compare class B complementary and push pull power amplifier. [3M]

i. Define Q factor. [2M]

j. Write the classification of tuned amplifiers. [3M]

Part-B (50 Marks)

SECTION I

2. a) Draw the exact h parameter model of CE amplifier [3M]

b) Derive the expression for current gain, input resistance, voltage gain and output Resistance of CE amplifier with emitter resistance using simplified h parameter model. [7M]

OR

3). Derive the expressions of input resistance, current gain and voltage gain of BJT Darlington amplifier. [10M]

SECTION II

4. Derive the expressions for hybrid pi conductances(i) g_m(ii) $g_{b'e}$ (iii) $g_{b'c}$(ii) g_{ce} of CE transistor at high frequencies. [10M]

OR

5.Derive the expression for CE short circuit current gain [10M]

SECTION III

6. a) Explain the effect of negative feedback on amplifier characteristics[6M]

b) Draw and explain the block schematic of voltage series feedback amplifier [4M]

OR

7. Derive the expression for frequency of oscillation of RC phase shift oscillator using BJT[10M]

SECTION IV

8. a) Draw the circuit diagram of class B push pull power amplifier and derive an expression for its conversion efficiency. [6M]

b) A single transistor is acting as ideal Class B amplifier with load of 1KΩ, if DC collector current is 10mA, V_{CC}=30V. Determine its efficiency. [4M]

OR

9. a) Derive the expression for conversion efficiency of Class A transformer coupled power amplifier. [6M]

b) Compare Series fed class A and transformer coupled class A power amplifier. [4M]

SECTION V

10.a) Draw the circuit of single tuned capacitance coupled amplifier and explain its operation. [6M]

b) Explain the effect of cascading single tuned amplifiers on bandwidth [4M]

OR

11.a) Draw the circuit of staggered tuned capacitance coupled amplifier and explain its Operation [5M]

b) Explain the differences between single tuned and staggered tuned amplifiers. [5M]

******

R17

Code No: R17A0404

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech II Semester Regular Examinations, Model paper-I

Pulse and Digital Circuits

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1 a. Draw the RC Low pass circuit. With necessary waveforms and expressions explain its working for step input. **[7+7 M]**

b. Prove that an RC circuit behaves as a good integrator if RC>15T, T is the period, input $E_m \sin\omega t$.

OR

2 a. What is attenuator? Draw the circuit of compensated attenuator show that condition for compensation is $R_1C_1=R_2C_2$. **[7+7=14M]**

b. Draw the series RLC circuit and derive expression for its transfer function.

SECTION-II

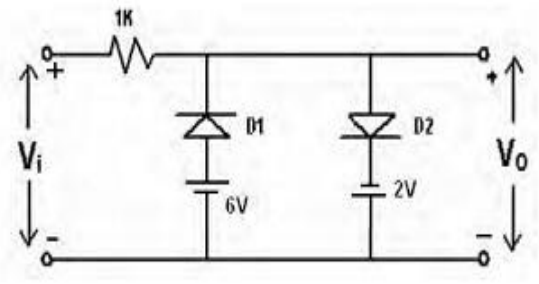
3 a. With the help of a neat circuit diagram explain the working of two level diode clippers. **[7+7=14M]**

b. Draw the circuit diagram of a Transistor clipping circuit. Explain its operation with its transfer characteristic and necessary expressions.

OR

4. a. Write short notes on shunt clipper, explain any on shunt clipper and draw its response, transfer characteristics. **[8+6=14M]**

b. Determine Vo for the network shown in Figure.1 for the given 16V P-P sin wave input. Also sketch the transfer characteristics. (Assume ideal diodes)



SECTION-III

5. a. With the help of a neat diagram and waveforms, explain the principle of operation of monostable multivibrator. **[10+4=14M]**

b. Explain the transistor switching times with the help of a neat circuit diagram.

OR

6. a. Explain the working of Schmitt trigger with the help of a neat circuit diagram.

b. Draw and explain the circuit of Astable Multivibrator with necessary waveforms. **[7+7=14M]**

SECTION-IV

7. a. Draw and explain the circuit of Bootstrap sweep generator. Derive an expression for sweep interval, T_s. **[7+7=14M]**

b. Explain UJT sweep generator with neat diagram.

OR

8 a. With neat sketches and necessary expressions, explain the transistor Miller time-base generator. **[7+7=14M]**

b. Briefly describe various methods to achieve sweep linearity in time-base circuit.

SECTION-V

9 a. Realize NAND and NOR gates using CMOS logic and explain their operation with the help of truth tables. **[7+7=14M]**

b. With a neat circuit diagram explain the operation of a TTL NAND gate Totem Pole output.

OR

10 a. Compare unidirectional and bi-directional Sampling Gates. Draw and explain the circuit diagram of a two-DIODE sampling gate. **[10+4=14M]**

b. Compare the various digital IC logic families.

****

R17

Code No: R17A0404

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech II Semester Regular Examinations, Model paper-II

Pulse and Digital Circuits

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1 a. Derive an Expression for the lower cutoff frequency of high pass RC circuit, and draw frequency response. **[7+7 M]**

b. A pulse of 5V amplitude and width of 0.5 msec. is applied to high pass RC circuit. Sketch the waveform. Also determine the percentage tilt in the output?

OR

2 a. With relevant waveforms, explain the response of an RC Low pass circuit with a square wave input under different time constants. **[7+7=14M]**

b. Obtain the response of High pass circuit to a sinusoidal input. Also obtain the relation between the lower cut-off frequency and time constant.

SECTION-II

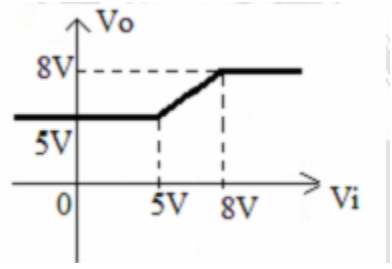
3 a. Explain the positive and negative clamper circuits. **[7+7=14M]**

b. Write short notes on shunt clipper, explain any on shunt clipper and draw its response, transfer characteristics.

OR

4. a. State and prove the clamping circuit theorem. **[8+6=14M]**

b. The ideal transfer characteristic of particular clipper circuit is shown in Figure. Design the circuit using ideal diodes and draw the input-output waveforms with proper explanation, if $V_i=10 \sin\omega t$.



SECTION-III

5. A self-biased binary uses n-p-n transistors have maximum values of V_{CE} (sat)=0.4V and V_{BE} (sat) = 0.8V and $V_{BE\ cutoff}$ = 0V. The circuit parameters are V_{cc} = 15V, R_C=1KΩ, R_1=6KΩ, R_2=15KΩ AND R_E=500Ω. **[14M]**

a) Find the stable-state currents and voltages.

b) Find the minimum value of h required for BJT to provide the above stable state values.

OR

6. a. Describe a bi-stable multivibrator. What do you mean by triggering? With the help of neat diagrams discuss the different methods of triggering a binary. **[7+7=14M]**

b. Design a free running multivibrator to generate a square wave of amplitude 10V and frequency 1kHz with 70% duty cycle. Consider n-p-n transistors with h_{fe}=25, $V_{BE(sat)}$=0.7V, $V_{CE(sat)}$=0.3V, $I_{C(sat)}$=5mA.

SECTION-IV

7. a. Mention the different types of sweep circuit. With neat circuit and waveform explain the working principle of Miller Sweep circuit. **[7+7=14M]**

b. Derive expression for sweep slope error (e_s), displacement error(e_d) and transmission error (e_t).

OR

8 a. Design Miller's Sweep circuit for the following specifications: Vcc=12V, i_c=1mA, h_{femin}=20, $V_{CE(sat)}$=0.3V, $V_{BE(sat)}$=0.7V, assume sweep period Ts=5 msecs. Briefly describe various methods to achieve sweep linearity in time-base circuit. **[7+7=14M]**

b. Draw the circuit of simple current time-base generator and explain its operation with the help of neat waveforms and necessary equations.

SECTION-V

9 a. Explain basic principle of Sampling Gate. Draw and explain the circuit diagram of a FOUR-DIODE sampling gate. **[7+7=14M]**

b. With a neat circuit diagram explain the operation of a TTL NAND gate Totem Pole output.

OR

10 a. With neat circuit diagram explain DTL NAND Gate. **[7+7=14M]**

b. Realize negative logic AND gate using diodes. Compare the logic families in terms of power dissipation and propagation delay.

****

R17

Code No: R17A0404

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech II Semester Regular Examinations, Model paper-III

Pulse and Digital Circuits

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

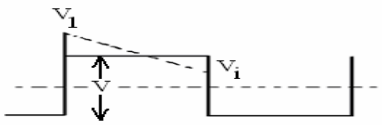
Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1 a. Derive the expression for percentage tilt (P) of a square wave output of RC High pass circuit. **[7+7 M]**

2.a) The output of a high pass RC circuit for a symmetrical square wave input is shown in Figure.1. Derive the expression for percentage tilt in the output.

b.



OR

2 a. What is attenuator? Draw the circuit of compensated attenuator show that condition for compensation is $R_1C_1=R_2C_2$. **[7+7=14M]**

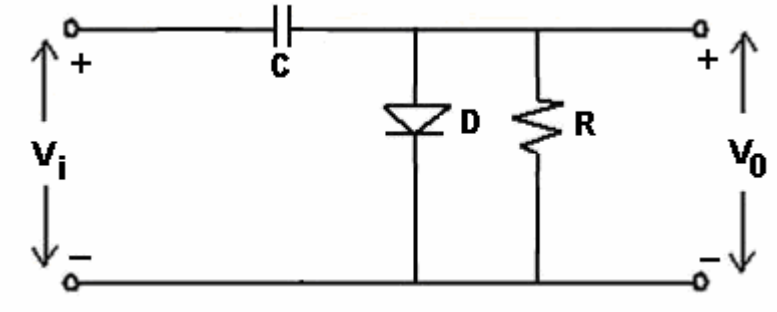
Draw the series RLC circuit and derive expression for its transfer function.

b.

SECTION-II

3 a. a) Explain negative peak clipper with and without reference voltage. **[7+7=14M]**

b. b) Sketch the steady state output voltage for the clamper circuit shown in figure.2 and locate the output d.c level and the zero level. The diode used has R_f = 1KΩ, R_r = 600 KΩ, V_γ = 0. C = 0.1μF and R = 20 KΩ. The input is a ± 20 Volts square wave with 50% duty cycle.

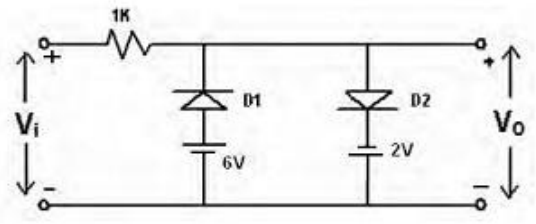


OR

4. a Write short notes on series clipper, explain any on series clipper and draw its response, transfer characteristics. **[8+6=14M]**

Determine Vo for the network shown in Figure.1 for the given 16V P-P sin wave input. Also sketch the transfer characteristics. (Assume ideal diodes)

b.



SECTION-III

5. a With the help of a neat diagram and waveforms, explain the principle of operation of astable multivibrator. **[10+4=14M]**

b Explain the transistor switching times with the help of a neat circuit diagram.

OR

6. a. Explain the working of Schmitt trigger with the help of a neat circuit diagram.

b. Draw and explain the circuit of monostable Multivibrator with necessary waveforms. **[7+7=14M]**

SECTION-IV

7. a. Draw and explain the circuit of Bootstrap sweep generator. Derive an expression for sweep interval, T_s. **[7+7=14M]**

b. Explain UJT sweep generator with neat diagram.

OR

8 a. With neat sketches and necessary expressions, explain the transistor Miller time-base generator. **[7+7=14M]**

b. Briefly describe various methods to achieve sweep linearity in time-base circuit.

SECTION-V

9 a. Realize NAND and NOR gates using CMOS logic and explain their operation with the help of truth tables. **[7+7=14M]**

b. With a neat circuit diagram explain the operation of a TTL NAND gate Totem Pole output.

OR

10 a Compare unidirectional and bi-directional Sampling Gates. **[10+4=14M]**

b. Draw and explain the circuit diagram of a four -DIODE sampling gate.

Compare the various digital IC logic families.

****

R17

Code No: R17A0404

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech II Semester Regular Examinations, Model paper-IV

Pulse and Digital Circuits

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1 a. Draw the RC High pass circuit. With necessary waveforms and expressions explain its working for pulse input. **[7+7 M]**

b. Prove that an RC circuit behaves as a good Differentiator.

OR

2 a. What is attenuator? Draw the circuit of compensated attenuator show that condition for compensation is $R_1C_1=R_2C_2$. **[7+7=14M]**

b. Derive the expression for percentage tilt (P) of a square wave output of RC High pass circuit

.

SECTION-II

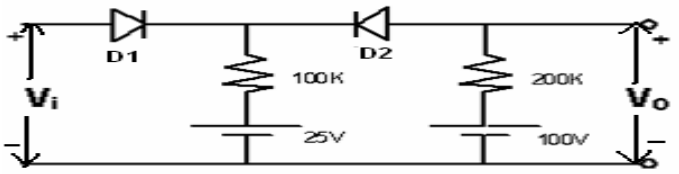
3 a. With the help of a neat circuit diagram explain the working of different diode clippers. **[7+7=14M]**

b. Draw the circuit diagram of a Transistor clipping circuit. Explain its operation with its transfer characteristic and necessary expressions.

OR

4. a. Explain the operation of two level slicer **[8+6=14M]**

b. For the circuit shown in Figure.1, a sine wave input of 100V peak is applied. Sketch the output voltage V_O to the same time scale & transfer characteristic. Assume ideal diodes.



SECTION-III

5. a. With the help of a neat diagram and waveforms, explain the principle of operation of bi-stable multivibrator. **[10+4=14M]**

b. Explain the transistor switching times with the help of a neat circuit diagram.

OR

6. a. Explain the working of Schmitt trigger with the help of a neat circuit diagram.

b. Draw and explain the circuit of Mono-stable Multivibrator with necessary waveforms. **[7+7=14M]**

SECTION-IV

7. a. Draw and explain the circuit of bootstrap generator. **[7+7=14M]**

b. Explain UJT sweep generator with neat diagram.

OR

8 a. With neat sketches and necessary expressions, explain the transistor Miller time-base generator. **[7+7=14M]**

b. Briefly describe various methods to achieve sweep linearity in time-base circuit.

SECTION-V

9 a. Realize NAND and NOR gates using CMOS logic and explain their operation with the help of truth tables. **[7+7=14M]**

b. With a neat circuit diagram explain the operation of a TTL NAND gate Totem Pole output.

OR

10 a. Compare unidirectional and bi-directional Sampling Gates. Draw and explain the circuit diagram of a four -DIODE sampling gate. **[10+4=14M]**

b. Draw the circuit diagram and explain DCTL, RTL and DTL

****

Code No: R15A0404 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester supplementary Examinations, Nov/Dec 2018

Pulse and Digital Circuits

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

*****

PART – A **(25 Marks)**

Q1. (a) Explain the condition when RC high pass circuit works as a differentiator? [2M]
(b) What is difference between linear and non-linear waveshaping circuits? [3M]
(c) Draw a circuit to transmit that part of a sine wave which is below +6V. [2M]
(d) What is the difference between positive clamping and negative clamping? [3M]
(e) Explain how a transistor acts as a open switch? [2M]
(f) What are the commutating capacitors? Why these are used in binary? [3M]
(g) Give the relationship between the slope error, displacement error and transmission error. [2M]
(h) Define the sweep time and restoration time for time-base generators. [3M]
(i) What is a sampling gate? What are the applications of it? [2M]
(j) Draw Bidirectional diode gate? [3M]

PART – B **(50 Marks)**

SECTION – I

Q2. (a) An RC differentiator circuit is driven from 500Hz symmetrical square wave of 10V peak-to-peak. Calculate the output voltages levels under steady state conditions, if RC= 1 msec. [5M]
(b) What are the drawbacks of uncompensated attenuators? Prove that the condition to prevent input signal from distortion is $R_1C_1 = R_2C_2$ in an adequately compensated attenuator. [5M]

OR

Q3. (a) In an RC low pass circuit R= 1KΩ and C=1μF. A square wave with half period of 10 μsec is applied as input to this circuit. Determine the output waveforms. [5M]
(b) A pulse of 5V amplitude and width of 0.5 msec is applied to high pass RC circuit consisting of R = 22 KΩ and C = 0.47μF. Estimate the output voltage levels and sketch the waveform. Also determine the percentage tilt in the output? [5M]

SECTION – II

Q4. (a) Explain the working of a two-level diode clipper with the help of circuit diagram, waveform and transfer characteristics. [5M]
(b) Explain the clamping circuit theorem considering the source resistance and the diode forward resistance. [5M]

OR

Q5. For the circuit shown in figure 1, an input voltage V_i linearly varies from 0V to 150 V is applied. Sketch the output voltage V_0 and transfer characteristics. Assume diodes are ideal [10M]

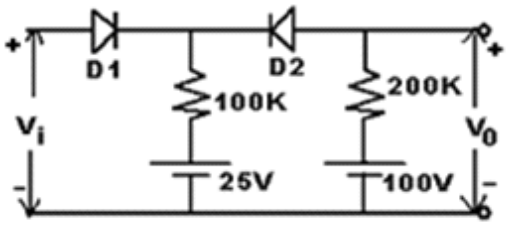


Figure 1

SECTION – III

Q6. (a) Design a collector coupled astable multivibrator using NPN silicon transistors with h_{fe}=40, $r_{bb'}$ = 200Ω supplied with Vcc=10V and circuit component values are Rc=1.2KΩ and C=270 pF. Plot the waveforms at collector and base of both the transistors. [6M]

(b) Define transition time and settling time in a bistable multivibrator. Justify that the resolving time is the sum of transition time and settling time. [4M]

OR

Q7. (a) Explain the operation of a collector coupled transistor monostable multivibrator with the help of neat circuit diagram and waveforms. [5M]

(b) Draw astable multivibrator and explain its operations . [5M]

SECTION – IV

Q8. (a) With suitable diagram, explain the function of sweep circuit using UJT. Derive the expression for frequency of oscillations [6M]

(b) What is the recovery time of a sweep circuit. How do you achieve short recovery time? [4M]

OR

Q9. (a) Explain the working of a transistor Bootstrap sweep circuit and derive expression for the slope sweep error [6M]

(b) What are the different methods of generating time-base waveforms? Explain about each briefly. [4M]

SECTION – V

Q10. (a) Explain about unidirectional diode sampling gate. Write its advantages and disadvantages. [4M]

(b) Explain the operation of two input TTL NAND gate? [6M]

OR

Q11. (a) Explain how to cancel the pedestal in a sampling gate with suitable circuit diagram.[6M]

(b) Discuss in brief (i) RTL gates (ii) DTL gates [4M]

****

R17

Code No: R17A0407

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech I Semester Regular Examinations, November 2018

SWITCHING THEORY AND LOGIC DESIGN

(EEE, ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1. a) Convert the number $(127.75)_8$ to base 10, base 3, base 16 and base 2. **[6+2+6=14M]**

b) Given that $(64)_{10} = (100)_b$, determine the value of b.

c) Perform the binary arithmetic operations on (+12)-(4) using signed 2'scomplement method.

OR

2. a) Write the procedure for constructing Hamming codes. Construct hamming codes for the 1011. **[6+4+4=14M]**

b) Justify the statement that "Gray code is a class of reflected code".

c) Realize the basic gates using NAND and NOR gates only.

SECTION-II

3. a) . Determine the canonical product-of-sums and sum-of-products form of **[6+8=14M]**

T = x'(y' + z')

b) For the given function T(W,X,Y,Z)=∑m(0,1,5,7,8,10,14,15)

i) Show the map ii) find all the prime implicants and indicate which are essential iii) Find minimal expression and realize using basic logic gates.

OR

4. a) Simplify the following function using K-map and implement using universal gates **[7+7=14M]**

F=A'BC'D'+A'BC'D+AB'CD+AB'CD+AB'CD'+ABCD+A'B'C'D'

b) Use tabular method and simplify the following functions

F=∑m(2,3,5,6,7,9,12,14,15)

SECTION-III

5. a) Design a combinational logic circuit with 4 inputs A,B,C,D. The output is HIGH if and only if A and C inputs go HIGH. Draw the truth table. Minimize the Boolean function using K-Map. Draw the circuit diagram. **[6+8=14M]**

b) Design full adder and Realize full adder using two adders and logic gates.

OR

6. **a)** Define magnitude comparator and Design a 2-bit comparator to compare two 2-bit numbers. **[8+6=14M]**

b) Design a circuit to convert Xs-3 code to BCD code.

SECTION-IV

7. **a)** Draw the logic diagram, truth table characteristic table and characteristic equation of an SR-latch. **[10+4=14M]**

b) Compare latch and flip-flop.

OR

8. **a)** Covert the following **[10+4=14M]**

i) JK flip-flop to T flip-flop ii) SR flip-flop to D flip-flop

b) Write the differences between combinational and sequential circuit.

SECTION-V

9. **a)** Design a clocked sequential circuit machine using D flip-flop for the state diagram. Use state reductions if possible make proper assignment. **[8+6=14M]**

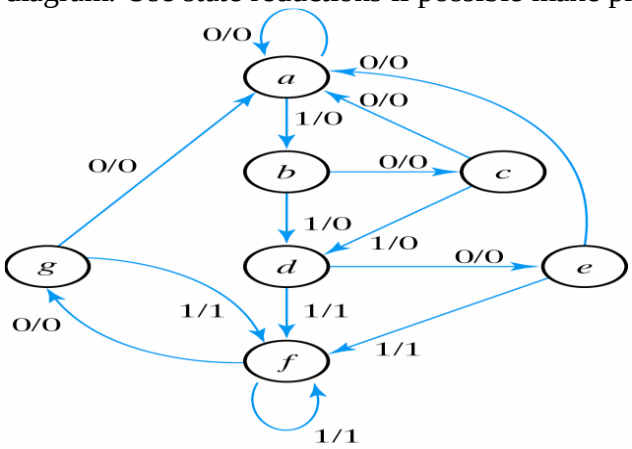


Fig. 5-22 State Diagram

b) Explain the following related to sequential circuits with suitable.

a) State diagram b) State Table c) State Assignment

OR

10. **a)** Design a Mod-6 synchronous counter using JK flip-flops. **[7+7=14M]**

b) What is meant by universal shift register and Design it.

****

R17

Code No: R17A0407

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech I Semester Regular Examinations, November 2018

SWITCHING THEORY AND LOGIC DESIGN

(EEE, ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1. a) Use 2's complement arithmetic to subtract **[6+4+4=14M]**
i) $(54)_{10}$ from $(231)_{10}$ ii) $(-27)_{10}$ - $(87)_{10}$

b) Define the terms i) Cyclic codes ii)Unit distance codes

c) Briefly explain about BCD code.

OR

2. a) A receiver has received a message code 1110110 which is an even parity Hamming code. Determine whether the message code has any error. If so correct the error. Give proper reasoning for your answer. **[10+4=14M]**

b) Explain the different logic gates in detail?

SECTION-II

3. a) State and Prove the Huntington postulates of Boolean algebra. **[7+7=14M]**

b) Find the complement of the function and represent in sum of minterms
F = xy + z'

c) Simplify the following function and realize using universal gates

F (A,B,C) = A'BC' + ABC + B'C' + A'B'

OR

4. a) Use tabular method and simplify the following functions **[7+7=14M]**
F=∑m(0,1,6,7,8,9,13,14,15)

b) What is importance of the Don't care conditions in K-map method.
F=∑m(0,1,3,8,6,7,14,15)+ d(5,11,13)

SECTION-III

5. a) Design a combinational circuit whose input is a 3 input binary number and whose output is a 2's complement of the input number. **[7+7=14M]**

b) Implement the following functions using multiplexer.

i)F1=∑m(2,3,6,8,12) ii) F2=∑m(1,3,5,6,7,8,10) iii)F3= ∑m(1,3,4,5,6,13,14)

OR

6. a) What is a Half Subtractor? Realise using universal gates.
b) Design 3 to 8 line decoder and explain the operation. **[5+5+4=14M]**
c) Implement full adder using 8:1 MUX.

SECTION-IV

7. a) What is race around condition? How it can be avoided? **[4+4+6=14M]**
b) Draw schematic circuit of master-slave JK flip-flop and explain its operation with the help of truth table.
c) Write the characteristic equations, excitation tables for JK, T, SR and D flip-flops.

OR

8. a) What is excitation table? Write the excitation tables for the following flip-flops. **[7+7=14M]**
i) SR flip-flop ii)JK flip-flop iii)T flip-flop
b) Convert D flip-flop to SR flip-flop.

SECTION-V

9. a) Analyse the following synchronous sequential circuit. **[10+4=14M]**

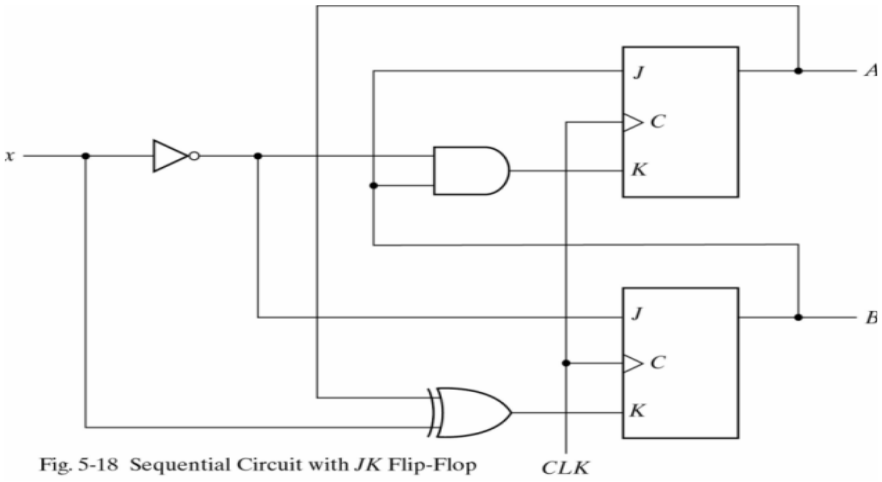


Fig. 5-18 Sequential Circuit with *JK* Flip-Flop

b) Compare mealy and moore machines.

OR

10. a) Design a modulo-12 up synchronous counter using T flip-flop and draw the circuit diagram. **[8+6=14M]**
b) Design and explain the operation of Bi-directional shift register.

****

R17

Code No: R17A0407

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech I Semester Regular Examinations, November 2018

SWITCHING THEORY AND LOGIC DESIGN

(EEE, ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1. a) Convert the decimal number 234 to binary, octal and hexadecimal. **[4+6+6=14M]**

b) Obtain the 1's and 2's complement of the binary numbers.
i)1011011 ii)0110101 iii)10110 iv)001101100

c) Write Gray code for the following decimal numbers
i)1000 ii) 724 iii) 83

OR

2. a) Perform $(46)_{10}$ - $(22)_{10}$ in BCD using 10's complement. **[4+10=14M]**

b) Given the 8-bit data word 01011011, generate the 12-bit composite word for the hamming code that corrects and detects single error.

SECTION-II

3. a) Demonstrate by means of the truth tables the validity of the following theorems of Boolean algebra. **[9+5=14M]**
i)Commutative law ii)Distributive law iii)Demorgan's theorems

b) What do you mean by minterms and maxterms?

OR

4. a) Simplify the function $F=\Sigma m(0,1,2,8,9,10,11)+\Sigma d(14,15)$ using K-Map and implement using gates. **[7+3+4=14M]**

b) Simplify the given Boolean function to minimal number of literals
F=X+Y[Z+(X+Z)']

c) Define prime and essential prime implicants.

SECTION-III

5. a) Draw the block diagram of BCD adder using two 4-bit parallel adders and **[10+4=14M]**

b) logic gates.
Design a combinational circuit to find the 2's complement of a given 4-bit binary number and realize using NADN gates.

OR

6. a) Design a logic circuit to convert BCD to gray code. **[8+6=14M]**

b) Design a 3 to 8 decoder. Draw the circuit diagram, functional table and explain the working of the decoder circuit.

SECTION-IV

7. a) Draw the schematic circuit of JK flip-flop and explain its operation with the help of truth table. **[8+6=14M]**

b) Define the terms preset and clear in connection with flip-flop.

OR

8. a) Write the conversion procedures of the flip-flops. Convert T-flip-flop to JK-flip-flop. **[8+6=14M]**

b) Discus the applications of the flip-flops.

SECTION-V

9. a) Compare synchronous and asynchronous circuits. **[4+10=14M]**

b) A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z

.The flip-flop input equations and circuit output equation are

JA=Bx+B'y' KA=B' xy'

JB=Ax'y' KB=A+xy'

Z=Ax'y'+Bxy'

i) Draw the logic diagram of the circuit.

ii) Derive the state equations for A and B

iii) Tabulate the state table

iv) Draw the state diagram.

OR

10. a) Define Counter and Design Decade synchronous counter using JK flip-flops. **[10+4=14M]**

b) Compare merits and demerits of ripple and synchronous counters.

****

R15

Code No: R15A0407

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester Regular/Supplementary Examinations, April/May 2018

Switching Theory and Logic Design

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART – A **(25 Marks)**

1. (a) Find the dual of the function f= ab+b'c+a'b' 2M
   (b) Convert the following numbers into Decimal numbering system 3M
   i) $(135.4)_6$ ii) $(430.2)_4$
   (c) Explain about prime implicants and essential prime implicants of a function. 2M
   (d) Design a full adder logic circuit. 3M
   (e) What are the differences between combinational and sequential circuits. 2M
   (f) Discus about Race-around condition in J K Flip-Flop. 3M
   (g) What are the applications of Flip-Flops? 2M
   (h) Explain the difference between synchronous counter and Asynchronous counter 3M
   (i) What is a merger chart? 2M
   (j) Differentiate between moore and mealy FSMs. 3M

PART – B **(50 Marks)**

SECTION – I

2. (a) Perform the following operations using 2's complement 6M
   i) 1011.01-1001.11 ii) 100010-100011
   (b) Convert the following to the other canonical form 4M
   (i) $F(A,B,C,D) = \Sigma_m(1,3,5,6,11,13)$
   (ii) $F(A,B,C,D) = \pi(1,2,5,7,10,12)$

(OR)

3. (a) Simplify the Boolean expression A'C'+ABC+AC'+AB' and realize it using basic gates. 5M
   (b) What was the original 8 bit data word that was written into the memory if the 12 bit Hamming code word read out is "000011101010". 5M

SECTION – II

4. (a) Simplify the following function using K-map and implement using gates. 5M
   $f(w,x,y,z)=\Sigma(0,2,5,7,9,11,13,15)$
   (b) Draw and explain the logic diagram of 3 to 8 decoder. 5M

(OR)

5. (a) Simplify the following function using Quine-McCluskey method 5M
   $F(w, x, y,z)= \Sigma_m (4,5,6,7,12,13,14) + \Sigma_\Phi(1,9,11,15)$
   (b) Design a combinational circuit that converts four-bit Binary code to four-bit Gray code. 5M

SECTION – III

6. (a) What is Race around condition and explain how it is eliminated in Master Slave. 6M

   (b) Show that the characteristic equation of JK flip is Q(t+1) = JQ'+K'Q 4M

(OR)

7. (a) Construct a JK flip flop using a T flip flop and other logic gates. 5M

   (b) Explain the operation of clocked SR flip flop with the help of logic diagram. 5M

SECTION – IV

8. (a) Draw the logic diagram of a 4-bit bidirectional shift register and explain its working. 5M

   (b) Design a Modulo-7 binary synchronous counter using J K Flip-Flop. 5M

(OR)

9. (a) Reduce the following state table to a minimum number of states using state reduction 5M

Present state	Next state		Output (Z)	
	X=0	X=1	X=0	X=1
a	c	b	1	1
b	d	c	0	0
c	g	d	0	1
d	e	f	1	0
e	a	f	1	0
f	g	f	1	0
g	a	f	1	0

   (b) Draw and explain the logic diagram of 4 bit twisted ring counter with the help of timing diagrams. 5M

SECTION – V

10. (a) Discuss about capabilities and limitations of finite state machines. 5M

    (b) Write short notes on incompletely specified machines. 5M

(OR)

11. (a) Find the equivalence partition for the machine shown in below table 10M

    (b) Show the standard form of the corresponding reduced machine.

    (c) Find a minimum-length sequence that distinguishes state A from state B

Present state	Next state, Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

****

Code No: R15A0407

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester supplementary Examinations, Nov/Dec 2018

Switching Theory and Logic Design

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

****

PART – A (25 Marks)

1. (a) Express the following numbers in decimal [2M]
   i) $(11010.0111)_2$ ii) $(FAFA.B)_{16}$
   (b) Find the complement of [3M]
   i) (x'+y'+z)(x'+y)(x+z) ii) (A'B+CD)E'
   (c) Discuss the advantages of priority encoder. [2M]
   (d) Design a full subtractor logic circuit. [3M]
   (e)Implement 8:1 MUX using 4:1 and 2:1 MUX. [2M]
   (f) Draw the logic diagram of SR flip flop. [3M]
   (g) Differentiate between latch and flip flop [2M]
   (h) Explain how a counter can be used as a frequency divider circuit. [3M]
   (i) What is distinguishable state ? [2M]
   (j) Differentiate between moore and mealy FSMs. [3M]

PART –B (50 Marks)

SECTION – I

2. (a)Simplify the Boolean expression xy'z+x'y'z+w'xy+wx'y+wxy and realize it using basic gates. [5M]
   (b) Consider the message bits m4 m3 m2 m1 = 1101. Encode it into hamming code to detect single error.[5M]

(OR)

3. (a)Express the function (xy+z)(y+xz) in canonical SOP and POS forms. [5M]
   (b) Perform the following operations using 2's complement [5M]
   i) 1001.11-1100.10 ii) 87-99

SECTION – II

4. (a) Simplify the following function using K-map [5M]
   $f(A,B,C,D,E)=\Sigma(3,6,7,8,10,12,14,17,19,20,21,24,25,27,28)$
   (b) A majority circuit is a combinational circuit whose output is equal to 1 if the input variableshave more 1's than 0's. The output is 0 otherwise. Design a three input majority circuit and implement it using NAND gates. [5M]

(OR)

5. (a) Implement the following Boolean function with a multiplexer. [5M]
   $F(A,B,C,D)=\sum(1, 3, 4, 11, 12, 13, 14,15)$
   (b) Simplify the following function using Quine-McCluskey method [5M]
   $F(w, x, y,z)= \Sigma_m (0,6,8,13,14) + \Sigma_\Phi(2,4,10)$

SECTION – III

6. (a) What is Race around condition and explain how it is eliminated in Master Slave D-flip flop. [6M]
   (b) Show that the characteristic equation of T flip is Q(t+1) = TQ'+T'Q [4M]

(OR)

7. (a) Construct a JK flip flop using a D flip flop and other logic gates. [5M]
   (b) Explain the operation of clocked JK flip flop with the help of timing diagrams. [5M]

SECTION – IV

8. (a) Design a synchronous counter using JK flipflops with the following repeated binary sequence 0,1,2,3,4,5,6. [5M]
   (b) Design a 4- bit universal shift register and explain its operation. [5M]

(OR)

9. (a) Draw and explain the logic diagram of 4-bit ring counter with the help of timing diagrams.[5M]

(b) A sequential circuit has two J-K flip-flops A and B and one input X. [5M]
The circuit is described by the following flip-flop input equations:

$J_A = X$ $K_A = B'$ $J_B = X$ $K_B = A$

Derive the state equations A(t+1) and B(t+1) and draw the state diagram of the circuit.

SECTION – V

10. (a) Find the equivalence partition for the machine shown in below table [3M]
    (b) Show the standard form of the corresponding reduced machine. [4M]
    (c) Find a minimum-length sequence that distinguishes state A from state B [3M]

Present state	Next state, Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

(OR)

11. (a) What is merger table method? Explain with suitable example. [5M]
    (b) Write short notes on state equivalence and machine minimization. [5M]

****

R15

Code No: R15A0407

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester Regular Examinations, April/May 2017

Switching Theory and Logic Design

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART-A

1. (a). Express the following numbers in decimal 2M
   (i) $(10110.0101)_2$
   (ii) $(16.5)_{16}$
   (b). Write the following Boolean expression in Product-of-Sum form 3M
   $f = \bar{a}\,b + \bar{a}\,\bar{c} + abc$
   (c) Express the basic difference between decoder and encoder? 2M
   (d) What are prime and essential prime implicants? Justify with suitable example using K map. 3M
   (e) What is the basic architecture difference between combinational and sequential circuits? 2M
   (f) Sketch the logic diagram of RS flip flop? 3M
   (g) Write the difference between synchronous and asynchronous counter. 2M
   (h) Define state diagram and state table. 3M
   (i) What are the limitations of Finite State Machines (FSM)? 2M
   (j) What is the difference between Mealy and Moore machine? 3M

PART B

Section-I

2. (a) Implement the following function using NAND gates [5]
   $F = A(B + CD) + \overline{BC}$ ⇒ $AB + AcD + \bar{B} + \bar{C}$
   (b) Express the complement of the following function in sum-of-minterm form
   $F(x, y, z) = \prod(3,5,7)$. [5]

OR

3. (a) Let X=$(1010100)_2$ and Y=$(1000011)_2$
   Perform (i) X-Y, (ii) Y-X using 2'complement representation. [2]
   (b) Represent the decimal number 6248 in (i) BCD, (ii) binary, (iii) gray [4]
   (c) State and prove the following laws of Boolean algebra: (i) Commutative, (ii) Associative. [4]

Section-II

4. (a) Minimise the following function using K-map [5]
   $F(A,B,C,D) = \sum m(1,4,5,7,8,9,12,14) + d(0,3,6,10)$
   (b) Construct a 3x8 decoder using logic gates and truth table. [5]

OR

5. Design half adder & full adder circuit [10]

Section-III

[5+5]

6. Convert the following

(a) JK Flip flop to T-Flip flop
(b) RS Flip flop to D-Flip flop

OR

7. (a) What is race condition in JK-Flip flop ? Demonstrate how it can be avoided using Master-Slave Flip flop? [6]
(b) Draw a 4-bit Johnson's counter and explains its operation? [4]

OR

Section-IV

8. (a) For the following state Table-1

PS	NS		OUTPUT	
	x=0	x=1	x=0	x=1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	F	0	1
E	A	F	0	1
F	G	F	0	1
G	A	F	0	1

Table 1

(i) Draw the corresponding state diagram [2]
(ii) Tabulate the reduced state table [6]
(iii) Draw the state diagram corresponding to the reduced state table [2]

OR

9. Design Mod 6 counter using J-K flip flop [10]

Section-V

10. Convert the following (see, Table 2) Mealy machine into corresponding Moore machine [10]

PS	NS	Z
	x=0	x=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

Table 2

OR

11. Draw the ASM chart for binary multiplier? [10]

****

R17

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech II year – II Semester Examinations

Model Paper-1

ELECTROMAGNETIC WAVES AND TRANSMISSION LINES

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1. a. State and Prove Gauss's Law. [7]
   b.Let $\bar{J}$= 400Sinθ/(r^2+4) a_r A/m^2. Find the total current flowing through that portion of the spherical surface r=0.8 bounded by $0.1\pi<\theta<0.3\pi$,$0<\Phi<2\pi$. [7]

OR

2. a. Show That $\bar{J}= \rho\overline{v_d}$ [7]
   b. Given The Flux density D=16/r cos(2θ)$\bar{a}_\theta$ c/m^2, Find the total charge with in the region 1<r<2m, 1< θ<2rad,1< Φ<2π [7]

SECTION-II

3. a. State The Law required to calculate magnetic fluex density or magentic field intensity for a given current or current distribution and derive the expression for the same. [7]
   b. Derive the conditions at boundary surface of Dielectric-Dielectric interface? [7]

OR

4. a. Define and Explain Ampere's circuit Law. [7]
   b. State Maxwell's Equations in Differential and Integral form with clear statement. [7]

SECTION-III

5. a. Derive the equation for uniform plane wave in terms of H. [7]
   b. A 100MHz uniform plane wave Propagates in a lossless medium for which €$_r$ =5 and μ_r=1 find v_p,β,λ,E_s,H_s. [7]

OR

6. a. State and Prove the Poynting Theorem. [7]
   b. Write short Notes on [7]
   i) Total internal reflection ii) Brewster Angle

SECTION-IV

7. a. Derive The Expression for Transmission Line Equation. [7]
   b. Given R = 10.4 Ω/mt

L = 0.00367 H/mt
G = 0.8×10^{-4} mhos/mt
C = 0.00835 μF/mt.

Calculate Z_0 and γ at 1.0 KHz. [7]

OR

8. a)Derive the expression for α and β in terms of primary constants of a line [7]
   b) Explain transmission line parameters in detail. [7]

SECTION-V

9. a) Establish the relations for Z_{sc} and Z_{oc} of rf lines and sketch their variation with βl. [7]
   b) A 60ohm lossless line is 30m long and is terminated with a load of 75+j50ohms at 3MHz find its reflection coefficient,VSWR,if the line velocity is 60% of the velocity of light [7]

OR

10. a) Explain the principle of single stub matching. [7]
    b) Calculate the skin depth for the following conditions. [7]
    Copper $f=10^{10}$Hz,$\mu=\mu_0$, $\sigma=5.8 \times 10^7$s/m

***

R17

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech II year – II Semester Examinations

Model Paper-II

ELECTROMAGNETIC WAVES AND TRANSMISSION LINES

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1. a**. S**tate and explain coulomb's law? [7]
   b. Find the force on a charge of -100mC located at P(2,0,5) in free space due to another Charge of 300μC located at Q(1,2,3). [7]

OR

2. a. State and Prove Laplace's and Poissson's Equation Starting from Gauss's Law [7]
   b. The potential field $V=2x^2yz-y^3z$ exists in a dielectric medium having $\varepsilon=2\varepsilon_0$ calculate the total charge within the unit cube $0<x<1m, 0<y<1, 0<z<1m$. [7]

SECTION-II

3. a. Define Ampere's Circuit Law in point and integral forms for Static fields. [7]
   b. Establish the fields in the different regions of a coaxial cable carrying a current I, and sketch their variation with radial distance.

OR

4**.** a**.** State and Explain Biot-Savart's law. [7]
   b. A Potential field is given by $V=15(x^2-y^2)$.The point p(4,-2,1) lies on the boundary of the conductor and free space At P, obtain the magnitudes of i)V ii) E iii)D [7]

SECTION-III

5.a. Derive The attenuation and phase constant in conducting medium [7]
   b. A Sinusoidal varying EM wave in a medium of $\varepsilon_r=1$ $\mu_r=1$ is transmitting power at a density 1.2watts/m^2 .Find the maximum values of E and H fields. [7]

OR

6.a. Derive Expression for reflection and transmission coefficients of an EM wave when it is Incident normally on a dielectric. [7]

b. A perpendicularly polarized wave is incident at an angle of θ_i=15degrees. It is propagating from medium1 to medium2 .medium 1 is defined by ε_{r1}=8.5,μ_{r1}=1,σ_1=0 and medium 2 is free space if E_i=1mv/m, determine E_r, H_i, H_r. [7]

SECTION-IV

7. a. Derive the Condition for Distrotionless Transmission Line. [7]

b. Measurements on a Transmission Line of length 120Km were made at frequency of 6000Hz.If Z_{OC}=520(-30deg) and Z_{SC}=640(43deg) find Z_o and P. [7]

OR

8. a.Explain the conditions which are used for minimum attenuation in transmission line [7]

b. The propagation constant of a lossy transmission line is 1+j2 m^{-1} and its characteristic impedance is 20+j0Ω at ω= 1rad/s. Find R,C,L,G for the Line. [7]

SECTION-V

9. a. Derive the relation between reflection coefficient and characteristic impedance [7]

b. Write short notes on smith chart. [7]

OR

10. A transmission line of length 0.40λ ? has a characteristic impedance of 100Ω and is Terminated in a load impedance of 200 + j180ω. Find the [14]
    (i) Voltage reflection coefficient
    (ii) Voltage standing wave ratio
    (iii) Input impedance of the line.

R17

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech II year – II Semester Examinations

Model Paper-III

ELECTROMAGNETIC WAVES AND TRANSMISSION LINES

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks

SECTION-I

1. a. Define Line charge Density? Derive the infinite line Electric field $E=\rho_L/2\pi\varepsilon\rho\ a_\rho$ [7]

b. Find E at(2,0,2) if a line charge of 10PC/m lies along the y-axis [7]

OR

2. a. Define Capacitance and obtain the parallel plate capacitance

b. A parallel plate capacitance has 500mm side plates of square shape separated by 10mm distance A sulphur slab of 6mm plates with $\varepsilon_r=4$ kept is on the lower plate find the capacitance of the set up If a voltage of 100V is applied across the capacitor calculate the voltages at both the regions of the capacitor between the plates. [7]

SECTION-II

3. Derive an expression for magnetic field strength,H,due to a finite filamentary conductor carrying a current I and placed along Z-axis at a point 'P' on Y-axis.Hence deduce the magnetic field sgtrength for the length of the conductor extending $-\infty$ to $+\infty$. [14]

OR

4. a.Explain the inconsistency of Ampere's cicutal Law [7]

b.A certain material has $\sigma=0$ and $\varepsilon_r=1$ if $H=4\sin(10^6t-0.01z)\overline{a_y}$ A/m.Make use of Maxwell's equations to find μ_r. [7]

SECTION-III

5. a. Derive the relation between E and H for a uniform plane wave in dielectric medium. [10]

b. Explain polarization of uniform plane wave. [4]

OR

6.a. Define Polyting's theorem and Polyting Vector. [7]

b.Explain wave propagation in good dielectric medium**.** [7]

SECTION-IV

7. a)Explain the conditions which are used for minimum attenuation in transmission lines [7]

b) Derive the secondary conditions for loss less transmission line. [7]

OR

8. Show that for an uniform transmission line the following relations are valid

a) $Z_O=\sqrt{Zoc.Zsc}$ [7]

b) Tanhpl=$\sqrt{Zsc/Zoc}$ [7]

SECTION-V

9.a. Derive the expression for the input impedance of a transmission line of length L. [10]

b. List out the applications and losses of transmission lines [4]

OR

10. Describe the construction of smith chart and give its applications. [14]

R17

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech II year – II Semester Examinations

Model Paper-IV

ELECTROMAGNETIC WAVES AND TRANSMISSION LINES

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks

SECTION-I

1. a .Define and Derive the relation between E and V. [7]

   b. Prove the poisson's equation for Electrostatic field. [7]

OR

2. a.Distinguish between the conduction and convention currents. Calculate the relaxation time for brass material, having Conductivity of $1.1x10^7$mho/m at 10MHz. [7]

   b.Find the capacitance of a 50cm.long coaxial cable, having conductors of 4cm and 2cm diameters, separated by a medium of a relative permittivity 2.56. [7]

SECTION-II

3.a.Define Inductance? Derive the toroid inductance [7]

b.A toroid has air core and has a cross-sectional area of $10mm^2$.It has 1000turns and its mean radius is 10mm.Find its Inductance [7]

OR

4.a. Obtain the integral form of Maxwell's equation for time varying fields. [7]

b. In a medium of $\mu_r=2$, find E,B and displacement current density if H=$25\sin(2x10^8t+6x)a_y$ mA/m [7]

SECTION-III

5. a. For good dielectrics derive the expressions for α,β,γ and η. [7]

b. A plane wave travelling in a medium of $\varepsilon_r=1,\mu_r=1$ has an electric field intensity of $100x\sqrt{\pi}$V/m.Determine the energy density in the magnetic field and also the total energy density. [7]

OR

6. a Derive Expression for reflection and transmission coefficients of an EM wave. [7]

b. A perpendicularly polarized wave is incident at an angle of θ_i=15degrees. It is is free propagating from medium1 to medium2 .medium 1 is defined by $\varepsilon_{r1}=8.5,\mu_{r1}=1,\sigma_1=0$ and medium2 space if E_i=1mv/m, determine E_r, H_i, H_r. [7]

SECTION-IV

7.a.Derive the attenuation constant and phase constant in terms of primary constants [7]

b.Explain different types of loading for transmission lines. [7]

OR

8.a.Derive the characteristic impedance of a transmission line in terms of its line constants [7]

b.At 8MHz the characteristic impedance of a transmission line as 40-j2ohms and the propagation constant 0.01+j0.18 per meter.Find the primary constant. [7]

SECTION-V

9. a. Explain the principal of single stub matching [7]

b. Write Short notes on Smith Chart [7]

OR

10. a. Derive the relation between reflection coefficient and characteristic impedance

b. write short notes on smith chart. [7+7]

R17

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech II year – II Semester Examinations

Model Paper-V

ELECTROMAGNETIC WAVES AND TRANSMISSION LINES

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks

SECTION-I

1.a. State and prove Continuity equation. [7]

b. Three point charges Q1=0.5nC,Q2=0.4nC, Q3=-0.6Nc are located in free space at (0,0),(3,0) and (0,4) respectively. Determine the potential, electric field intensity and flux density at(3,4). [7]

OR

2. a. Determine the amount of work necessary to assemble three point charges Q1, Q2,Q3 in an empty space. Extend your result to n-point charges. [7]

b. Show that $\bar{J}= \rho\overline{v_d}$. [7]

SECTION-II

3. a. State and Prove the Ampere's Force Law. [7]

b.A toroidal ring has 200turns. The outer diameter of the ring is 15cm with the inner diameter of 12cm.Find the flux density if the current is 8A. [7]

OR

4. a. State and explain boundary conditions between two dielectric media.

b. A circular loop conductor having radius of 0.2m is placed in XY plane. The loop consists of a resistance of 10ohms. If the Magnetic field is B=Sin10^4t Tesla, find the current flowing in the loop. [7]

SECTION-III

5. a. Explain properties if uniform plane wave..

b.Derive the wave equation in dielectric medium. [7+7]

.

OR

6.a.Derive the equation for uniform plane wave in free space condition. [7+7]

b.The electric field in free space is given by E=50cos(10^8t+βx)a_yV/m. Find the direction of wave propagation. Calculate β and time it takes to travel a distance of λ/2.

SECTION-IV

7. Derive the equation for input impedance of the Eighth-Wave($\lambda/8$) line? Explain its significance. [14]

OR

8. Write Short notes on
i) Smith Chart
ii) Single stub matching [14]

SECTION-V

9.a. Derive an expression for the propagation constant and characteristic impedance of Transmission line with R, L,C, G.
b. A telephone line has R=30Ω/km, L=100Mh/km, G=0, C=20μF/km.
At f=1KHz, obtain i) Z_0 ii) propagation constant iii) phase velocity. [7+7]

OR

10.a. Derive an expression for the input impedance of a lossless line of length 'l' in Terms of Z_0,β,Z_L and l when terminated by a load Z_L.
b. A lossless transmission line length 'l' with Z_0=50 is terminated by a load of Z_L=50+j50.Determine the reflection coefficient "R_r" and the standing wave Ratio. [7+7]

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

UG Model question paper-I

CONTROL SYSTEMS
II YEAR II SEMESER
ECE &EEE

Time: 3 hours **Max Marks: 70**

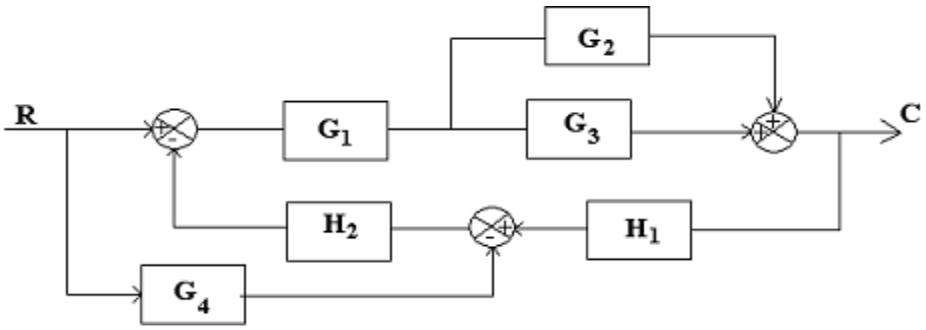
Note: This question paper contains of 5 sections. Answer five questions, choosing one question from each section and each question carries 14 marks.

SECTION-I

1 a) What are the basic elements of a control system?
b) Explain the advantages of signal flow graph over block diagram representation. (14M)

(OR)

2. Draw a signal flow graph for the Block diagram shown below and find its closed loop transfer function. (14M)



SECTION -II

3.Define transient response specifications.
i) Delay time ii) Rise time iii) Peak time iii) Peak overshoot
iv) Settling time of second order system (14M)

(OR)

4 a) Obtain the unit step response of a unity feedback system whose open loop transfer function is G(S) = 4/S(S+5). (7M)
b) Determine the step, ramp and parabolic error constants of the unity feedback Control system. The open loop transfer function is following.
G(S) = 1000/(1+0.1S)(1+10S) (7M)

SECTION-III

5. a) Write the necessary conditions for stability. (14M)

b) Consider a sixth order system with the characteristic equation, $S^6 + 2S^5 + 8S^4 + 13S^3 + 20S^2 + 16S + 16 = 0$. Using Routh's stability criterion, find whether the system is stable or not, give the reasons?

(OR)

6. Sketch the root locus plot of a unit feedback system with the open loop transfer function $G(S) = K/S(S+2)(S+4)$. (14M)

SECTION-IV

7. Explain the frequency domain specifications (14M)

(OR)

8.Sketch the Bode plot for $G(S)=200/S(S+5)(S+10)$. (14M)

SECTION-V

9.a) Define controllability and observability.

b) Evaluate the controllability of the system with the matrix (14M)

$$\begin{bmatrix} \dot{X}1 \\ \dot{X}2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -3 & -4 \end{bmatrix} \begin{bmatrix} X1 \\ X2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u$$

$$Y = \begin{bmatrix} 1 & 0 \end{bmatrix} X$$

(OR)

10.a)Obtain the state transition for the system (14M)

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -3 & 1 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

b) Explain about diagonalization.?

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

UG Model question paper-II

CONTROL SYSTEMS

II YEAR II SEMESER

EEE AND ECE

Time: 3 hours **Max Marks: 70**

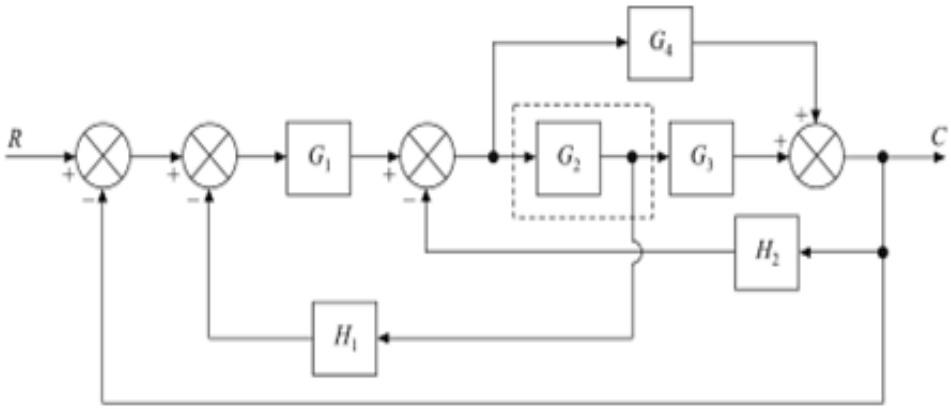
Note: This question paper contains of 5 sections. Answer five questions, choosing one question from each section and each question carries 14 marks.

SECTION-I

1. a) Explain the differences between closed loop and open loop systems with examples.
   b) Explain the effect of feedback and feedback characteristics (14M)

OR

2. Determine the Transfer function of the Block Diagram shown below using block diagram reduction technique. (14M)



SECTION –II

3.For a unity feedback system whose open loop transfer function is G(S) = 4/S(S+5).Find Wn,ξ.? (14M)

OR

4 Find the delay time, rise time, peak time, settling time and peak overshoot for unity feedback system with open loop transfer function (14M)

$$G(s) = \frac{16}{s(s+6)}$$

SECTION-III

5 a.The characteristics equations a feedback control system is given as $s^3+2Ks^2+(K+2)s+4 = 0$ Determine the value of K for which the system to be stable with the help of Routh Hurwitz criterion.

b. write the various construction rules to develop the root locus (14M)

OR

6. Sketch the root locus plot of a unit feedback system with the open loop transfer function G(S) = K/S(S+2)(S+4). (14M)

SECTION-IV

7 a.. Explain the general procedure to construct bode plot

b.. For a certain control system sketch the polar plot $G(S)H(S) = \frac{1}{S(S+2)(S+10)}$ (14M)

OR

8 . Sketch the polar plot for G(S) = 1/s(1+s)(1+2s) and determine the gain and phase margins. (14M)

SECTION-V

9. Obtain the state transition matrix for the system (14M)

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -3 & 1 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

OR

10. Diagonalize Matrix A in the system

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1 & -2 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} r(t)$$

(14M)

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

UG Model question paper-III

CONTROL SYSTEMS

II YEAR II SEMESER

EEE and ECE

Time: 3 hours **Max Marks: 70**

Note: This question paper contains of 5 sections. Answer five questions, choosing one question from each section and each question carries 14 marks.

SECTION-I

1.a) Define the transfer function in control system

b)Define effect of feedback on sensitivity, stability and gain (14M)

OR

2.State and explain the Mason's gain formula. (14M)

SECTION-II

3. Explain effects of proportional derivative and proportional integral controllers in system performance (14M)

OR

4. A unity feed back system is characterized by an open loop transfer function G(s)= s(s +5) K . Determine the gain K so that the system will have a damping factor of 0.7. For this value of K determine the natural frequency of the system. It is subjected to a unity step input. Obtain the closed loop response of the system in time domain (14M)

SECTION-III

5. Derive the expressions for frequency domain specifications of a second order system. (14M)

OR

6. Given the open loop transfer function of a unity feedback system G(s) = $10(S+2)/S(S+5)$.Draw the Bode plot and measure from the plot the frequency at which the magnitude is 0 Db? (14M)

SECTION-IV

7. write the various construction rules to develop the root locus (14M**)**

OR

8. Given the open loop transfer function G(s) = $k/(S+5)(S+10)$. Sketch the polar plot and investigate the open loop and closed loop systems stability (14M)

SECTION-V

9.state equation of a system is given by (14M)

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -3 & 1 \\ -2 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u(t), \quad t>0$$

OR

10.a) Is the system controllable?

b) Compute the state transition matrix (14M)

c) Compute x1(t) under zero initial condition and a unit step input

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -3 & 1 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

R17

Code No: R17A0551

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech IISemester MODEL QUESTION PAPER

DATABASE SYSTEMS

(ECE& MECH)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: .Question paper Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION – I

1. Explain about Database architecture with a neat diagram?

OR

2. What are the advantages of DBMS over file management system?

SECTION – II

3. Explain the following with examples.

a) Key constraints. b) Foreign key constraints.

OR

4. What is a view? Explain about views in detail?

SECTION – III

5. Explain the following

a) Joins b)Aggregate functions

OR

6. Explain the following

a) UNION b) INTERSECT c) EXCEPT

SECTION – IV

7. What is Normalization? Explain 1NF,2NF?

OR

8. What is MVD explain in brief?

SECTION – V

9.What is Transaction state? And explain ACID properties?

OR

10. Explain the concept of serilizability?

****

R17

Code No: R17A0551

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech IISemester MODEL QUESTION PAPER

DATABASE SYSTEMS

(ECE& MECH)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: .Question paper Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION – I

1. a) Describe storage manager component of database system structure?
b) Explain levels of abstraction in DBMS

OR

2. Write a short notes on database languages with examples?

SECTION – II

3. Explain the E-R diagram components and notations with their extended features?

OR

4. Explain the keys
a) primary key b)foreign key c) super key d) candidate key

SECTION – III

5. Define BCNF? How does BCNF differ from 3NF? Explain with an example.

OR

6. What is Redundancy? What are the different problems encountered by redundancy? Explain them.

SECTION – IV

7. What is functional dependency? Explain about dependency preserving?

OR

8. Explain the following
a) 4NF b) 5NF

SECTION – V

9. What are the transaction isolation levels in SQL?

OR

10. Write short notes on recoverability?

****

R17

Code No: R17A0551

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B. Tech IISemester MODEL QUESTION PAPER

DATABASE SYSTEMS

(ECE& MECH)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: .Question paper Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION – I

1. Define DBMS? List Database system applications.

OR

2. List four significant differences between a file processing system and a DBMS?

SECTION – II

3. a) Write a detail note on participation constraints?
b) What is the class hierarchy? How is it represented in the ER diagrams?

OR

4. Explain the concept of Triggers?

SECTION – III

5. what is nested query explain with suitable example?

OR

6. Explain the following
a) NULL values b) HAVING clause c)GROUP BY

SECTION – IV

7. Explain FD and MVD with examples

OR

8. What is Normalization? Discuss what are the types? Discuss the 1NF, 2NF, 3NF with example?

SECTION – V

9. Explain the concept of testing on serializability?

OR

10. What is Transaction state? And explain ACID properties?

****